International Journal of Electrical and Computer Engineering (IJECE)
Vol. 11, No. 2, April 2021, pp. 1053~1062
ISSN: 2088-8708, DOI: 10.11591/ijece.v11i2.pp1053-1062

Elevator controller based on implementing a random access memory in FPGA

Azzad Bader Saeed
Electrical Engineering Department, University of Technology, Baghdad, Iraq

Article Info

Article history:

Received Jun 25, 2020
Revised Sep 9, 2020
Accepted Sep 23, 2020

Keywords:

Elevator controller
FPGA
Look-up-table
Processing time
Programmable logic block

ABSTRACT

Previous techniques of elevator controllers suffer from two main challenges: processing time, and software size. In this work these challenges have been overcame by implementing a controller random access memory (RAM) in a fast FPGA for a proto-type of two-floors elevator, as known the RAM and FPGA are fast devices. A look-up-table LUT (which is fast technique) has been proposed for this work, this LUT has represented a proposed relation between 10 and 7 lines, the states of the sensors and switches have been represented by the 10 input lines, and the commands for the motors of slide door and traction machine have been represented by the 7 output lines. The proposed LUT has been schematically realize by a (10×7) bits RAM which has been implemented in field programmable gate arrays (FPGA). The proposed system has been performed using 'ISE Design Suit' software package and FPGA Spartan6 SP-605 evaluation kit, the clock frequency of this FPGA is 200 MHz which is respectively high. The processing time and software size of the proposed controller had reached to 20ns and 3.75 MB, which they are less than that obtained from the results of previous techniques.

This is an open access article under the CC BY-SA license.

Corresponding Author:

Azzad Bader Saeed
Electrical Engineering Department
University of Technology
Al-Sina'a street, Baghdad, Iraq
Email: azzad.b.saeed@uotechnology.edu.iq

1. INTRODUCTION

Human can easily move upward or downward from floor to another using the elevators. Today elevators have been developed to include: 1) video and audio calling, 2) stand by power supply to overcome the suddenly cutting off the main AC supply 220 Volt, 3) many safety instruments such as Fan for moving the air inside the car of the elevator [1]. Elevators are characterized by their: speed of moving, processing speed, number of floors, reliability, performance precision, and type of the controller [2]. Two types of elevators are available today: electro-mechanical and hydraulic-powered, the electro-mechanical type (which is widely used in most buildings) involves three principle units: car, counterweight, and traction machine [3]. The hydraulic-powered type (which is hardly used in buildings) consists of a main pipes system, these pipes are composed in telescope shape, this pipes system positioned below the ground floor, it is powered by an electrical liquid pump [4].

Usually, the traction machine of the elevator includes a DC motor which is fed by an AC to DC power supply, they are positioned in a special room at the top of the elevator. This motor rotates in two directions, clockwise and anticlockwise, in clockwise direction the car of the elevator moves upward, while in anticlockwise the car will move downward [5]. A rapped steel wire is used to tie the car and the

counterweight precisely, the DC motor moves this steel wire in two directions through several pulleys [6]. The counterweight of the elevator is used to balance with the weights of the car and the human in it, whereas it reduces the load torque on the motor when the car moves upward [7]. Usually, the weight of the counterweight equals the car weight with 40% of the maximum rated load [8]. When the traction machine moves the car upward, then the counterweight goes downward, while when the car moves downward, then the counterweight goes upward [9], i.e. the car and counterweight move in opposite directions.

Each electromechanical elevator consists of a controller, manual switches, and sensors [10]. Usually, the controller involves a processor unit which presents commands according to the status of the switches and sensors [11]. The number of the manual switches depends on the number of available floors, each floor has its special control switch in the car [12], there are also two switches in the car are used to open and close the slide door [13]. At each floor there is a manual switch outside the car is used for car calling [14]. Several sensors are used in the elevators such as, floor position sensors, sensors of entry and exit from the car, maximum human weight sensors, and sensors of slide door opening and closing. Another motor is used in the elevators, which is used for open and close the slide door of the car, modern elevators include video calling and spare power supplies [15]. Two kinds of electro-mechanical elevator are shown in Figure 1, the first one is the lifting drum, and the second is traction drive.

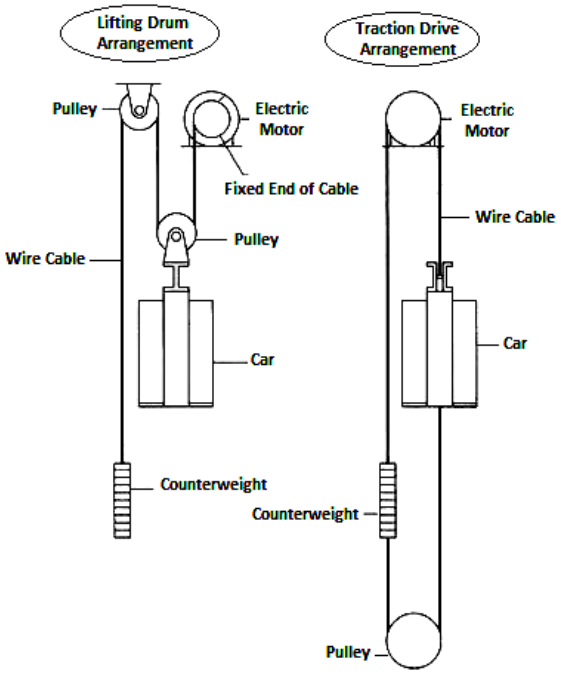

Figure 1. Two kinds of electric-mechanical elevator

There are three main types of controllers are widely used in elevators: the first technique uses C or assembly language as a software controller for the elevator, which is performed by microprocessor or microcontroller (as embedded system), where it has presented accepted results of processing time and software size [16]. The second technique uses the fuzzy-logic system as a software controller (that is also performed by microprocessor or microcontroller) for the elevator, which is the best in processing and operation and has low software size but it is slow system [17]. The third technique uses a verilog hardware design language (VHDL) code program as a software controller that is implemented in field programmable gate array (FPGA), which it has also presented accepted results of processing time and software size [18]. All these previous works present 200 ns as minimum processing time, and 10 MB as minimum software size, these values are high respectively, which is the problem. This problem has been solved in this article, whereas these results have been reduced to minimum possible values.

In this work, the look-up-table concept has been used to overcome the problem of processing time and software size of previous techniques, which is fastest decision system and it has lowest software size, it is a direct and fast relation between input and output parallel data [19, 20], the input parallel data represent the status of manual switches and sensors, and the output data represent the decisions. In same time, the random

access memory (RAM) has been used in the proposed system, as known it is considered as fastest storage device [21], it presents a fast relation between parallel address bits and parallel data bits [22]. Another device has been used in this work, which is the FPGA, it is widely used in processing systems due to the following features: 1) fast device due to its parallel processing, 2) low cost, 3) the capability of upgrading, 4) high reliability, 5) low power consumption [23, 24]. Note, in this work, the reducing of processing time was the first reason for using the FPGA and the RAM, while the other reasons are capability of upgrading, reliability, low cost, and low power consumption [25].

There are 10 input and 7 output lines in the proposed look-up-table. The status of the manual switches and sensors has been represented by the 10 input lines, and the commands for the motors of the slide door and traction machine have been represented by the 7 output lines. This look-up-table (LUT) has been performed schematically by a 10×7 bits RAM, then this schematic RAM has been converted to VHDL code program, and finally this program has been uploaded into FPGA (Xilinx Spartan6 SP-605 kit). All these processes have been executed using 'ISE Design Suit' software package. The input and output lines of the proposed LUT have been represented by the address and data lines of the schematic RAM. After implementing the proposed LUT into the FPGA, the last one has operated as a real RAM, so at final step, the FPGA has been programmed by inserting the proposed data bits of the schematic RAM into corresponded address locations. In this time the FPGA was ready to operate as the proposed controller for 2-floors elevator. A Practical test has been applied to the proposed controller using 10 input manual switches at the address lines, and 7 light emitting diodes LEDs at the data lines of the FPGA, it has been observed that the processing time was nearly 20ns, and the software size was 3.75 MB. It is worth to mention that these results were so less than that of the previous related techniques.

The FPGA is an integrated circuit device is composed from many flip-plops, NAND, and OR gates, they connected in a specific manner for build the Programmable Logic Blocks PLDs, and many PLDs are included in FPGA [26]. The FPGA is found to implement huge digital electronic systems [27]. A specific task can be performed by FPGA by uploading a suitable VHDL code program in it, the FPGA can only programmed by this type of codes (VHDL) [28]. The FPGAs are characterized by their, fast processing, low cost respectively, upgrading capability, high performance, high reliability, low power consumption [29]. There are two main types of FPGAs: Xilinx and Altera, they differ in the internal design and connections. The FPGAs differ by their, clock frequency (speed), maximum software size capability, and number of input/output lines [30].

2. RESEARCH METHOD

In this paper, a look-up-table LUT (which is fast processing and easy technique) [19, 20] has been designed as an elevator controller. This LUT has been implemented by schematic RAM that has been implemented in FPGA. The LUT of the proposed elevator has been designed with 10 input and 7output lines, the 10 input lines correspond to the states of 1) all the used sensors, 2) the switches at each floor outside the car, 3) the floor selection switches in the car, 4) the switches of opening and closing the slide door of the car. The 7 output lines correspond to the commands of the: 1) motors of the slide door and traction machine, 2) clearing the flip-flops of all of the used switches. In this work, a schematic 10×7 bits RAM has been used to implement the proposed LUT, this process has been performed by the 'ISE Design Suit' software package. Several points have been considered to design the proposed LUT, they are:

- Two floors have been used in the proposed prototype elevator.
- There are 4 switches inside the car, 2 switches for floor selection, and 2 switches used to open and close the slide door.
- There are 2 switches outside the car are used for floor calling, the first one used for ground floor, and the other for the first floor.
- There are 4 sensors: 2 sensors are used for floor position reaching, and the other 2 are used for producing signals when the slide door of the car is closed and opened.

When the schematic 10×7 bits RAM has been designed to represent the proposed LUT, the 10 input lines of the LUT is corresponded by the 10 address lines of the RAM, and the 7 output lines of the LUT is corresponded by the 7 data lines of the RAM. The data and address bits of the RAM is assigned as shown:

X_0: switch status is used for car calling, it is located at ground floor
X_1: switch status is used for car calling, it is located at first floor
X_2: switch status inside the car is used for calling the ground floor
X_3: switch status inside the car is used for calling the first floor
X_4: switch status inside the car is used to close the slide door
X_5: switch status inside the car is used to open the slide door
X_6: sensor status is used to present signal when the door is closed

X_7: sensor status is used to present signal when the door is opened
X_8: sensor status for reaching the ground floor
X_9: sensor status for reaching the first floor
Y_0: move the car upward
Y_1: move the car downward
Y_2: slide door closing
Y_3: slide door opening
Y_4: reset all the flip-flops of all switches
Y_5: busy signal generation
Y_6: reset the flip-flops of X_4, X_5 switches inside the car

Table 1 illustrates the moving steps probabilities which are required for the proposed elevator. This table shows 20 steps of relation between address and data bits of the proposed schematic RAM. The 8×1 bits RAM is the maximum available size of RAM that is included in the 'ISE Design Suit' software package, but the required size of RAM in the proposed system is 10×7 bits. At first step a schematic of 10×1bits RAM has been composed using four 8×1 bits RAM and the de-multiplexer M4_1E which is shown in Figure 2, as shown, the XLXN_4(7:0), XLXN_8, and XLXN_9 pins corresponds to the 10 address lines, and XLXN_10 pin corresponds to 1 data line. The next step was to generate a schematic of 10×7 bits RAM, which is performed by combination of 7 of the schematic 10×1 bits RAM. The next generated schematic RAM is 7×(10×1)) bits that corresponds to 10×7 bits RAM, the final required RAM has been illustrated in Figure 3, as shown in this final schematic RAM, the XLXN_4(7:0), XLXN_8, and XLXN_9 pins corresponds to 10 address lines, and the (XLXN_3-XLXN_9) correspond to the data lines.

The next process is the converting of the generated schematic 10×7 bits RAM to VHDL code program using 'ISE Design Suit' software package, then this program has been uploaded into the FPGA Xilinx Spartan6 (type: SP-605 evaluation kit, after this step the FPGA became the proposed controller 10×7 bits RAM. The final process has been performed by storing the required 20 data in the corresponded 20 address locations as shown in Table 1.

Table 1. Address and data bits of the proposed controller RAM

Address bits	Data bits
$X_0X_1X_2X_3X_4X_5X_6X_7X_8X_9$	$Y_0Y_1Y_2Y_3Y_4Y_5Y_6$
1000000101	0010010
1000001001	0100010
1000001010	0001010
1000000110	0000010
1001100110	0010010
1001001010	1000011
1001001001	0000010
1001011001	0001010
1001010101	0000110
0000000101	0000000
0100000110	0010010
0100001010	1000010
0100001001	0001010
0100000101	0000010
0110100101	0010010
0110001001	0100011
0110001010	0000010
0110011010	0001010
0110010110	0000110
0000000110	0000000

For testing the proposed controller, and depending on Table 1, one can start with pushing ON the switch X_0 of car calling by someone at ground floor, where the car in the first floor, so the address number $(1000000101)_2$ will be presented at the RAM address lines, in this time, all the switches X_2-X_5 in the car, the switch X_1, and the switch X_8 are OFF (LOW). The binary number $(0010010)_2$ will be produced at the RAM data lines, which means the states of Y_2, Y_5 are ON (HIGH), and all other data bits Y_0, Y_1,Y_3,Y_4, Y_6 are OFF (LOW), in this case the controller RAM commands the slide door motor to close the door, and produce the Busy signal. After the slide door will be closed, then the binary number $(1000001001)_2$ will be produced at the RAM address lines, referring to this number, the sensor state X_6 became ON (HIGH), and the sensor state X_7 became OFF (LOW). At this moment the binary number$(0100010)_2$ will be produced at the RAM data lines, the state of data line Y_1 became ON (HIGH) and the state of Y_5 became ON (HIGH) too, this will

command the traction motor to move the car in downward direction toward the ground floor, and in same time produce busy signal.

When the car is reached to the ground floor the binary number $(1000001010)_2$ will be produced at the RAM address lines, in this case the sensor state X_8 became ON (HIGH), and the sensor state X_9 became OFF (LOW). At this time the binary number $(0001010)_2$ will be produced at the RAM data lines, here the state of Y_1 became OFF (LOW), and the state of Y_3 became ON (HIGH), this mean that the controller RAM will command the car to stop and then command the motor to open the slide door. After that, the person will enter the car of the elevator then he push the switch of closing the door. Next steps of Table 1 will be performed until reaching the person to the first floor and then he open the slide door to get out from the car.

The proposed controller has been practically implemented in the FPGA Xilinx Spartan-6 (type: Sp-605 evaluation kit), this implementation is shown in Figure 4. As illustrated in this figure, there are two connected boards, the upper is the experimental board which contains seven light emitting diodes LEDs, they correspond to the seven output (data) bits of the controller, in same time it contains ten switches, which correspond to ten input (address) lines of the controller. The lower board is the FPGA, the clock frequency of this FPGA is 200 MHz. As shown in this figure the two boards have been connected by 17 wires, 10 for address lines, and 7 for data lines.

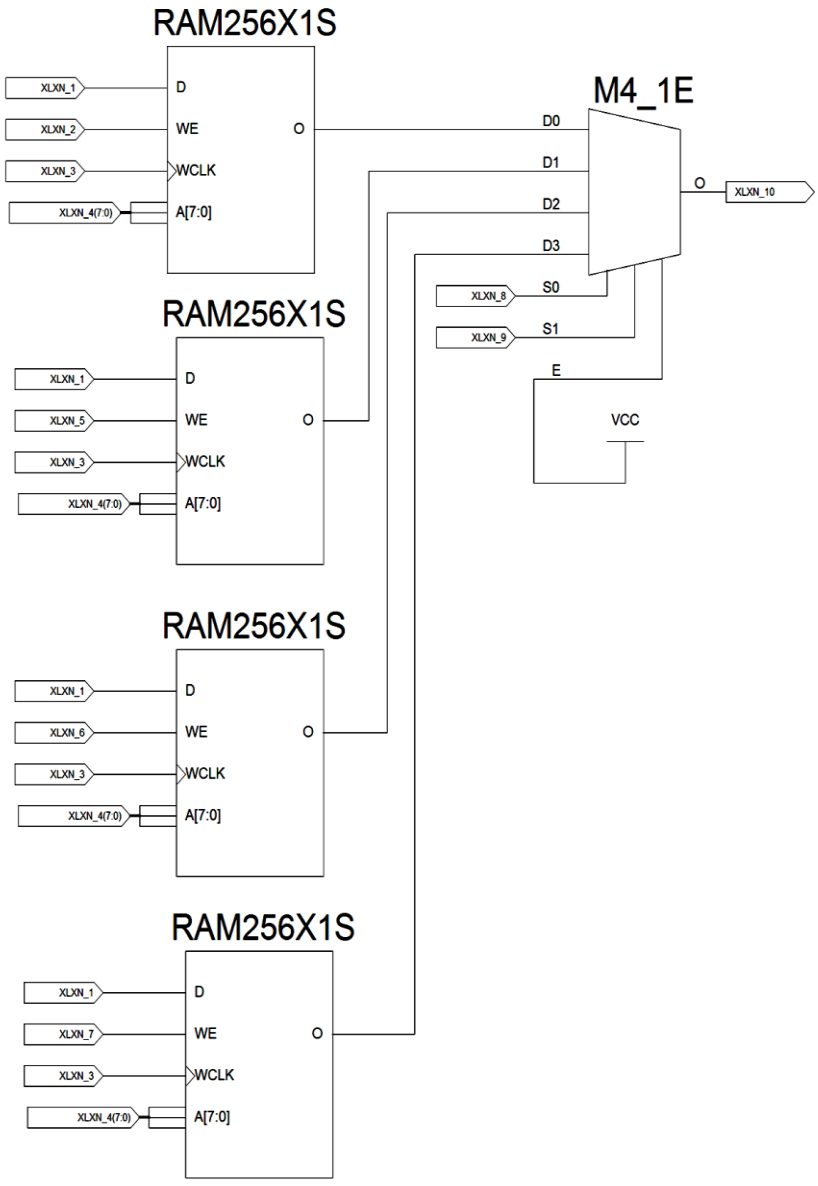

Figure 2. The schematic design of the proposed (10×1) bits RAM

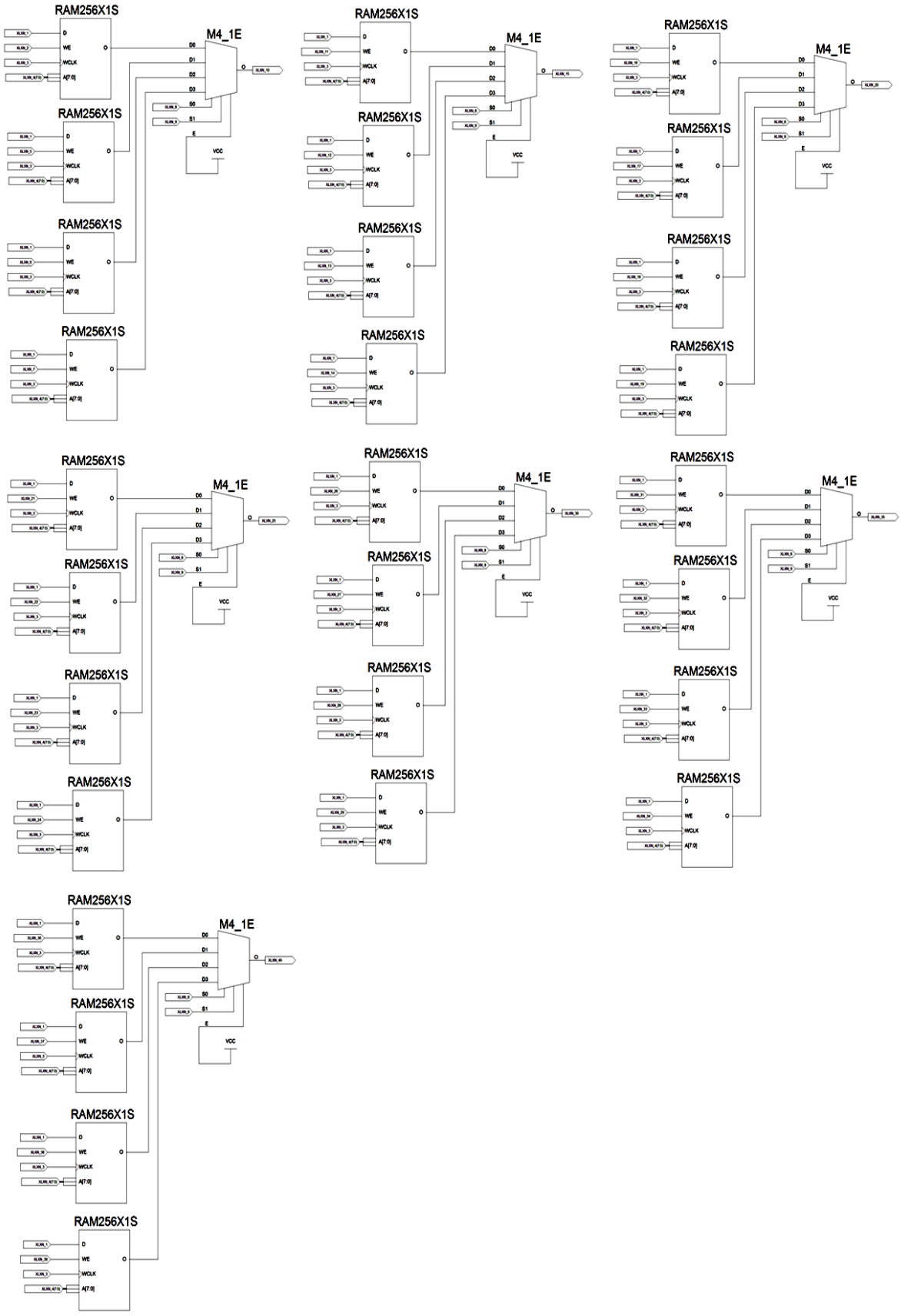

Figure 3. The complete schematic design of the proposed 10×7 bits RAM

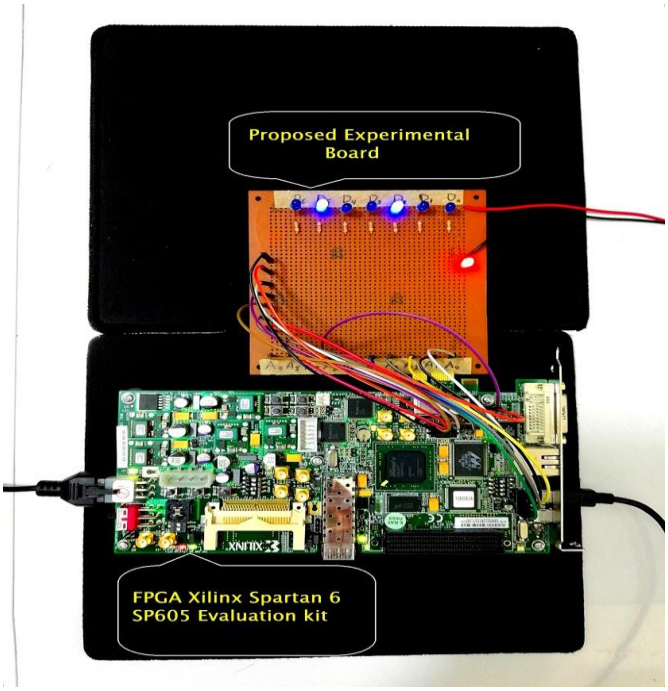

Figure 4: Practical implementing of the proposed controller using FPGA

3. RESULTS AND DISCUSSIONS

After completing the schematic design of the proposed 10×7 bits RAM, it has been converted to VHDL code program, this program has been uploaded into the FPGA Xilinx Spartan-6 (type: SP-605 evaluation kit), which has been performed using the software package 'ISE Design Suit v14.5'. The clock frequency of this FPGA is 200 MHz. Two main results have been obtained by practical testing of the proposed controller with using the oscilloscope, they are: the processing time was nearly 20 ns, and the software size was 3.75 MB. Note the software size capacity of the used FPGA is 150 MB.

As a result of practical testing of the proposed controller, The software package' ISE Design Suit' presents a report of successfulness of the proposed software, the main part of this report is shown in Figure 5. As shown in this figure, the proposed name of the implementing file is elevator, and the design goal has been presented which is balanced. This report shows that the errors and warning are never occurred during the testing of the proposed file, and the generated VHDL code program was successful. The report shows that the number of 'slice LUTs' was 1% from the maximum capacity of the FPGA, the number of 'Used as Logic' was 1%, and the number of 'Used as Memory' was 1%, which they are also so slight values that making the proposed program small in size.

There are several related works had proposed various designs of elevator controller. Some of them had proposed software in C and Assembly language that have been executed using microprocessors and microcontrollers. Some of related works has used the Fuzzy-logic controller system, and few of them had used the FPGA as a processor. These related works has been discussed as follows:

Ismail *et al*., [31] had proposed a simulation of elevator controller based on Fuzzy-logic intelligent system, whereas, this simulation is not practically implemented. The energy and time have been considered in this work, the energy has been controlled for different loads, more energy is consumed for higher load when the car of the elevator is fully occupied by persons and moves in upward direction, and lower energy is consumed for lower load when the car is fully occupied and moves in downward direction. This work has designed multi-simulation systems for different heights of buildings. The simulation size of this work (for minimum height state) has reached to 50 MB, while the processing (performing) time has reached to 950 nsec. As shown, the obtained results of this work are so higher from that of the proposed work of this paper.

Muhammad *et al*., [32] had proposed an efficient elevator controller with three levels using Verilog-HDL code program, this proposed controller is used for different number of floors. The proposed controller of this work is a simple model that have 8-input lines and 2-output lines, the input lines are connected to 6-switches and single clock signal, while the 2-output lines are connected to floor number display and main DC motor used for upward/downward moving. The proposed controller of this work has ignored an important element, which is the controlling of door motor. The proposed HDL program of this work had been

implemented in FPGA Xilinx Spartan-3 which has clock frequency 50 MHz. The software size of this work had reached to 10 MB, while the minimum processing time had reached to 200 nsec. As illustrated, the simulation size and the processing time of this work are higher than that of the proposed work of this paper.

circuit Project Status (07/06/2019 - 00:35:10)			
Project File:	elevator.xise	**Parser Errors:**	No Errors
Module Name:	circuit	**Implementation State:**	Programming File Generated
Target Device:	xc6slx45t-3fgg484	**• Errors:**	No Errors
Product Version:	ISE 14.5	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	54,576	0%	
Number of Slice LUTs	119	27,288	1%	
Number used as logic	7	27,288	1%	
Number using O6 output only	7			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as ROM	0			
Number used as Memory	112	6,408	1%	
Number used as Dual Port RAM	0			
Number used as Single Port RAM	112			
Number using O6 output only	112			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as Shift Register	0			
Number of occupied Slices	33	6,822	1%	
Number of MUXCYs used	0	13,644	0%	
Number of LUT Flip Flop pairs used	119			
Number with an unused Flip Flop	119	119	100%	

Figure 5. The main part of report of the testing of the proposed controller

Jillsmon *et al*., [18] had built a Verilog-HDL code program for elevator controller that is used with different building heights, number of floors, and persons weight. This work had used an algorithm in its software, which is used for reducing the number of required computations. The controller of this work had been uploaded into FPGA Xilinx Artix-7 which has clock frequency 50 MHz. The size of the proposed software of this work had reached to 15 MB, and the processing time had reached to 400ns. One can observe that the software size and processing time of this work are higher than that of the proposed controller of this paper. Table 2 shows a comparison between the results of the proposed work of this paper and the related works.

Table 2. Comparison between results of the proposed work of this article with the related works

Work	Implementation	Processing Time	Software size	Upgrading Capability
of this paper	in FPGA Spartan-6 SP605 kit	20 nsec	3.73 MB	yes
Ismail S. *et al*., [31]	Not implemented	950 nsec	50 MB	yes
Muhammad A. *et al*., [32]	in FPGA Xilinx Spartan-3	200 nsec	10 MB	yes
Jillsmon V. *et al*., [18]	in FPGA Xilinx Artix-7	400	15 MB	yes

4. CONCLUSION

The main challenges of this work are: processing time ,and software size, the first challenge has been overcame using the fast tools RAM and FPGA, where these tools can be upgraded and programmed easily, which are preferred features. The second challenge has been overcame using LUT technique, this technique is considered as a fast technique of relation between input and output data, also this technique can be designed with small size of software. Using these devices and techniques, one can implement a fast elevator controller. The LUT can be implemented by schematic RAM which can be converted to VHDL code program, then the last one can be uploaded into FPGA. Using the software package 'ISE Design Suit', one can implement the proposed fast controller easily. The proposed fast controller has presents wonderful results, where the processing time was nearly 20ns, and the proposed software size was 3.75 MB. The first result has been obtained due to: i) the proposed fast techniques and tools, ii) the 200 MHz clock frequency of the used FPGA. By increasing the input and output lines of the controller (which means increasing of switches, sensors, and output command), the proposed software size will be increased. The propose work has used the RAM rather than the ROM (read only memory) as a controller because the RAM is so faster than the ROM.

REFERENCES

[1] Seung-Tae P. and Bo-Suk Y., "An implementation of risk-based inspection for elevator maintenance," *Journal of Mechanical Science and Technology*, vol. 24, no. 12, pp. 2367-2376, 2010.

[2] Kheir Al-Kodmany, "Tall Buildings and Elevators: A Review of Recent Technological Advances," *Buildings journal*, vol. 5, no. 3, pp. 1070-1104, 2015.

[3] Tomasz H. and Roman T., "Novel Rope-Free Mechatronic Elevator System to Automation of Transport in Agricultural Farms," *Journal of Engineering for Rural Development*, no. 15, pp. 318-323, 2016.

[4] Chaitali M., et al., "A new Technique of Rope Free, Motor less Elevator using Electromagnetic Principle," *Imperial Journal of Interdisciplinary*, vol. 3, no. 9, pp. 858-861, 2017.

[5] Shuang Zheng and Fugang Liu, "The Design of Elevator Control System Based on PLC and Configuration," *Advances in Computer Science, Intelligent System and Environment*, vol. 104, pp. 743-748, 2011.

[6] Omkar M. Shete1, et al., "Design and Control of an Elevator Control System Using PLC," *International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering (IJIREEICE)*, vol. 5, no. 4, pp. 142-146, 2017.

[7] May Thu Win, et al., "Design and Implementation of Elevator Control System by Arduino Microcontroller," *International Journal of Science, Engineering and Technology Research (IJSETR)*, vol. 7, no. 12, pp. 815-819, 2018.

[8] Kamalu U. A. and Ogunleke F. A., "Implementation of a Four-Floor Programmable Logic Controlled Elevator System," *International Journal of Scientific & Engineering Research (IJSER)*, vol. 9, no. 6, pp. 969-985, 2018.

[9] Ganesh Nomula, et al., "Design and Analysis of Elevator Control System Using PLC," *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, vol. 8 no. 12S2, pp. 277-281, 2019.

[10] Vladimir S., "Properties of the Rubber Vibration Isolator of the Elevator," *MATEC Web of Conferences*, vol. 251, no. 1, pp. 1-5, 2018.

[11] S. B. Ron Carter and A. Selvaraj, "Design and Implementation of PLC based Elevator," *International Journal of Computer Applications*, vol. 68, no. 7, pp. 4-10, 2013.

[12] A. M. Anusha and Ashok V. Sutagundar, "Design of a PLC Based Elevator Control System," *International Journal on Emerging Technologies*, vol. 6, no. 2, pp. 32-36, 2015.

[13] Abdelkarim Ahmed Eltahir and Zhang Jiang Min, "Design of Five Floors Elevator with SCADA System Based on S7200 PLC," *International Journal of Science and Research (IJSR)*, vol. 5, no. 4, pp. 1309-1314, 2016.

[14] Viveka L., "Elevator Installation in Virtual Reality: How practicing in virtual reality affects learning experience and could it enhance the transfer of training," University of Tampere, Master's Thesis, 2018.

[15] Chang L., et al.," The Elevator Fault Diagnosis Method Based on Sequential Probability Ratio Test (SPRT)," *Science Publishing Group, Journal of Automation, Control and Intelligent Systems*, vol. 5, no. 4, pp. 50-55, 2017.

[16] Ahmed Al Mansur, et al.," Design and Development of PC Based Elevator Control Systems via ATmega32 Microcontroller," *SEU Journal of Science and Engineering*, vol. 10, no. l, pp. 102-107, 2016.

[17] Pasura A., et al., "An Elevator Kinematics Optimisation Method for Aggregate Production Planning Based on Fuzzy MOLP Model," *International Journal of Mechanical Engineering and Robotics Research*, vol. 7, no. 4, pp. 422-427, 2018.

[18] Jillsmon V., et al., "FPGA Implementation of Elevator Controller," *International Journal of Computer Applications*, pp. 5-8, 2015.

[19] P. Jardin, G. Baudoin," Filter Look up Table method for Power Amplifiers Linearization," *IEEE Transactions on Vehicular Technology*, vol. 56, no. 3, pp. 1076-1087, 2007.

[20] Jason Cong, et al., "Energy-Efficient Computing Using Adaptive Table Lookup Based on Nonvolatile Memories," *International Symposium on Low Power Electronics and Design (ISLPED)*, Beijing, 2013, pp. 280-285.

[21] Azath Mubarakali, et al., "A new efficient design for random access memory based on quantum dot cellular automata nanotechnology," *Nano Communication Networks*, vol. 21, pp. 1-8, 2019.

[22] Shuting Liu, et al., "Flexible and fully biodegradable resistance random access memory based on a gelatin dielectric," *Nanotechnology*, vol. 31, no. 25, pp. 1-7, 2020.

[23] Steve K., "Advanced FPGA Design: Architecture, Implementation, and Optimization," *John Wiley & Sons, Inc.*, Canada, 2007.
[24] Ian K., et al., "FPGA Architecture: Survey and Challenges," in *Electronic Design Automation*, vol. 2, no. 2 (2007), pp. 135–253, 2008.
[25] Ian G., "Digital Systems Design with FPGAs and CPLDs," *Elsevier Ltd*, 2008.
[26] Ted H., et al., "Handbook of FPGA Design Security," *Springer Netherlands*, no. 1, 2010.
[27] Daniel A. S., "Analog and Digital Electronics," *Daniel Adam Steck*, 2017.
[28] Roger W., et al., "FPGA-Based Implementation of Signal Processing Systems," *John Wiley and Sons, Ltd.*, 2008.
[29] Azzad Bader Saeed, "Simulation Design of an Intelligent System for Automotive Transmission Gearbox Based on FPGA," *EMITTER International Journal of Engineering Technology*, vol. 6, no. 2, pp. 395-411, 2018.
[30] Azzad Bader Saeed and Sabah Abdul-Hassan Gitaffa, "FPGA Based Design of Artificial Neural Processor Used for Wireless Sensor Network," *EMITTER International Journal of Engineering Technology*, vol. 7, no. 1, pp. 200-222, 2019.
[31] Ismail S. and Abdullah A. "Controlling of Load Elevators by the Fuzzy Logic Method," *International Journal of Electrical and Computer Engineering*, vol. 7, no. 8, pp. 1079-1082, 2013.
[32] Muhammad A. and M. A. Saeed, "Design and Implementation of Efficient Elevator Control System using FPGA," *International Journal of Innovation and Applied Studies*, vol.9, no. 4, pp. 1541-1546, 2014.

BIOGRAPHY OF AUTHOR

Azzad Bader Saeed is inventor and lecturer, he received the Msc. Degree in electronic engineering in 2005 from University of Technology in Iraq, and he received the PhD. Degree in electronic engineering in 2017 also from University of Technology in Iraq. He is currently an affiliate and faculty in Electrical Engineering Department in University of Technology in Iraq. He is a member of the Iraqi Inventors and Creator Association.