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Monitoring and controlling the speed and direction of a DC motor through FPGA and comparison of FPGA for speed and performance optimization

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ABSTRACT

We are living in the 21st century, an era of acquiring necessity in one click. As we, all know that technology is continuously reviving to stay ahead of advancements taking place in this world of making things easier for mankind. Technology has been putting his part in introducing different projects as we have used the field programmable gate arrays (FPGAs) development board of low cost and programmable logic done by the new evolvable cyclone software is optimized for specific energy based on Altera Cyclone II (EP2C5T144) through which we can control the speed of any electronic device or any Motor Control IP product targeted for the fan and pump. Altera Cyclone FPGAs' is a board through which we can monitor the speed and direction of the DC motor. As we know how to make understand, dynamic analog input using an A-to-D convertor and we know how to create pulse width modulation (PWM) output with FPGA. Therefore, by combining these two functions we can create an FPGA DC motor controller. Our paper is divided into three parts: First, all of us will attempt to imitate the issue and can try to look for its answer. Secondly, we will try to verify the solution for real-time. In addition, in the last step, we will verify the solution on the real-time measurements.

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1. INTRODUCTION

Technologies are actively playing its component for individuals to accomplish easiness. Numerous methods have been accustomed to manage the actual pace associated with air conditioning as well as other dc motors within real-time via field programmable gate array (FPGA). The book strategy can be used once the manage formula will be put in place within upon FPGA for that simulation associated with variable-speed drives. The actual specific simulink device can be used to style methods as well as a credit card application instance utilizing a direct-torque-control (DTC) induction motor drive that may be put in place [1]-[5].

The actual manage from the pace from the revolving device can be done along with FPGA because it's very quick as well as simple for the actual altering fill as well as instantly makes up the actual pace since the fluffy strategy keeps growing curiosity in neuro-scientific numerous products. The actual pace could be managed via numerous methods such as the pulse width modulation (PWM) method and so on. As well as

concerning checking as well as managing the actual pace Pc, microcontroller, as well as PLA are now being accustomed to managing the actual pace associated with products [6]-[10]. Execution of the software program component utilizing VHSIC hardware description language (VHDL) about Xilinx FPGA (XC2S30) dependent proportional integral derivative (PID) controller concerning DC motor pace manage program is offered to deal with the actual pace [10]-[16]. Therefore, through maintaining everything within our thoughts, we now have very carefully created this type of program that will help all of us away within managing the actual pace associated with any kind of gadget the Cyclone II FPGA EP2C5T144 is a development board, this board can easily be incorporated into functional applications It is possible to use it for a number of things., it can be used, including data collection, signal processing, basic logic control, mathematical calculations, and many more. The I/O's are routed to the header pins which are used to connect memories, peripherals and other modules that can further be expanded. The actual Altera EP2C5T144C8 Cyclone almost all FPGA possesses an old gadget, however, it continues to be popular and it is effective at a few sophisticated programs since it offers 4068 reasoning components, twenty-six 4k MEMORY obstructs providing an overall total associated with 119, 898 pieces, 13 multipliers, 2 PLLs, as well as 90 I/O's and it has the optimum time clock rate of recurrence associated with three hundred MHz Within our task. We now have installed a good EPCS4 expensive settings storage nick along with a 50 MHz oscillator with this panel [17]-[19].

The actual I/O's tend to be discrete to 4 2x14-method headers, which can be attached to the actual exterior circuits by way of cable jumpers or even PCB installed along with coordinating electrical sockets. Once we possess linked 3 LEDs to PIN 3, 7, as well as 9 along with a push-button, is attached to PIN 144. The actual panel offers 2 10-way headers inside it which include 1 about JTAG and something for that sophisticated serial encoding to that the USB Blaster could be linked. Altera Quartus almost all 11.0 software program has been utilized in pointing FPGA. VHDL, as well as verilog, tend to be 2 equipment explanation 'languages' (HDLs) which are popular about FPGA style. Right now, utilize capacity to the actual panel that will blink energy brought as well as three LEDs might be expensive from 1 Hz. The style may be preserved within the settings expensive storage and it is packed to the FPGA whenever energy comes. Usually, styles tend to be packed straight into the actual FPGA throughout improvement by way of JTAG and therefore are just preserved to settings storage once they will work usually utilizing sophisticated serial encoding. By making use of the ability switch, we can manage the actual pace associated with any kind of gadget. Because the task includes a broad range associated with managing the actual pace associated with any kind of gadget. It may be employed for the actual protection program, transport program, monitoring program, as well as industrialization. This particular document offers within the subsequent since the very first area may be the introduction. Second consists of project design [17]-[22]. The third section is a method, systems equation, and hardware, designs complete with testing, results, conclusion and speed optimization future work for the coming generations. The paper is organized is being as: Section 2 presents the block diagram of project design, section 3 presents the theoretical analysis pf our system design; section 4 discusses the method, section 5 shows of the full system, section 6 discusses the controller along with decoder model; section 7 shows the system simulation outcomes, section 8 discusses the system results. Finally, section 9 shows conclusions.

2. BLOCK DIAGRAM OF PROJECT DESIGN

Beneath may be the prevent diagram in our task that exhibits the entire summary of the DC motor combined with the put in place quests about the FPGA. Since the arranged pace is diverse, respectively, the actual PWM waveform additionally differs. It is noticed how the present pace that is shown about the 7 segment shows equates to the actual arranged pace worth. The actual alter within the pace from the motor for any various changes could be noticed appropriately. In Figure 1, the block diagram consists of the FPGA frame, the DC motor, and the programming is performed in such a way that two signals are sent to the motor drive. One is the signal for speed control; to control the speed, it is a standard pulse with mobilization, and the other is to control the path of the attached unit.

3. THEORETICAL ANALYSIS OF OUR SYSTEM DESIGN

Program modeling for that DC motor as well as bodily action may be talked about with this area, see Figure 2. A typical actuator that can be used within managing the machine may be the DC motor. This, therefore, offers the rotary movement in conjunction with tires and so on. That will supply the translational movement [23]-[25]. Within the determined, the actual electrical signal from the armature and the rotor diagram tend to be proved. Voltage supply that is the actual enter put on the actual motor's armature and the result would be the rotational pace from the base linked (θ/dt). Base and the rotor tend to be thought to

become firm. There is a vicious rubbing design that is ultimately the actual rubbing torque. The actual rubbing torque here is proportional towards the base angular speed. The specific body parameters used appear to be (T) second correlated with rotor inertia, (b) engine viscous friction constant, (Ke) electromotive force constant, (Kt) engine torque constant, (R) electrical resistance, (L) electrical inductance, (T) torque, (i) armature current, (e) back electromotive force, and angular speed.

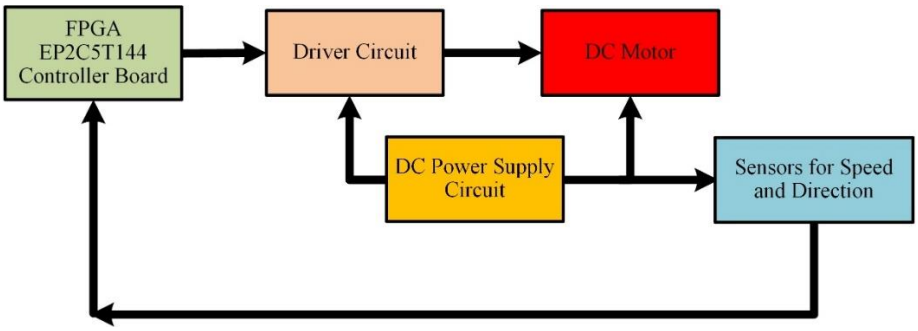


Figure 1. Block diagram of suggested system

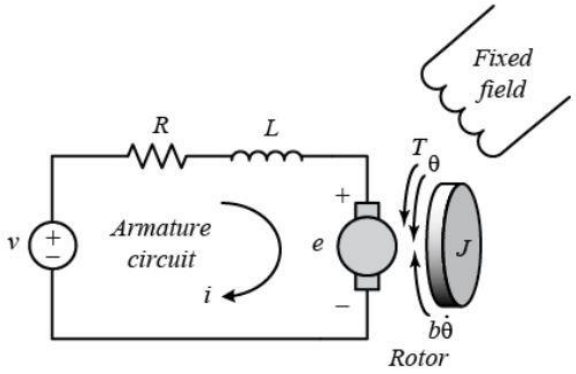


Figure 2. The same signal as well as free of charge entire body DC motor

4. METHOD

Every industry requires some way to control the speed of their machinery. Control techniques applied and presentation of their theories in industries are different because everyone wants to maximize the speed and performance of their equipment [24]. The development of advanced semiconductor technology has boosted the flexibility of speed control. In early times, development growth was very less but after switching towards the software-based simulation and modeling, control speed has been increasing over time. The feedback systems are used to adjust the output and detect the errors accordingly. It allows taking the measuring precautions to maintain the speed of the system.

The FPGA, which is used to produce PWM pulses whose width can be varied using the Cyclone program, preserves the accuracy of the system. PWM pulses are being controlled by the inverter gain generated by the FPGA. The pulses are not quite efficient to drive the MOSFET, so the buffer is used to amplify the signal. Isolation is necessary to separate the power circuit from the control circuit. Based on the needs, the actually arranged pace is actually designated towards the changes and the catch manage change is actually allowed. Arranged worth and also the formerly determined worth associated with pace are going to be studied as well as delivered to the actual PID controller being a mistake as soon as it's produced. Within the suggestions program, the present pace optical sensor, as well as the heartbeat counter-top component, can be used inside it [26]. Following the assessment, the actual PID controller component may determine the same PID worth and can deliver this towards the PWM electrical generator component. It has after that given towards the engine via DAC when the present pace equates to the actually arranged pace, the actual engine will get begin operating at an arranged pace. Once again, through altering the actually arranged pace, the above-mentioned process is actually repetitive through pushing an additional drive switch change within the FPGA component [27]. The FPGA cyclone II EP2C5T144 is presented in the Figure 3.

Figure 3. FPGA cyclone II EP2C5T144

5. EQUATION OF THE FULL SYSTEM

The particular torque created inside the DC motor is going to be proportional to the armature existing along with the usefulness from the real permanent magnet region. Because the permanent magnet region is really constant after which the actual torque produced is going to be proportional to be able to warrant the particular old existing. All of us by having a component constant Kt simply because confirmed inside the method. This species is known as a great armature-controlled motor in (1).

$$Tki - t \tag{1}$$

The trunk emf is proportional for the angular pace in the bottom having a constant component Ke (2).

$$e = Ke\theta \tag{2}$$

To denote both continuous motor torque and also continuous emf back by deciding due to the torque of the motor as well as back again emf constants tend to be identical, that is, Kt = Ke. In 3 as well as 4 appear to be generated according to the second regulation by Newton as well as the voltage regulation by Kirchhoff.

$$J\theta + b\ddot{\theta} \doteq K\imath \tag{3}$$

$$L\frac{di}{dt} + Ri = V - K\dot{\theta} \tag{4}$$

5.1. Transfer function of the system

When it comes to the real dynamic utes Laplace, it can be proposed by using the real change Laplace and over-modeling formula. By applying Laplace transform, we will get (5 and 6).

$$s(Js + b)\theta(s) = KI\ (s) \tag{5}$$

$$(Ls + R)I(s) = V(s) - Ks\theta(s) \tag{6}$$

By eliminating I(s) between the two where the input and rotational velocity of the armature voltage is considered as output.

$$P(s) = \frac{\theta}{v(s)} = \frac{K}{(Js+b)(Ls+R)+K^2}\left[\frac{rad/_s}{v}\right] \tag{7}$$

5.2. State space modeling of the system

Since the condition parameters, the actual formula could be indicated by selecting the actual rotational pace as well as the present (8 and 9).

$$\frac{d}{dt}\begin{bmatrix}\dot{\theta}\\ i\end{bmatrix} = \begin{bmatrix}\frac{-b}{J} & \frac{K}{J}\\ \frac{-K}{L} & \frac{-R}{L}\end{bmatrix}\begin{bmatrix}\dot{\theta}\\ i\end{bmatrix} + \begin{bmatrix}0\\ \frac{1}{L}\end{bmatrix}V \tag{8}$$

$$y = [1\ 0]\frac{\dot{\theta}}{i} \tag{9}$$

5.3. Pulse width modulation (PWM)

PWM of the transmission or even energy supply entails the actual modulation associated with its responsibility period that is accustomed to express the info on the conversation funnel to manage the quantity of energy delivered to a lot [28]. The actual sequence the waveform can be used for that Pulse-width modulation in whose heartbeat thickness is modulated that leads to the actual variance from the typical worth from the waveform as shown in Figure 4. We have considered the square waveform f(t) with a low-value Ymin, duty cycle (D), a High-value Ymax, and the average value of the waveform is given by (10).

$$\bar{y} = \frac{1}{T}\int_0^T f(t)dt \quad (10)$$

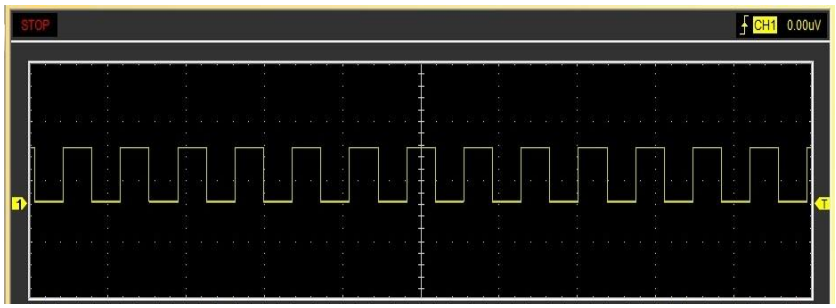


Figure 4. Basic PWM signal with 50% duty cycle

Because f(t) is a square wave, the value of ymax for 0< t < D.T, and ymin for D.T < t < T.

6. CONTROLLER ALONG WITH DECODER MODEL

Usually, there are lots of methods to put into action the design, however, we now have utilized the actual FPGA method of putting into action this. The actual effective method is to apply FPGA like a controller towards the growth. The 2nd choice is by using the actual microcontroller rather than the FPGA [29]. FPGA utilized the reasoning multithreading real-time digesting nick that doesn't possess the function of the built-in peripheral which may be realistically designed.

Furthermore, FPGA is normally made up of logic gates, which means that we can make them run on our call or we can make them do anything and that is the main power of the FPGA. This was the main reason and that is why we have chosen FPGA for our project. This particular can make FPGA a much better appropriate choice concerning real-time software, for example, performing DSP algorithms. It's contingency simply because we can consider sequential performance as an including gentle processor chip primary as the micro-controller is sequential. FPGA can massively handle parallel processing that is why it is now the increasing solution path for the demanding application. FPGA works fairly moderate time clock rates that are calculated inside a couple of countless MHz's; however, they may also carry out the duty from hundreds and hundreds of information for each time clock period whilst working within the reduced tens associated with w selection of energy.

FPGA can offer 50 to 100 occasions the actual overall performance, which is versatile simply because we can include as well as take away the actual performance because needed [30]. This particular can't be carried out through the microcontroller. FPGA is mainly loved simply because it's a hardwired as well as arbitrary assault produced by the actual leader alpha rays can't damage the actual storage places as well as next, the actual time of FPGA dependent improvement is lengthy and may end up being used for that sophisticated advanced chips too. Whilst FPGA is costly than the usual solitary MCU, its performance being an inlayed DSP, storage obstructs, along with a versatile I/O ring might counteract the price of several products.

The full bridge circuit of DC motor is presented in the Figure 5. The key reason for utilizing PWM about generating a DC motor would be to an individual. The actual PWM signal in the motor signal about security reasons and enhance the actual transmission originating from PWM. A digital signal can be used that allows the voltage that will be used throughout a lot within a possible path. This particular signal is usually utilized in robotics along with other programs to permit the DC engine to operate ahead as well as backward placement. It will help to operate the actual motor within a possible path. Should you change the actual DC motor cable connections upon this type of motor compared to its base may turn within the reverse path.

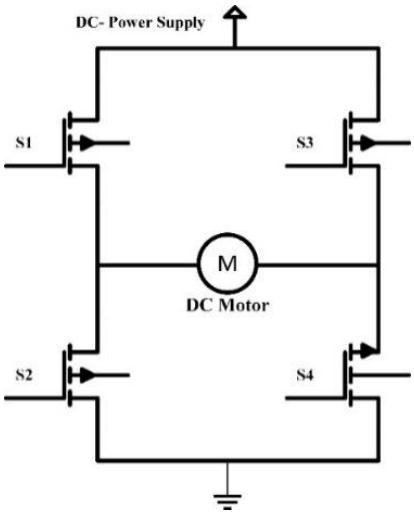


Figure 5. H-Bridge for DC motor

7. SYSTEM SIMULATION OUTCOMES

We now have simulated the task style within 2 various software programs. One of the most significant applications used for the engineering program is the MATLAB/Simulink. Another is Intel Quartus for that FPGA that is a typical software program to complete energy as well as electrical circuit simulation. It's a software program specifically created for engine hard disks as well as energy consumer electronics. It offers a strong simulation concerning energy consumer electronics, analog, and also the electronic manage, motor drives, magnetics, as well as powerful program research.

As we have used Quartus II software for the programming and simulation of our project. Figure 6 present the RTL of simulation circuit diagram and the full VHDL code is presented in the Figure 7. An entire prevent diagram that exhibits the actual fresh program that contains FPGA, a Driver circuit and DC motor. Through pressing the actual drive switch, customers provide instructions as well as responsibility series to FPGA that therefore produce the actual PWM transmission to the driver circuit to enhance the ability to satisfy what's needed. However, because the individual needed, the particular route tranny versions the particular polarity in the producing voltage [30]. When the program begins the actual engine operates indicators. Lastly, FPGA requires both of these indicators to decode as well as display the actual customers concerning the pace as well as the path.

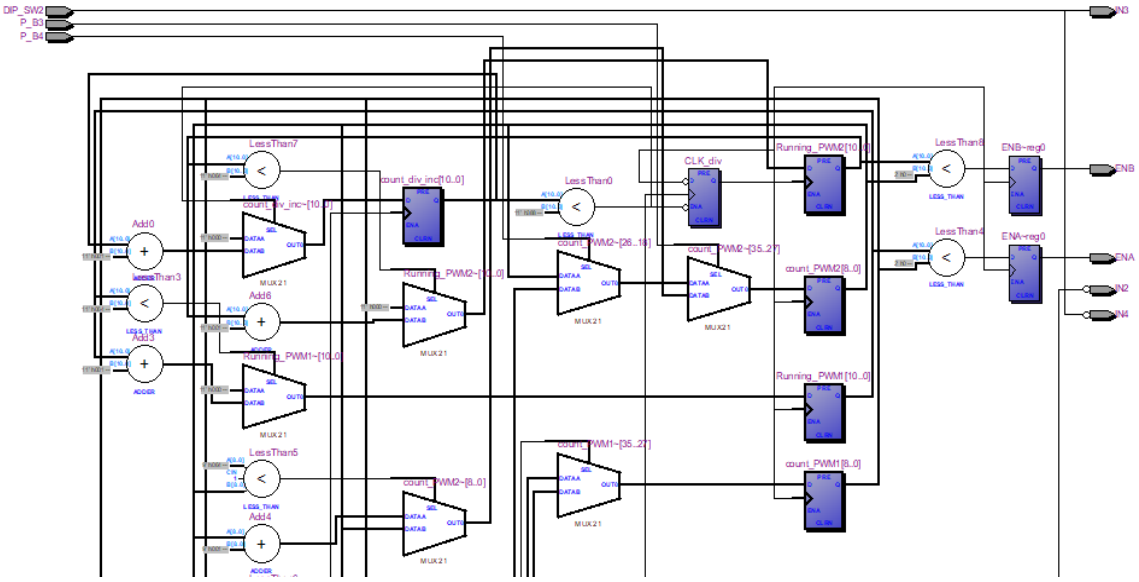
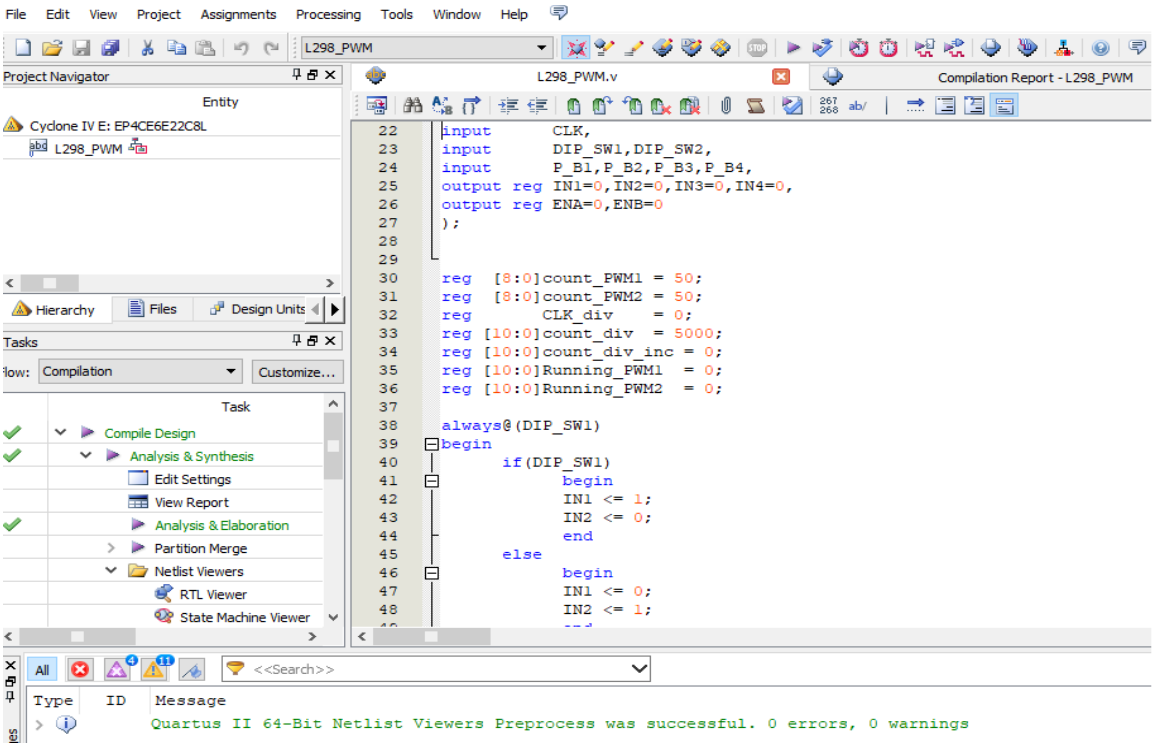


Figure 6. RTL diagram of Feed-forward simulation circuit




```
22  input       CLK,
23  input       DIP_SW1,DIP_SW2,
24  input       P_B1,P_B2,P_B3,P_B4,
25  output reg IN1=0,IN2=0,IN3=0,IN4=0,
26  output reg ENA=0,ENB=0
27  );
28
29
30  reg  [8:0]count_PWM1 = 50;
31  reg  [8:0]count_PWM2 = 50;
32  reg       CLK_div    = 0;
33  reg [10:0]count_div  = 5000;
34  reg [10:0]count_div_inc = 0;
35  reg [10:0]Running_PWM1  = 0;
36  reg [10:0]Running_PWM2  = 0;
37
38  always@(DIP_SW1)
39 begin
40        if(DIP_SW1)
41              begin
42              IN1 <= 1;
43              IN2 <= 0;
44              end
45        else
46              begin
47              IN1 <= 0;
48              IN2 <= 1;
```

Figure 7. Quartus II code window

8. SYSTEM RESULTS

The propsed setup block diagram is presented in the Figure 8. To feel the actual pace from the motor, the drive inside a round type is attached to the actual base from the motor. The pit is drilled over the drive; opto-interrupter gadget can be used using a supply of gentle as well as a detector in the additional finish. Once the drive revolves between your source of light and the detector, after that all of a sudden 1 pulse for each trend is produced. Beneath is the number of pulses produced is actually measured on the particular period and the pace is denoted through the RPM exhibits the actual pace as opposed to sensed pace. Figure 9 present the relation between speed and measuring voltage.

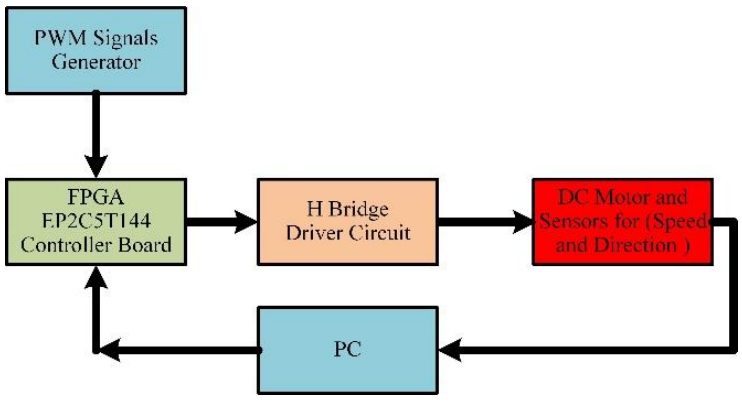


Figure 8. Proposed setup of project

We have designed the generalized digital PID-PWM module in which we can change the parameter accordingly to the desired output. The pulses are produced by the FPGA and the efficiency is measured at different speed conditions after testing the modular drive for different input voltages and currents. The actual pace effectiveness is actually proven for that solitary, 3, 5, 7 as well as 9 pulses for each fifty percent period. It's also noticed how the variance is actually linear as much as the actual pace 1095 rpm after which

effectiveness reduces additionally. It's also observed how the pace raises then your effectiveness additionally obtains raises. The actual PWM method employed for the actual pace manage from the generate and also the change is due to the actual deficits within the equipment as well as changing towards the invertor. The design and the implementation of the FPGA Cyclone II EP2C5T144 with determined software of Quartus are presented in this paper in which we have compared the speed of the devices with FPGA XLR8 and Arduino. The full hardware of the system is presented in the Figure 10.

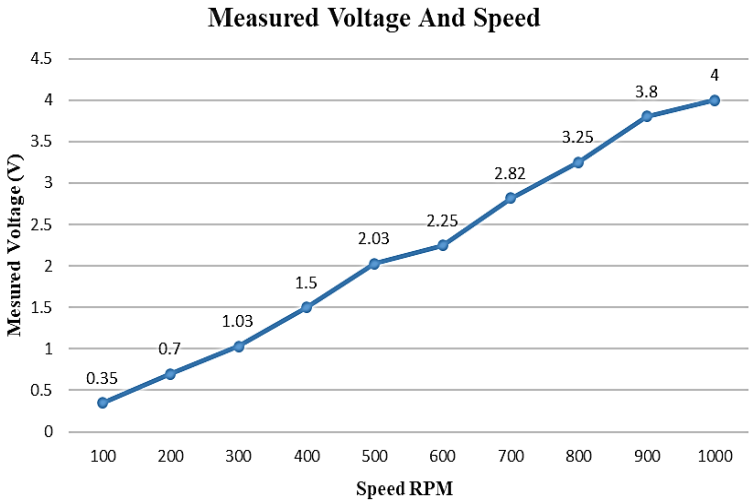


Figure 9. Measurring voltage and sensed speed (RPM)

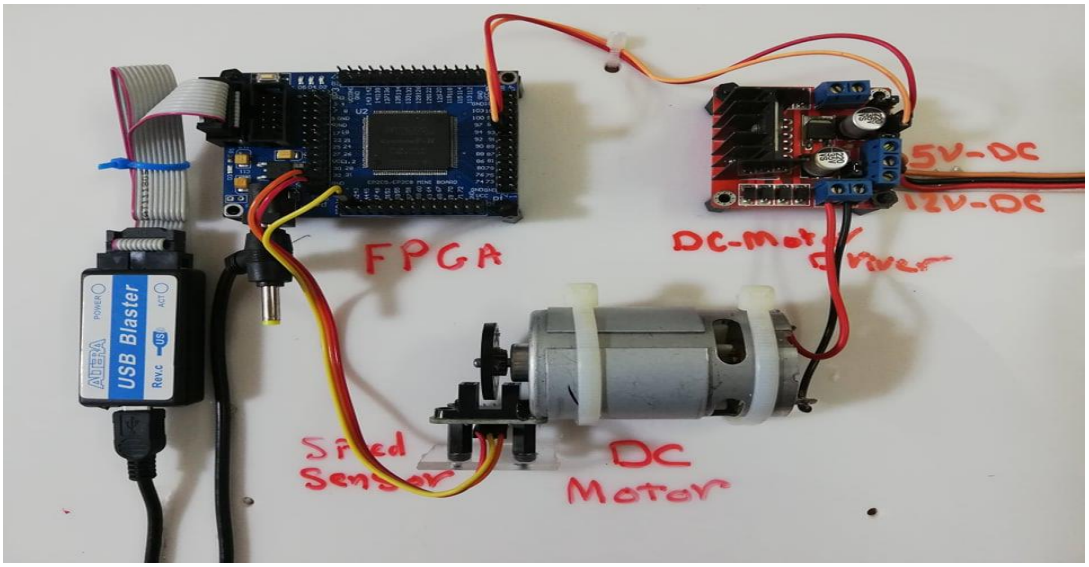


Figure 10. System hardware setup

9. RESULTS AND CONCLUSION

The application of the FPGA structure is very much suitable for high-speed processes. It is the high-speed processor and we can also set the sampling rate and control the speed of the operation. The design for this approach has been tested and found feasible as well. It describes a model that simulates the DC motor controller using FPGA. The fresh outcomes verify the actual powerful design within real-time that exhibits the actual connection between speed as well as each result pace from the engine. The task had been put in place utilizing FPGA and also the resources from the VHDL process of discovering the actual design parameter that is used utilizing easy dimensions as well as regular lab gear.

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