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Electrical characterization of si nanowire GAA-TFET based on dimensions downscaling

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ABSTRACT

This research paper explains the effect of the dimensions of Gate-all-around Si nanowire tunneling field effect transistor (GAA Si-NW TFET) on ON/OFF current ratio, drain induces barrier lowering (DIBL), sub-threshold swing (SS), and threshold voltage (V_T). These parameters are critical factors of the characteristics of tunnel field effect transistors. The Silvaco TCAD has been used to study the electrical characteristics of Si-NW TFET. Output (gate voltage-drain current) characteristics with channel dimensions were simulated. Results show that 50nm long nanowires with 9nm-18nm diameter and 3nm oxide thickness tend to have the best nanowire tunnel field effect transistor (Si-NW TFET) characteristics.

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1. INTRODUCTION

The tunnel field-effect transistor (TFET) is a semiconductors device used to a promising candidate at low power applications in nanometer scales mostly because the conventional metal-oxide-semiconductor field effect transistor (MOSFET) approached the physical and thermal limits. However, the essential physical limitation of MOSFET that is to scale them at the submicron region is the pursuing short channel effects (SCEs) [1]. The silicon nanowire transistor is also used as a candidate device which has the excellent gate controlled and highly influenced electrical behavior to overcome the problems caused by short channel effects [2-5]. In the last decade, the rapid development in shrinking of semiconductors device led to the short channel effects as very harsh problem such as increasing drain induced barrier lowering (DIBL), and many research have been done in the last decade to find the substitutive device structure for striving improvements. Subsequently device structures such as double-gate (DG), surrounding-gate (SG), gate all around (GAA) and carbon nano tube (CNT) FinFETs and graphene-nano-ribbon (GNR) transistors have been incited for resolving the scaling matter of bulk transistors [6-11]. Gate all around-silicon nano wire tunneling FET (GAA-SiNWTFET) has most optimized gate structure than the FinFETs. The key performance for a transistor is the drain current (I_d), drain induced barrier lowering (DIBL), threshold voltage (V_T), sub-threshold slop (SS) and faster switching performance (I_{ON}/I_{OFF}) which is related to the sub-threshold slop when the transistor operate at low voltage [12].

$$SS \cong \left(1 + \frac{C_d}{C_{ox}} ln \frac{KT}{q}\right) \quad (1)$$

Where C_d and C_{ox} are the drain and oxide capacitance, respectively with:

$$ln \frac{KT}{q} = 60\ mV/\ dec \quad (2)$$

The sub-threshold slop (SS) is the voltage applied on the gate to change the drain current by decade [13]. To obtaining a low sub-threshold slop (SS < 60mV /dec) and high switching performance (I_{ON}/I_{OFF} > 10^5) [14], the quantum mechanism in tunneling TFETs has been introduced as a substitution carrier injection mechanism in MOSFETs which suffers from thermal limitation [15-17]. Other advantages of the TFETs are to reduce leakage current, and to provide higher current than the MOSFET, better electrostatic control, prevention of the short channel effects and suitable to fabricate with CMOS processing techniques [18-22]. Therefore the TFETs have been gaining popularity over MOSFETs in the technology nodes [23]. Several excellent article and overview have been done in the last few years ago, which summarize the TFET modern on specific TFET topic [24]. According to aforementioned results that are about characterization and features for TFET, this paper is proposed .Therefore the importance of the work lies in what it shows from investigated characterization for electrical parameters which can be critical factor of TFET.

2. RESEARCH METHOD

The GAA NW Si-TFET is a P-I-N structure with an intrinsic semiconductor part (I) between heavily doped source (p^+) and the drain (n^+). By using band-to-band tunneling FET mechanism, gate all around controls the tunneling between the channel and (source and drain) regions as showed in Figure 1 [25] Figure 2 shows a cross-sectional area of the device. The silicon channel radius is (R) for the gate length (L) which has doping concentration with 10^{16} per cm^{-3}, SiO_2 has been used as a gate oxide dielectric and the constant doping profile has been selected of 10^{20} per cm^{-3} for the both source and drain region. The tunneling process is transfer electron or hole through the junction, this process causes pairs of electrons and holes, hence the transfer rates of electrons and holes are opposite and equal [26]. We used in this work non local band to bestige the tunneling generation rate across a tunneling length and incorporates the change in the electric field along the tunneling length. This model is more accurate for reverse biased tunneling junction with high doping and conservation sub- threshold slop up to 60 mV/ dec.

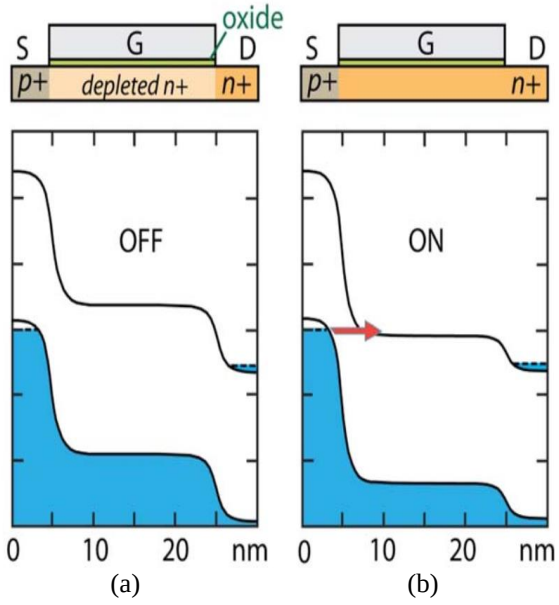

Figure 1. Energy band for a TFET a normally off device. (a) the gate fully depletes the channel, (b) a positive gate voltage turns the channel on [23]

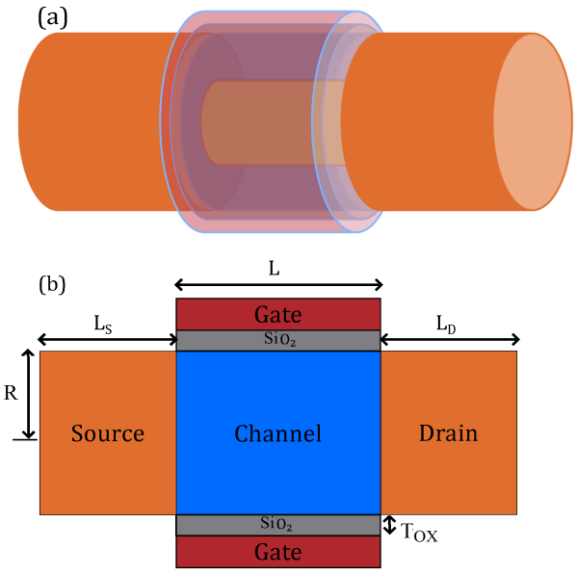

Figure 2. The schematic 3D structure, and (b) the overall dimension of GAA FET

The device has been structured and simulated by using Silvaco TCAD [27] in specified scaling down dimensions within underlying physics with tunneling phenomena proposed by Kane [28]. The designed TFET in this paper, simulate with various dimensions for channel radius (R), channel length (L) and gate oxide thickness (T_{OX}) to study the electrical characterization and analysis importance parameters effects on the device such as DIBL, SS, G_m, V_T and ON/OFF current ratio. The dimensions profile has been selected to be (25, 18, 9, 5) nm for channel radius, (200, 100, 50, 25) nm for channel length and (4, 3, 2, 1) nm for gate oxide thickness. The software can generate useful characteristic GAA TFET curves for researchers, especially to fully explain the underlying physics of TFET.

This simulation tool is utilized to investigate the characteristics of the Si-GAA TFET based on various channel's parameters. The output characteristic curves of the transistor under different conditions and with different parameters are considered. The effects of variable channel dimensions, namely; channel length, width and oxide thickness in addition to scaling factor of the TFET, are determined based on the I–V characteristics that derived from the simulation. In this paper, the I_d–V_g characteristics of transistor at the temperature of 300 K are simulated and evaluated with the simulation parameters for channel lengths, channel diameters, and channel oxide thicknesses have been listed in Table 1.

Table 1. Simulation parameters

Simulation type	Variable Parameters		Constant Parameters	
Channel length effect	Channel length (L)	(25, 50, 100, and 200) nm	Channel radius (R)	(5) nm
			Oxide thickness (T_{OX})	(1) nm
			Channel Doping (P)	10^{16} cm^{-3}
			Drain Doping (P^+)	10^{20} cm^{-3}
			Source Doping (N^+)	10^{20} cm^{-3}
			Drain length	80 nm
			Source length	80nm
Channel radius effect	Channel radius (R)	(5, 9, 18, and 25) nm	Channel length (L)	(200) nm
			Oxide thickness (T_{OX})	(1) nm
			Channel Doping (P)	10^{16} cm^{-3}
			Drain Doping (P^+)	10^{20} cm^{-3}
			Source Doping (N^+)	10^{20} cm^{-3}
			Drain length	80 nm
			Source length	80nm
Channel Oxide thickness effect	Oxide thickness (T_{OX})	(1, 2, 3, and 4) nm	Channel length (L)	(200) nm
			Channel radius (R)	(5) nm
			Channel Doping (P)	10^{16} cm^{-3}
			Drain Doping (P^+)	10^{20} cm^{-3}
			Source Doping (N^+)	10^{20} cm^{-3}
			Drain length	80 nm
			Source length	80nm

Three simulation steps were conducted to evaluate the dimensions dependent performance of TFET in terms of the considered metrics. In the first step, channel length has been varied, whereas other channel dimensions (R and T_{ox}) were kept with constant values. In the second step, the effect of changing channel diameter has been investigated with both channel length and oxide thickness of channel was kept constant. In the final step, oxide thickness was varied and length and radius of channel were fixed.

3. RESULTS AND DISCUSSIONS

In this section, the results of dimensional effect on the electrical characteristics presented and discussed. Downscaling of length of channel (L), radios of nanowire of channel (R), and oxide thickness (T_{OX}) and its effect on the I_{ON}/I_{OFF} ratio, sub-threshuld swing (SS), drain indused barrier lowering (DIBL), treshuld voltage (V_T), and transconductance (G_m) of channel have been studied.

3.1. Downscaling channel length

The result of the effect of scaling down of channel length (L) on the electrical characteristics of GAA NW-TFET has been investigated, the channel length L has been scaled down from 200nm to 25nm, whereas oxide thickness and radius were kept constant at 1 nm and 5 nm, respectively. Also, the drain voltage for transfer characteristics has been chosen to be V_{DD} = 1 V. The simulation of transfer characteristics (drain current I_d–gate voltage V_g) has been conducted with different values of channel lengths L, where L=25, 50, 100, 200nm.

Based on the obtained results that illustrated in Figure 3, the I_{ON}/I_{OFF} ratio exponentially increases with the channel length less than 100 nm, while, for channel length above 100nm the I_{ON}/I_{OFF} were almost constant. As shown in Figure 3, the maximum value of the I_{ON}/I_{OFF} ratio is more than $3.2*10^3$ at L ≥ 100 nm. Figure 4 shows the relation of SS and DIBL characteristic with channel length, this figure explain that the SS improved and decreased as the channel length increased up to 50nm and reached 72.6 mV/dec, while, for L ≥ 50nm, the values of SS were almost constant. For DIBL, the results in Figure 4 shows that the DIBL decreases with increasing channel length up to 100nm, then the values of DIBL were almost constant at 106 mV/V.

Figure 5 shows the relation of length of gate with transconductance (G_m) and threshold voltage (V_T), both V_T and Gm increased linearly with L up to L=50nm, then both (G_m and V_T) almost constant for L ≥ 50nm. According these results the best and minimal Lg must be about 50 nm that has best DIBL, Gm and V_T with acceptable I_{ON}/I_{OFF}.

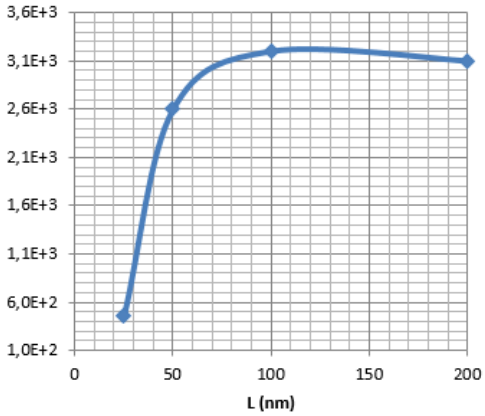

Figure 3. Characteristics of I_{ON}/I_{OFF} ratio with L

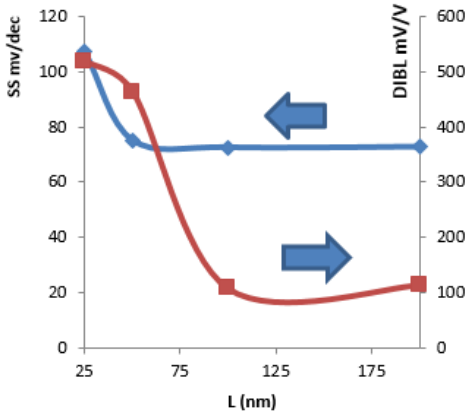

Figure 4. The characterestics of SS and DIBL with channel length

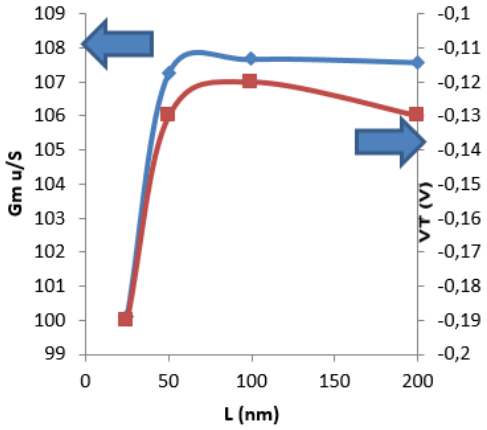

Figure 5. The length of gate effect on transconductance (G_m) and threshold voltage (V_T)

3.2. Downscaling channel radius

The minimizing of channel radius R and its effect on the electrical characteristics of GAA TFET have been investigated in this section. The value of R was changed (5, 9, 18 and 25 nm) while L=200nm and T_{OX} = 15 nm. Figure 6 shows the electrical characteristics of I_{ON}/I_{OFF} ratio depending on the effect of changing channel radius R. The I_{ON}/I_{OFF} ratio for both voltages (V_D = 1 V and V_G = 1.5 V). The I_{ON}/I_{OFF} ratio is increasing proportional with increasing channel radius. It is possible to recognize that at R lower than 10nm there are highly increasing in I_{ON}/I_{OFF} ratios, while at R higher than 10nm there are lower increasing in I_{ON}/I_{OFF} ratios. So, if the channel dimeter minimize from 25nm to 10nm, the I_{ON}/I_{OFF} ratios with decreased

from 3.9 *10^5 to 7*10^4 respectively. While, the minimizing the channel radius from 10nm to 5nm will drop down the I_{ON}/I_{OFF} ratios from 7*10^4 to 3.2*10^3 respectively.

Figure 7 depicts the variation of SS and DIBL values with variable channel radius. The SS highly improved and increased from 72.8 to 57.5 mV/dec when the radius changed from 5 to 10nm respectively, the SS increased slightly to 50 mV/dec when the radius increased to 25nm. Figure 7 illustrate that the BIDL behavior look like same as SS, the DIBL improved and dropped highly also from 116 to 60 mV/V with radius from 5 to 10 nm respectively, and dropped slightly from 60 to 38 mV/V with the range of channel radius 10 to 25nm.

Furthermore, the impacts of varying channel radius on V_T and G_m are illustrated in Figure 8. The threshold voltage is almost constant regardless channel width except at the R = 10 nm, where V_T scores the highest value of 0.13 V. Finally, the G_m increased as channel radius increased. GGA TFET achieved higher G_m at D = 25 nm, the G_m characteristics increased with decreasing R and achieved the lower value at D = 5 nm. According these results the minimal R with good electrical characteristics must be about 10 nm that has best DIBL, Gm and V_T with acceptable I_{ON}/I_{OFF}.

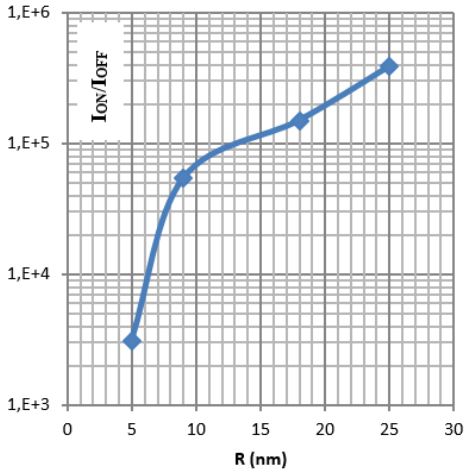

Figure 6. Characteristics of I_{ON}/I_{OFF} ratio with R

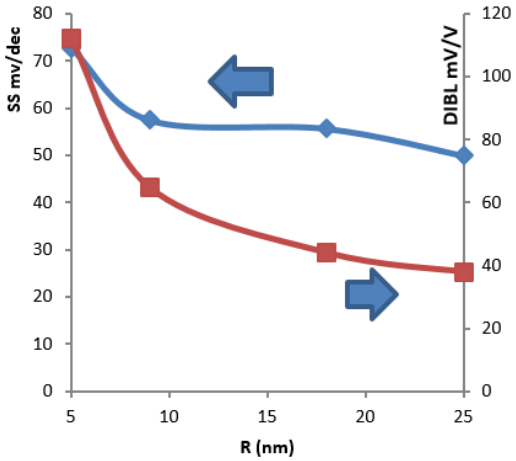

Figure 7. The variation of SS and DIBL with R

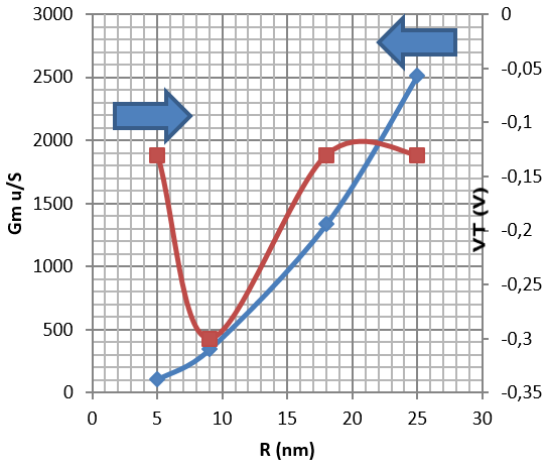

Figure 8. Characteristics of V_T and G_m with R

3.3. Downscaling channel oxide thickness

Figures 9 to 11 show the channel oxide thickness variation in relation to the electrical characteristics of GAA TFET. For this simulation step, T_{OX} has been varied (1, 2, 3 and 4 nm), the channel length and channel radius has been kept constant at 200 nm and 5nm respectively. Figure 9 illustrates the relation

between the I_{ON}/I_{OFF} ratio with the channel oxide thickness. The minimum I_{ON}/I_{OFF} ratio ($3.1*10^3$) with V_{DD} = 1 V was obtained at minimum T_{OX} = 1 nm and then increased to $2.5*10^{13}$ at T_{OX} = 4 nm. From the results shown in Figure 10, it is clear that for a lower channel oxide thickness, T_{OX} = 1 nm the TFET has shown worse SS characteristics with the best SS value of 72.8 mV/dec compared to other T_{OX} values. The SS improved with increasing T_{OX} and the best value (21.4 mV/V) was at T_{OX} = 3nm. Figure 10 also displays channel oxide thickness versus DIBL characteristics of TFET. DIBL increased linearly with increasing T_{OX}, the best value at T_{OX} =1nm. Figure 11 represents the relation of both V_T and G_m, G_m has a peak value at 2nm while V_T increased with increasing Tox and its value almost constant after T_{OX} =1nm. According these results the minimal T_{OX} with good electrical characteristics must be 2 nm that has best DIBL, Gm and V_T with acceptable I_{ON}/I_{OFF}.

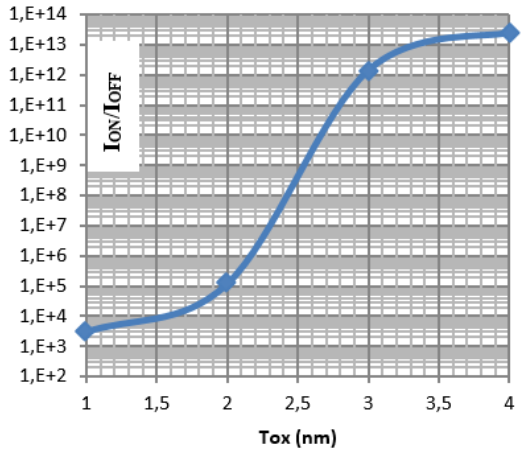

Figure 9. Characteristics of I_{ON}/I_{OFF} ratio with T_{OX}

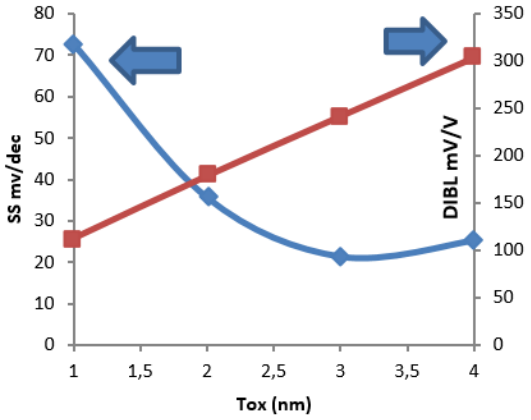

Figure 10. The characterestics of SS and DIBL with T_{OX}

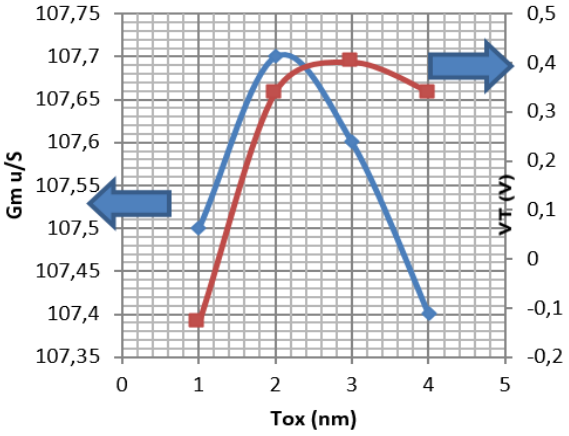

Figure 11. Characteristics of V_T and G_m with T_{OX}

4. CONCLUSION

The downscaling effect on the electrical characteristics of GAA Si-NW TFET has been investigated, TCAD simulation tool has been used to create the output characteristics of TFET and the critical parameters related to the electrical characteristics transistor. Downscaling of length of channel (L), radios of nanowire of channel (R), and oxide thickness (T_{OX}) and its effect on the I_{ON}/I_{OFF} ratio, sub-threshuld swing (SS), drain indused barrier lowering (DIBL), treshuld voltage (V_T), and transconductance (G_m) of channel have been studied. The results shows that the minimal channel length with good electrical characteristics was at 50nm, the minimal channel redius with good electrical characteristics was at 10nm, and finally, the minimal channel oxide thickness with good electrical characteristics was at range 2 to 3nm.

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