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Hybrid memristor-CMOS implementation of logic gates design using LTSpice

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ABSTRACT

In this paper, a hybrid memristor-CMOS implementation of logic gates simulated using LTSpice. Memristors' implementation in computer architecture designs explored in various design structures proposed by researchers from all around the world. However, all prior designs have some drawbacks in terms of applicability, scalability, and performance. In this research, logic gates design based on the hybrid memristor-CMOS structure presented. 2-inputs AND, OR, NAND, NOR, XOR, and XNOR are demonstrated with minimum components requirements. In addition, a 1-bit full adder circuit with high performance and low area consumption is also proposed. The proposed full adder only consists of 4 memristors and 7 CMOS transistors. Half design of the adder base on the memristor component created. Through analysis and simulations, the memristor implementation on designing logic gates using memristor-CMOS structure demonstrated using the generalized metastable switch memristor (MSS) model and LTSpice. In conclusion, the proposed approach improves speed and require less area.

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1. INTRODUCTION

Memristors have made a huge breakthrough in computer architecture designs because of its non-volatility behavior. A lot of researches had reported their outcome even though is not commercially available [1-4]. Much evidence proved that using analog-based circuit operation will results in much faster data processing compared to current digital-based operation. It can remember its past value even when the power supply disconnected or turned off. Its resistance depends on the history of the applied inputs: Voltage or current. Moreover, it is predicted that memristors will be the key to designing analog-based data processing as shown in (1) and (2).

$$V_{out,AND} = \frac{R_{on}}{R_{on} + R_{off}} V_{high} \cong 0 \quad (1)$$

$$V_{out,OR} = \frac{R_{off}}{R_{off} + R_{on}} V_{high} \cong V_{high} \quad (2)$$

Therefore, hybrid CMOS circuits were proposed by many researchers for performance improvement [5-11]. The combination with memory characteristics of the memristors creates a unique opportunity for the next generation computers in which memory and logic devices blended to avoid a data bandwidth limitation between processing units and the memory [12, 13]. Simulating the developed model of memristor was the best way to monitor the electrical properties as compared with the CMOS properties [14-18].

In this paper, a Hybrid CMOS-memristor for Half-Adder is implemented using LT-SPICE. The implementation started with the simulation of the AND and XOR logic gate. This to make sure that every hybrid component is working. Then, the comparison in terms of area and delay consumption for the proposed full adder are collected. Compared with previous works, this approach presents considerably less delay and area.

2. METHODOLOGY

The design phase can be divided into several stages. The initial stage focuses on designing the static CMOS logic gates such as AND, XOR, and Full Adder. The second stage is to implement the memristor equivalent circuits for the AND, XOR and Full Adder. The circuits are built as per circuit diagrams. All of the requirements and limitations are considered. Moreover, all of the gates are simulated in LT Spice. The output waveforms are analyzed and verified working as per expectation. All of the results are compared with previous researches.

2.1. Implementation of memristor AND logic gate and XOR logic gate

Figure 1 shows an AND gate using memristor the resistor after the input has been replaced with memristor to see how it work. As for R1 is using resistor because the memristor input cannot come from other memristor output, the output that will produced is unpredictable. The output status of a digital logic AND gate returns "LOW" only when any of its inputs are at a "0" level of logic. In other words, each LOW input will give a LOW output for a logic AND gate.

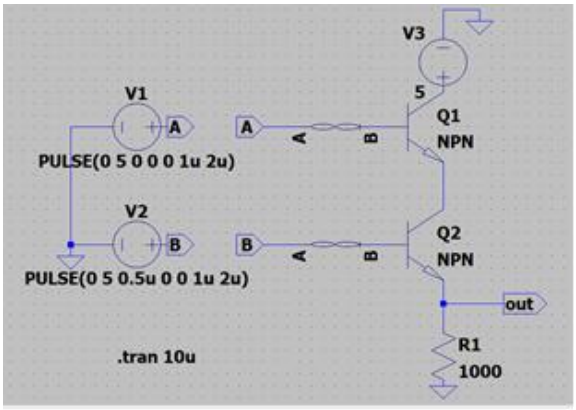

Figure 1. AND gate memristor

The logic AND Boolean expression for a digital logic AND gate is given as A.B = **Q**. The operation of a digital 2-input logic AND gate can then be defined as: "If both A and B are valid, then Q is true". Exclusive-OR gate feature is accomplished by integrating regular logic gates to produce more complicated gate functions that are commonly used in the creation of arithmetic logic circuits, computational logic comparators, and error detection circuits. The "Exclusive-OR" two-input gate is a two-adder module, providing the sum of two binary numbers, rendering it more complicated in nature than other basic logic gate forms.

2.2. Memristor full adder logic gate

Using previous designs of AND, OR, and XOR, a hybrid memristor-CMOS full adder constructed using 4 memristors and 7 CMOS transistors. In this proposed full adder, the Sum bit circuit and Carry out bit separated from each other for silmulation purposes using LT-Spice as shown in Figure 2. An AND gate memristor used to produce a carry output, while the XOR gate using memristor to produce sum output. The full adder is used to add two single-digit binary numbers which contribute to a two-digit production.

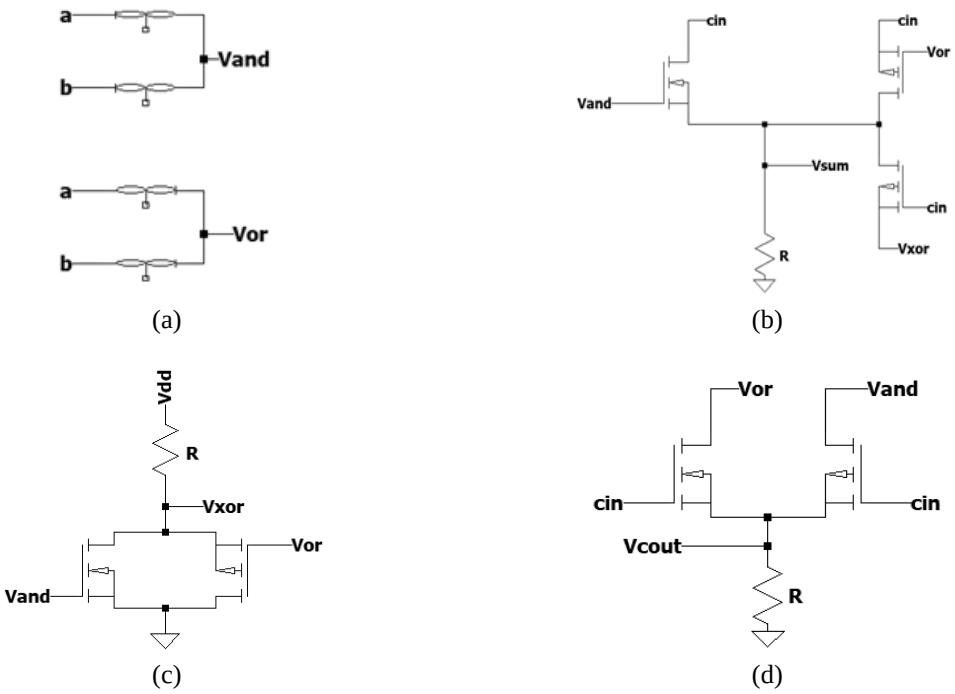

Figure 2. Full adder with separated element. (a) AND and OR circuit, (b) XOR circuit, (c) sum bit circuit, (d) Carry out bit circuit, R=10 k Ω, Vdd=5 V

3. RESULTS AND DISCUSSION

All of the simulations in this work are done using the generalized metastable switch memristor (MSS) model proposed by Knowm Inc. [19]. The MSS model is capable of modeling the memristor's hysteresis behavior precisely and is suitable for RRAM technology. This model was introduced by Knowm referring to the previously proposed model by Biolek [20] and VTEAM [21]. The parameters are set as follows; R_{on}=500 Ω, R_{off}=150k Ω, V_{on}=2.5 V, V_{off}=2.5 V. The current-voltage relationship of this memristor is shown in Figure 3. The software used for these simulations is LTSpice XVII, a free high-performance SPICE simulation software for Windows. The resistor used for all of the voltage reading purposes is 10k Ω. The simulation results for one MSS memristor model are shown in Figures 3 and 4. According to the hysteresis loop of this memristor model, it is visible that it follows the parameters set earlier with both V_{on} and V_{off} are equal to 2.5 V.

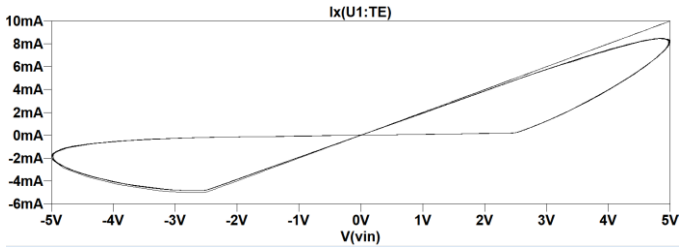

Figure 3. Hyteresis loop simulation

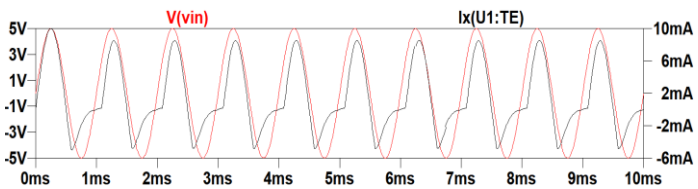

Figure 4. MSS model simulation

3.1. Memristor-CMOS XOR design

A high-performance CMOS XOR logic gate design obtained using AND gate that is connected to a single NMOS and OR gate that is connected to a single PMOS. This design can be implemented using four memristors combined with two CMOS as a switch as shown in Figure 5. The basic operation of an XOR logic gate is to output zero voltage if the two applied inputs are equal. Figures 6 and 7 show the operation of this different input XOR. When the two inputs are both high, the AND circuit will output high and provide the voltage to the NMOS which operates on high voltage. When NMOS conduct, PMOS does not conduct and the output voltage is equal to zero. Correspondingly, when inputs applied are both low, the OR gate will output low and provide voltage to the PMOS which operates on low voltage. When the PMOS conduct, NMOS does not conduct and the output voltage is equal to zero. The simulation waveforms for the XOR circuit shown in Figure 8.

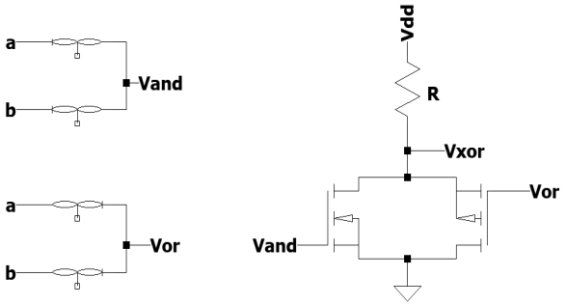

Figure 5. Schematic of memristor-CMOS XOR2 circuit, R=10k Ω, Vdd=5 V

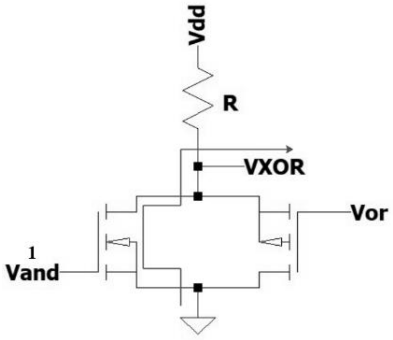

Figure 6. The state when both inputs are 1

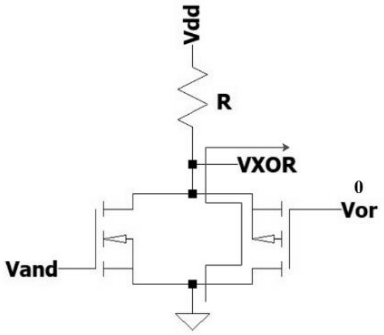

Figure 7. The state when both inputs are 0

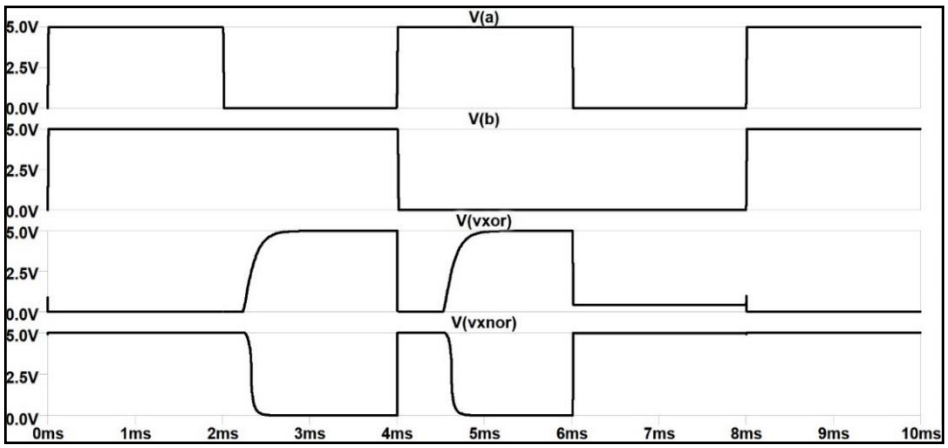

Figure 8. Simulation waveforms of XOR and XNOR logic gates shown in Figures 7 and 8

The input voltages are represented by V(a) and V(b). The XNOR gate is achieved using additional CMOS inverter. The waveform is tabulated in Table 1 with logic 1 is 5 V and logic 0 is 0 V. The presented XOR and XNOR have simple topology and fewer components that constructed with 4 memristors and 2 CMOS transistors, another additional 2 CMOS transistors are required as an inverter for XNOR circuit. This topology reduces CMOS usage and hence leads to lower area and power consumption

Table 1. Tabulated data of somulation waveforms in Figure 9

Time(ms)	Input		Output	
	V(a)	V(b)	V(xor)	V(xnor)
0 - 2	1	1	0	1
2 - 4	0	1	1	0
4 - 6	1	0	1	0
6 - 8	0	0	0	1

3.2. Memristor-CMOS full adder design

The presented Sum bit circuit is made up of 3 CMOS transistors and output from the AND, OR and XOR circuit. The operation of the Sum bit circuit shown in Figure 9. The Sum bit is equal to high when the inputs (Cin.B.A) are equal to 001, 010, 100, and 111. Meanwhile, the presented Carry out circuit is consists of 2 CMOS transistors and output from the AND and OR circuit. The operation of this Carry out circuit explained in Figure 10 where Carry out bit is equal to high when the inputs (Cin.B.A) are equal to 011, 101, 110, and 111. The operation of this circuit shown in Figure 11. The operation of this full adder circuit shown in the simulation results shown in Figure 11.

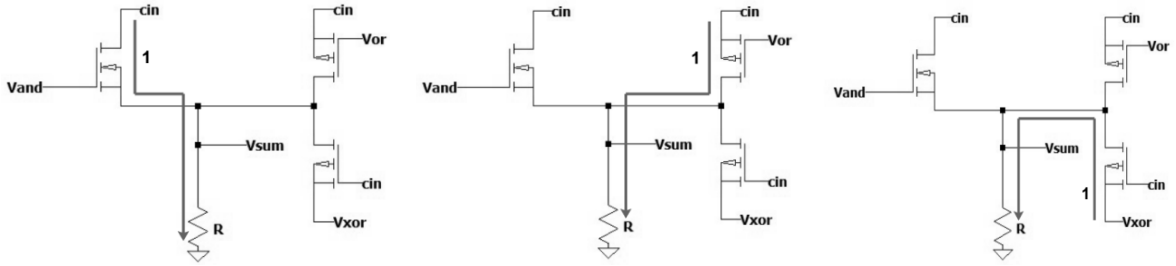

Figure 9. The path when the sum bit is high (1), (a) Cin.B.A (111), (b) Cin.B.A (100), (c) Cin.B.A (001, 010), the current flows is shown by the line with R=10k Ω

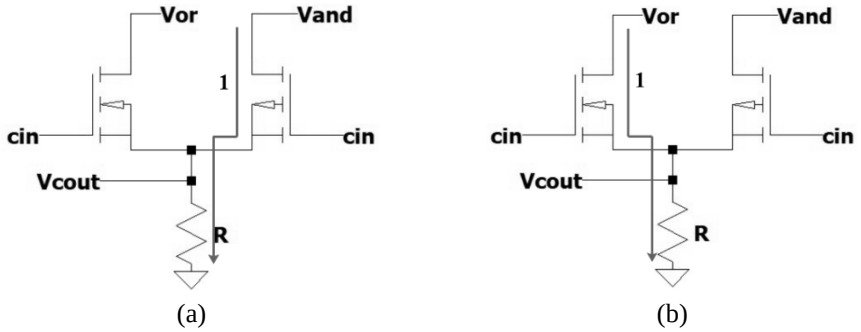

Figure 10. The path when the carry out bit is high (1), (a) Cin.B.A (011), (b) Cin.B.A (101, 110, 111), the current flows is as shown by the line with resistor R is equal to 10k Ω

Table 2 explains the tabulated data simulation waveforms of full adder from Figure 11. There are 8 different intervals to show 3-bit input from '000' to '111'. The output V(sum) and V(cout) shows the output from the designed hybrid memristor-CMOS meets same as the normal Full Adder.

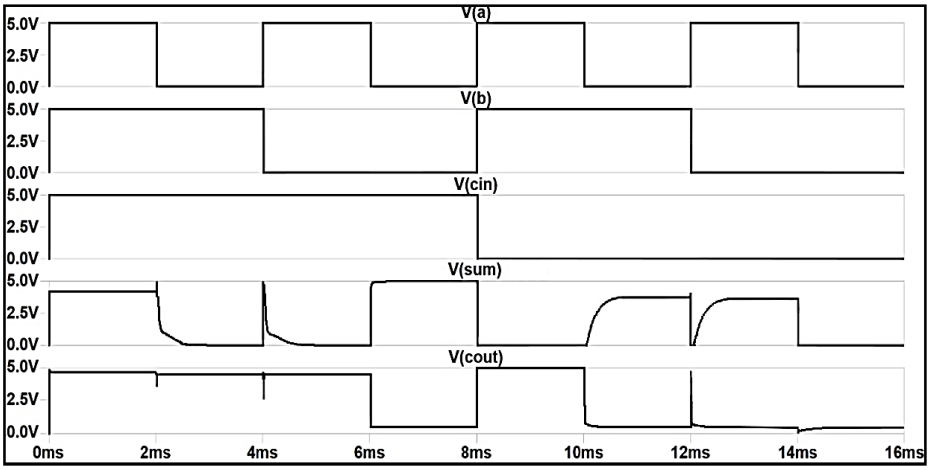

Figure 11. The simulation results of the full adder circuit in Figure 12, the input voltages are represented by V(a), V(b) and V(cin), in the simulation, logic 1 is 5 V and logic 0 is 0 V

Table 2. Tabulated data of simulation waveforms in Figure 11

Time(ms)	Input			Output	
	V(a)	V(b)	V(cin)	V(sum)	V(cout)
0 - 2	1	1	1	1	1
2 - 4	0	1	1	0	1
4 - 6	1	0	1	0	1
6 - 8	0	0	1	1	0
8 - 10	1	1	0	0	1
10 - 12	0	1	0	1	0
12 - 14	1	0	0	1	0
14 - 16	0	0	0	0	0

By combining the circuit of Sum bit and Carry out bit together, the complete full adder circuit is made up of 7 CMOS transistors and 4 memristors. This proposed full adder circuit has fewer components compared with other structures and with fewer components, it leads to less delay, less power, and less area consumption and hence, a high-performance full adder circuit was proposed.

3.3. Comparison and discussion

A summary and comparison in terms of area and delay consumption for the proposed full adder are shown in Table 3. The comparison is done with other memristors based design structures for basic logics and Full Adders. In terms of delay, this proposed full adder structure has a lower delay compared to MAGIC, IMPLY, and CRS with 4N delay. However, it is slower than the MRL and MAD structure. Meanwhile, in terms of area, this proposed structure has the smallest area consumption with only 14 components in total. With a smaller area, the power consumed by this structure is bounded to be low and efficient.

Table 3. Area and delay comparison of different Full Adders

	Delay	CMOS	Memristor	Resistor
Proposed	4	7	4	3
CRS [22]	14	0	16	1
MPLY [23]	19	0	28	5
Improved IMPLY [24]	10	0	9	1
MAGIC [25]	16	0	28	0
MRL [26]	1	8	18	0
MAD [27]	2	14	8	9

4. CONCLUSION

Memristor has recently risen in popularity for its capability and potential to revamp the development of computer architecture in terms of power, area, and efficiency. However, more researches are still needed to fully utilize this missing circuit fundamental in terms of its possibility in replacing or accommodate current CMOS technology in both logic and memory applications. In this work, logic gates design based on the

hybrid memristor-CMOS structure is demonstrated and analyzed. 2-inputs AND and OR gate is presented using 2 memristors and additional 2 CMOS transistors are required for NAND and NOR gate operation. Not only are that, a simple XOR logic made up of 4 memristors and 2 CMOS transistors also proposed. In addition, a full adder circuit was also proposed with a low delay and smallest area consumption that constructed with a total of 4 memristors and 7 CMOS transistors. In conclusion, logic gates design using hybrid memristor-CMOS structure has been successfully demonstrated and analyzed.

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