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A 5G mm-wave compact voltage-controlled oscillator in 0.25 µm pHEMT technology

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ABSTRACT

A 5G mm-wave monolithic microwave integrated circuit (MMIC) voltage-controlled oscillator (VCO) is presented in this paper. It is designed on GaAs substrate and with 0.25 µm-pHEMT technology from UMS foundry and it is based on pHEMT varactors in order to achieve a very small chip size. A 0dBm-output power over the entire tuning range from 27.67 GHz to 28.91 GHz, a phase noise of -96.274 dBc/Hz and -116.24 dBc/Hz at 1 and 10 MHz offset frequency from the carrier respectively are obtained on simulation. A power consumption of 111 mW is obtained for a chip size of 0.268 mm^2. According to our knowledge, this circuit occupies the smallest surface area compared to pHEMTs oscillators published in the literature.

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1. INTRODUCTION

As any new generation of mobile communication, 5G must offer better performance than previous generations. According to the International Telecommunication Union, 5G is expected to support very high download speeds (until 10 Gbit/s), and an extremely low latency time (about 1 ms) [1]. As the microwave frequency band is, practically, fully occupied, new frequency bands are required to meet the needs of 5G. In the millimeter-wave band, 26 GHz to 2 GHz frequencies are the most recommended by 5G actors [2].

Millimeter-wave frequencies offer huge capacity, allowing more transferred data through a particular channel in order to achieve multi-gigabit rates per second [3] and a very low latency time. Such advantages offer new opportunities for high-speed wireless Internet access, data and video streaming, and cable replacement. In return, it requires a reliable design process, a qualified foundry design kit based on rigorous modelling of passive and active components, and also predictable simulations in time and frequency domains that can handle highly non-linear integrated circuits.

Each communication system integrates local oscillators Figure 1 [4] and its own performance influences the performance of the entire system. Therefore, the design of a VCO for millimeter frequencies presents a great challenge for RF circuit designers [5]. For most VCOs published in the literature, the oscillation frequency tuning is obtained using varactors [6-10]. Due to the high level of varactor Amplitude-to-Phase noise conversion [11], reference [12] presents a frequency tuning technique based on varactor-mounted GaAs pHEMT transistors in order to minimize the noise conversion and to reduce the size of the final circuit and its fabrication costs, too.

In this paper, we follow the approach of [12] using the PH25 process technology from UMS foundry. The circuit studied in this paper presents good performance in terms of phase noise (PN) level, output power and DC power consumption while occupying less than half of the area occupied by the structures proposed in [12-15]. This paper is organized as follows: in section 2, we present the VCO circuit as well as its layout. While the third section is dedicated to the results of post-layout simulation. Then these results are analyzed and compared with others from the literature in section 4. Finally, a conclusion is presented in the last section.

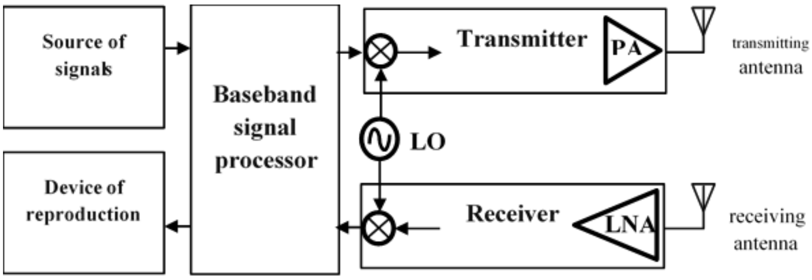


Figure 1. Simplified diagram of the transceiver system

2. VOLTAGE CONTROLLED OSCILLATOR CIRCUIT

The architecture of the proposed VCO is based on the Colpitts structure studied in the references [16-18] and the structure proposed by the authors in [12] as shown in Figure 2. The active part of this oscillator consists of two transistors pHEMT 1 and pHEMT 2: each one has 4 fingers and a gate length and width of 0.25 µm and 20 µm, respectively. A higher number of fingers increases the output power [19]. Each transistor is biased at the operation point (VDS=2.2 V, VGS -0.6 V) and the three inductors Ld1, Ld2 and Lg equals respectively to 0.15 nH, 0.15 nH and 0.1 nH. The performance of the circuit strongly depends on the bias conditions [20], for this reason the values of the bias voltages and inductors are chosen carefully. The resonant circuit of the VCO is based on two source-drain shorted transistors pHEMT 3 and pHEMT 4. Consequently, these two transistors act like varactors whose capacitance value is tuned by the voltage source Vtune applied to their gates.

The VCO circuit is based on passive components and pHEMT transistors of the PH25 process (United Monolithic Semiconductors foundry). The passive and active devices models fit well their performances, and they integrate parasitic behaviors. Therefore, in order to obtain the layout presented in Figure 3, a number of optimization and retro-simulation steps are required. In order to minimize any kind of asymmetry in the generated waveforms, and to avoid the introduction of additional noise, special attention has been focused on the layout symmetry [21].

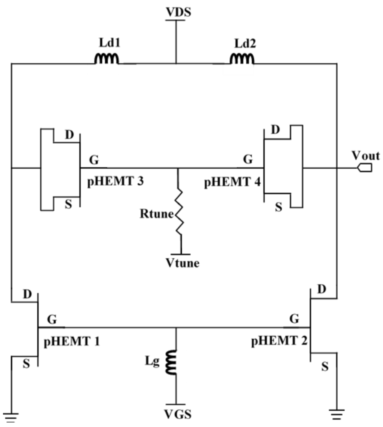


Figure 2. Voltage controlled oscillator circuit

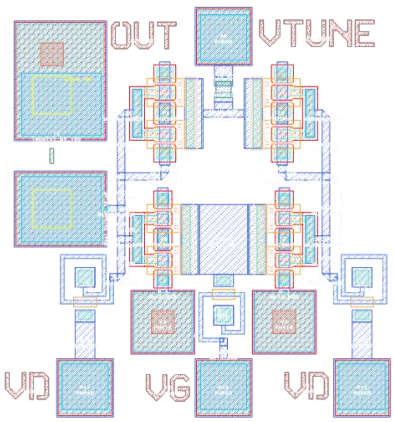


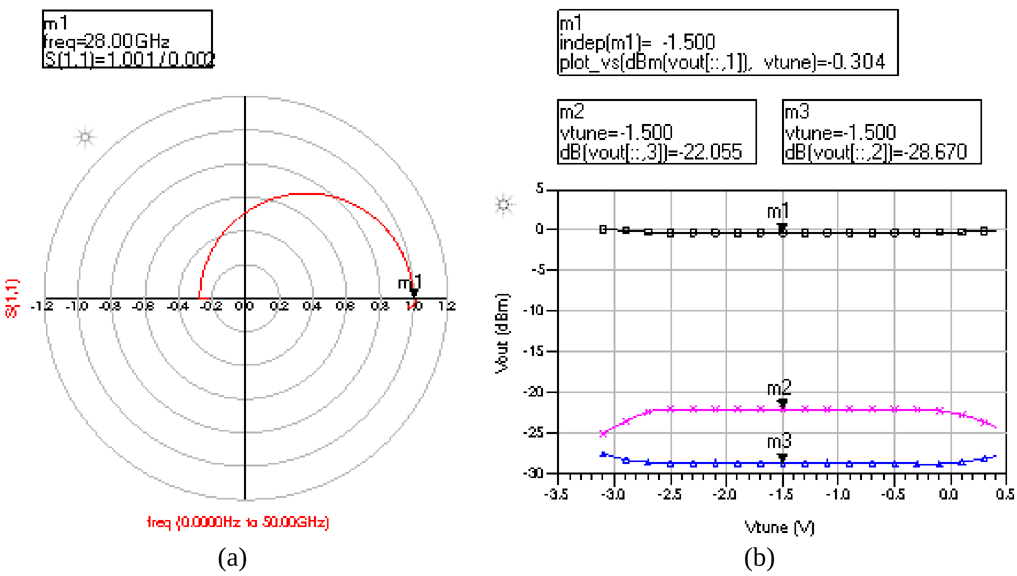
Figure 3. VCO layout

The circuit is implemented on GaAs substrate for a chip size circuit equal to 0.268 mm^2 (540x496 µm). The chip includes the oscillator circuit, RF access pad and three bias pads. While the chip size of the circuits presented in [8, 12, 15] are 3.75 mm^2, 0.515 mm^2 and 0.5 mm^2 respectively. It is therefore a compact and reduced structure, compared to the structures published, recently, in the literature.

3. POST-LAYOUT SIMULATION

In order to ensure that the designed circuit will operate as expected, it is essential to carry out post-layout simulations that consider all the parasitics and undesirable effects related to the additional interconnection lines and parasitic aspects of the passive and active elements. For designing and optimizing an oscillator, the first step is to verify the oscillation stability of the circuit. The oscillator converges if the two Barkhausen conditions are satisfied, i.e., at the oscillation frequency, the loop gain is greater or equal to 1 and the phase is near zero [22, 23]. This can be easily verified by using the "OscTest" tool available in the ADS simulator. As we can observe in Figure 4 (a), at frequencies around 28 GHz, the reflexion coefficient magnitude is 1.001 and its phase is 0.002° on small signal simulation, therefore the Barkhausen conditions are well verified.

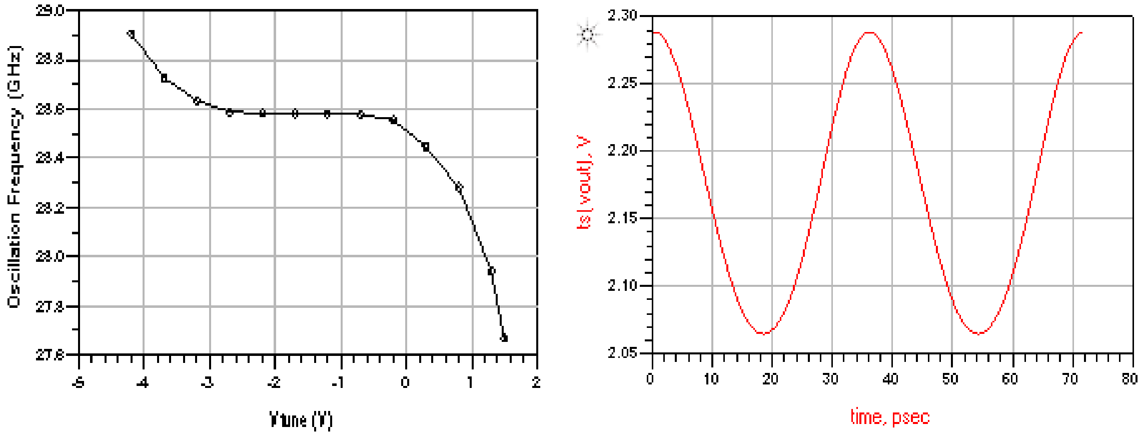
Large signal simulation with harmonic balance shows the power spectrum of the output signal Vout Figure 4(b), we can clearly see that the fundamental power is around 0 dBm, it is constant over the entire voltage tuning range of the VCO. The output powers of the first and second harmonics are -28.67 dBm and -2.05 dBm respectively, corresponding to 28dB rejection of the first harmonic and 22 dB rejection of the second harmonic. The oscillation frequency varies between 27.67 GHz and 28.91 GHz when varying the gate pHEMT1 and pHEMT2 voltages from 1.5 V to -4.1 V Figure 5 (a). Consequently, the circuit has a frequency tuning range of 1.24 GHz, corresponding to a frequency sensitivity of 221.4 MHz/V. Figure 5 (b) shows the time domain of the output signal Vout, the signal shape is clearly sinusoidal (for Vtune=1.3 V). The phase noise simulation, presented in Figure 6, shows that phase noise are -96.274 dBc/Hz and -116.27 dBc/Hz at offset frequency 1 MHz and 10 MHz from the carrier, respectively.



(a) (b)

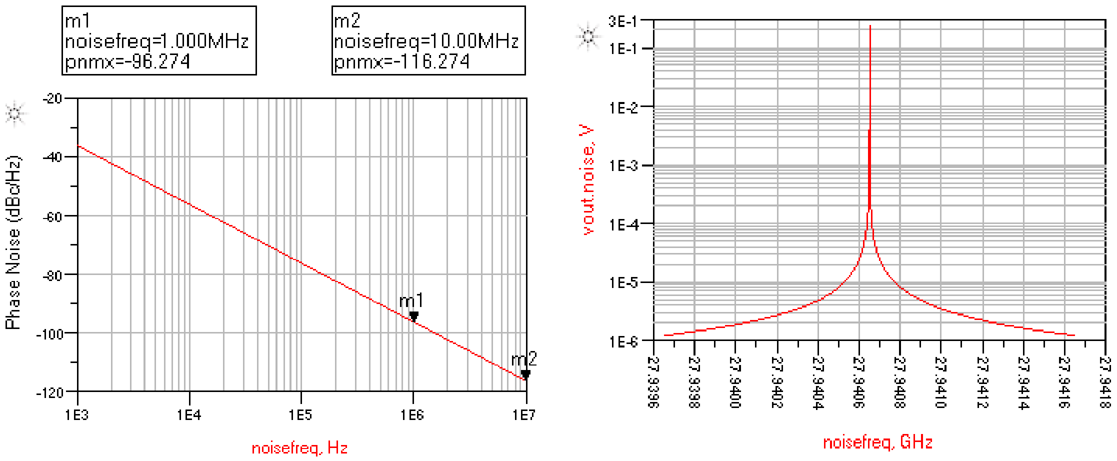
Figure 4. (a) Loop gain and, (b) power of the fondamental (-□-), first (-Δ-) and second (-x-) harmonic versus Vtune

Nowdays, the energy consumption is an important consideration for wireless communication systems such as 5G [24]. The DC simulation indicates that the power consumption of our VCO circuit is very low, with a power of 111 mW maximum. Finally, to study the impact of the technology dispersion on the performance of the circuit proposed in this paper, we performed for a statistical "MONTE CARLO" analysis. Is shown in Figure 7 that for small variations of the circuit parameters, the output power varies slightly by a few decibels. In the worst case, the output power, of the fundamental harmonic, decreases to -3 dBm while the rejection of the first and second harmonics remains higher than 21 dB and 16 dB respectively along the VCO frequency bandwidth and for the fifty iterations of the "MONTE CARLO" simulation.



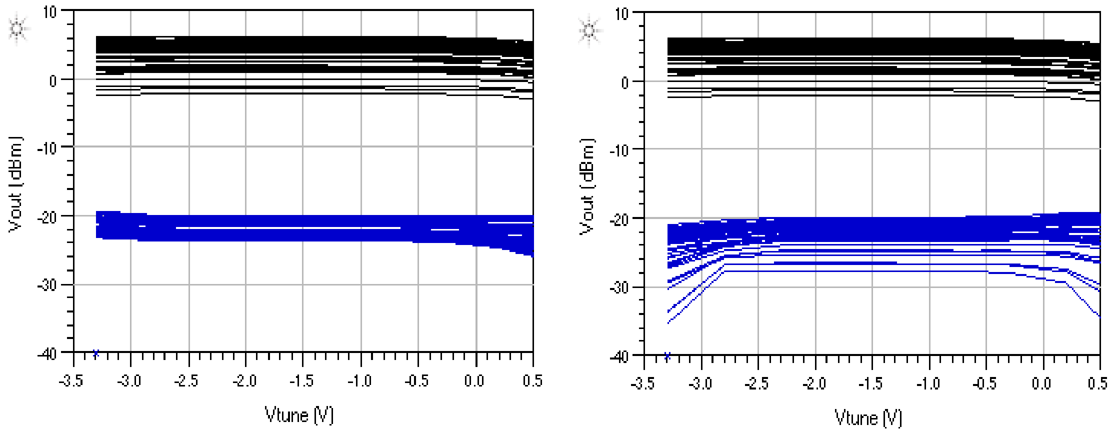
(a) (b)

Figure 5. (a) Oscillation frequency versus Vtune and (b) time domain of the output signal for Vtune=1.3 V



(a) (b)

Figure 6. SSPN (a) and absolute noise spectrum, (b) for Vtune=1.3 V



(a) (b)

Figure 7. Monte carlo analysis: (a) the fundamental (black line) and the first harmonics (blue line), (b) the fundamental (black line) and the second harmonics (blue line)

4. ANALYSIS AND DISCUSSIONS

VCO performances comparison depends on the intended application, while the oscillator specifications may vary from one application to another. But to get a general idea about the performance of an oscillator, designers use the Figure of Merit defined by the following equation [25, 26]:

$$\text{FoM} = L(f_0, \Delta f) + 10\log\left(P_{Consumption}\right) - 20\log\left(\frac{f_0}{\Delta f}\right) \quad (1)$$

where $L(f_0, \Delta f)$ is the single sideband phase nois (SSPN) at Δf offset frequency, f_0 is the oscillation frequency and, finally, $P_{Consumption}$ is the DC power consumption of the circuit in mW.

In the Table 1, we have cited the performance of some voltage controlled oscillators, published in the literature. These oscillators operate in the mm-Wave frequency band and are dedicated to the wireless communication systems. We observe that the size of our circuit, designed using 0.25 µm GaAs pHEMT, is very small compared to other pHEMT VCOs published in the literature, it also has an acceptable phase noise level and consumes a low electrical power.

Table 1. Performance of different VCOs

Ref.	Oscillation frequency (GHz)	Output power (dBm)	Phase noise (dBc/Hz) at 1 MHz	FoM (dBc/Hz)	Chip area (mm^2)	Structure	Transistor
[8]	29.4	2.85	-98	-166.41	3.75	4 Colpitts VCO	0.13µm SiGe BiCMOS
[12]	27.7	9.75	-113.115	-181.06	0.515	Colpitts	0.15µm GaAs pHEMT
[14]	28	-	-93	-172	0.5	Differential VCO	0.13µm SiGe BiCMOS
[14]	38	-	-90	-171.7	0.5	Differential VCO	0.13µm SiGe BiCMOS
[15]	28.3	11.8	-102	-	0.5	Negative resistance	0.15µm GaAs pHEMT
[16]	28.2	1.63	-106.9	-155.78	-	Hartley	0.15µm GaAs pHEMT
This work	28.29	0	-96.274	-164.85	0.268	Colpitts	0.25µm GaAs pHEMT

5. CONCLUSION

Provide a statement that what is expected, as stated in the "Introduction" chapter can ultimately result in "Results and Discussion" chapter, so there is compatibility. Moreover, it can also be added the prospect of the development of research results and application prospects of further studies into the next (based on result and discussion).

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