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Design and implementation of 4-bit binary weighted current steering DAC

Jayeshkumar J. Patel, Amisha P. Naik
Department of Electronics and Communication Engineering, Institute of Technology,
Nirma University Ahmedabad, India

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ABSTRACT

A compact current-mode Digital-to-Analog converter (DAC) suitable for biomedical application is repesented in this paper. The designed DAC is binary weighted in 180nm CMOS technology with 1.8V supply voltage. In this implementation, authors have focused on calculaton of Non linearity error say INL and DNL for 4-bit DAC having various type of switches: NMOS, PMOS and transmission gate. The implemented DAC uses lower area and power compared to unary architecture due to absence of digital decoders. The desired value of Integrated non linearity (INL) and Differential non linearity (DNL) for DAC for are within a range of +0.5LSB. Result obtained in this works for INL and DNL for the case DAC using transmission gate is $\pm$0.34LSB and $\pm$0.38 LSB respectively with 22mW power dissipation.

Corresponding Author:

Jayeshkumar J. Patel,
Department of Electronics and Communication Engineering,
Institute of Technology, Nirma University,
S G Highway, Ahmedabad, Gujarat, India.
Email: jayesh.patel@nirmauni.ac.in

1. INTRODUCTION

The Digital to Analog converter (DAC) is a circuit which converts digital signal into analog one. It is widely used in digital signal processors. DACs are often used to convert finite- precision time series to a varying physical data. These are mainly used in different applications like data distribution and acquisition systems, amplifier, Electronics display [1-7].

The Current steering DACs are the more commonly used architecture because of their small size and simplicity, high resolution and high speed. Based on the binary principle, current sources are scaled. Here for i^{th} current source, output current is equal to the 2^i*I, Where I = Least significant bit (LSB) current. For the design of DAC, various switches like NMOS, PMOS and transmission gate are explored. Characteristics of switching elements are one of the prominent factors for dynamic non linearity of DAC [8, 9].

In the proposed 4-bit DAC, four binary weighted current sources are used, those are represented as: I_o, $2I_o$, $4I_o$ and $8I_o$. The main advantage of this architecture is number of current cells required will be same as no. of bits. Hence, this architecture is most suitable for higher resolution implementations. The disadvantage with this architecture: it produces number of glitches (unwanted signal) on the contrary the unary architecture offers higher accuracy with greater linearity at the cost of chip area and power overhead [10, 11].

2. CURRENT STEERING DAC

DAC are vailable in form of various architectures: Decoder based DAC, Weighted R DAC, R-2R Ladder DAC, charged DAC, Cuurent steering DAC. Compared to other Architecturrs, Current steering DAC

is faster and low power consuming. There is no need of extra buffer to drive a load. A current steering DAC uses a reference current source. The source is replicated in each branch of DAC. The current sources belong to the branch is switched on or off according to digital inputs. In case of binary weighed current steering DAC, Current source having the value of 2^N*Io. Where Io is reference current. No. of switches are same as no. of current sources and same as N. Based on ON/OFF of current sources, total current is added and it will be the output current. Switches are MOS switches- NMOS, PMOS or transmission gate and sane are controlled directly by digital inputs. Output current is as per input code [12-18]. N-bit DAC is represented as low shown in Figure 1.

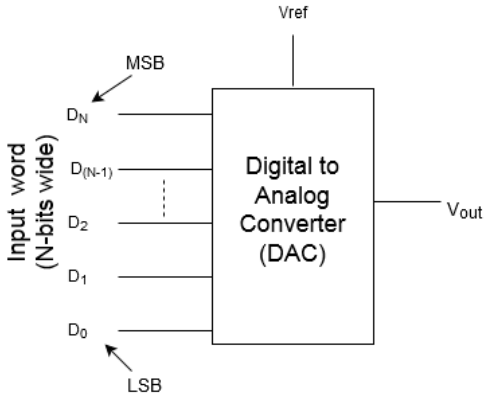

Figure 1. N-bit DAC representation

For N-bit DAC, output is expressed as follow:

$$V_{OUT} = \left(D_{N-1}\,2^{N-1} + \ldots + D_0\,2^0\right)\frac{V_{REF}}{2^N}$$

$$V_{OUT,\max} = \frac{2^{N-1}}{2^N}\cdot V_{REF}$$

A 4-bit binary weighted current steering DAC is designed and implemented with various switching approaches suitable for biomedical application. Though this architecture occupies lesser digital area and power, but suffers from glitches specifically when have more numbers of transitions in input. The authors have calculated INL, DNL of 4-bit Binary Current Steering DAC having various type of switches: NMOS, PMOS and transmission gate [9, 12]. DAC are evaluated based on the various parameters like Resolution, poer concumption, setteling time, dynamic range, non-linearity error (INLand DNL). In this paper, focus is given on INL and DNL. Differential nonlinearity (acronym DNL) represents a deviation of actual step size with reference to ideal step size, where step size is a difference of analog outputs for adjacent input values [6, 10]. Mathematically DNL for DAC is represented as follow:

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1$$

Integral nonlinearity **(**acronym INL) represents a deviation of actual analog output of DAC with reference to expected ideal value for given digital input value. It is also expressed in terms of DNL as follow [6, 10].

$$INL\ (n) = \sum_{k=0}^{n} DNL(k)$$

The characteristics of Switch play an important role for high speed, low power and high-resolution DAC. Which decides the Non linearity say DNL and INL of DAC. There are other architectures in implementation say unary current steering DAC. Said architecture is complex in terms of number of current sources. Here each current source has the same value of Io (reference current) but number of current sources are (2^N-1) and same no. of switches as well. It offers advantage in form of less glitches but required more

area. It is also required to have additional hardware to convert binary code into thermometer code [19-22].

Looking to implementation, area efficiency and free from additional hardware for binary to thermometer code conversion, Binary current steering DAC structure is the simplest one. N bit configuration which needs only N current sources. They are straight-forwardly worked by the linear binary input codes. However, due to the inadequate synchronization of the switches and dynamic behavior of the circuit, large glitches in form of impulses are observed at the output terminal. This problem is addressed using better switch. This structure also offers a merit in form of less no. of transistors as well. The 4-bit binary weighted current steering DAC is as shown in Figure 2 [17, 20, 23-25].

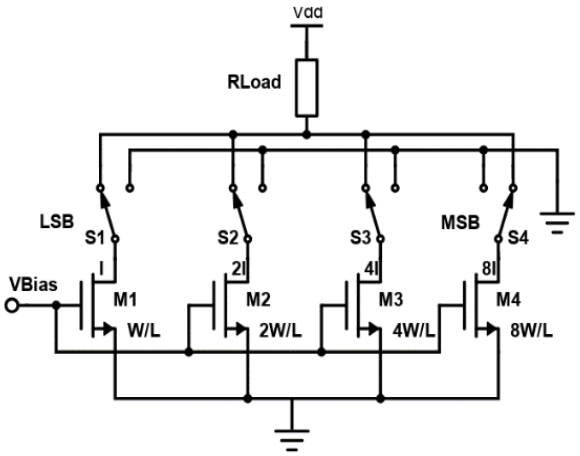

Figure 2. 4-bit binary weighted current steering DAC

The present work is focused to design and analyse the effect of various types of switches on non linearity eroor say DNL and INL. Based on understanding from the literature survey, three types of switches say NMOS, PMOS and transmission gate have been tried and simulation of each one has been carried out. For the proposed design and simulation, cadence tool is used with 180 nm CMOS technology. The proposed current steering DAC offers desired INL and DNL with rated power consumption.

3. VARIOUS SWITCHING APPROACHES

A main source of nonlinearity originates because of glitches in the current cell. More no. of transitions results more no. of changes the states of switches say on to off or vice versa. In case of 4-bit binary weighted DAC, when input changes from 0011 to 0100, big glitch is observed because of 3 transitions. Similarly, when input changes from 0111 to 1000, even big glitch will be there as there are 4 transitions. In case of unary weighted DAC, there is only 1-bit transition so there is no glitch but it needs more no. of current sources; for 4-bit unary current steering DAC, 15 current sources of having same value are required. Thermometer code is used to control the switches. Additional hardware is required to convert binary code into thermometer codes [26-29].

Characteristics of switch also play an important role. There are various options for the same: NMOS, PMOS, Transmission gate. NMOS and PMOS are used as a single device and controlled by sinlge input. While transmission gate is parallel combination of NMOS and PMOS and complementary control inputs are desired in this case [22].

4. SIMULATION RESULTS AND DISCUSSIONS

4-bit binary weighted current steering DAC have been implemented using cadence virtuoso in CMOS 180 nm technology. This converter developed and simulated in a 180 nm CMOS technology with supply voltage of 1.8 V. Based on three different type of switches, three possible combinations have been simulated. DNL and INL were calculated for all three DACs. It has been observed that the DNL and INL in case of DAC having Transmission gate are as ±0.42 LSB and ±0.4LSB, respectively. With the operating frequency of 200 Mhz, simulated power consumption was 22 mW.

Authors represented and compared three architectures and their outputs in form of currents. Figure 3 to Figure 8 shows the simulated results and output of proposed segmented DAC using various kinds of switches say NMOS, PMOS and transmission gate. Each architecture having two parts: one is current mirror and second is switching elements, current mirror part is common in all three architectures.

In case of NMOS switch-based architecture, big glitches have observed and same results poor non linearity. Glitches are available when there are a greater number of transitions in digital inputs e.g when input change from 0111 to 1000, prominent glitch is there. The step size should be equal but it is observed that even in some cases of input changes, it is reduced rather than to be increased. Same will have adverse impact on non-linearity error in terms of INL as well as DNL. Here in case of PMOS switch, same kind of observations are there as observed in case of NMOS switches. As digital input increase, output should increase. It is not always observed in case of NMOS and PMOS kinds of switches.

Transmission gate is one good option as a switch. Architecture having transmission gate offers a big advantage in form of reduction of glitches as well as continuous rise of current as desired which makes lesser value of INL and DNL. Graphs for INL and DNL of proposed current steering DAC using transmission gate switches are represented in Figure 9 and Figure 10 respectively. The simulated result of binary weighted DAC using transmission gate as a switch are as shown in Table 1.

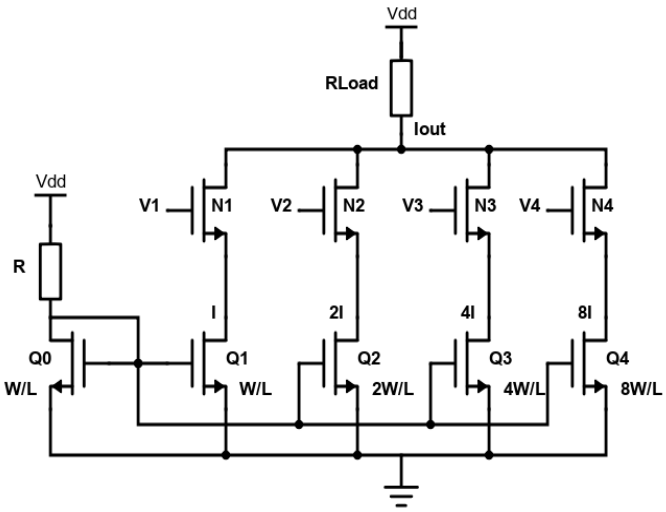

Figure 3. Architecture of binary weighted DAC with NMOS switches

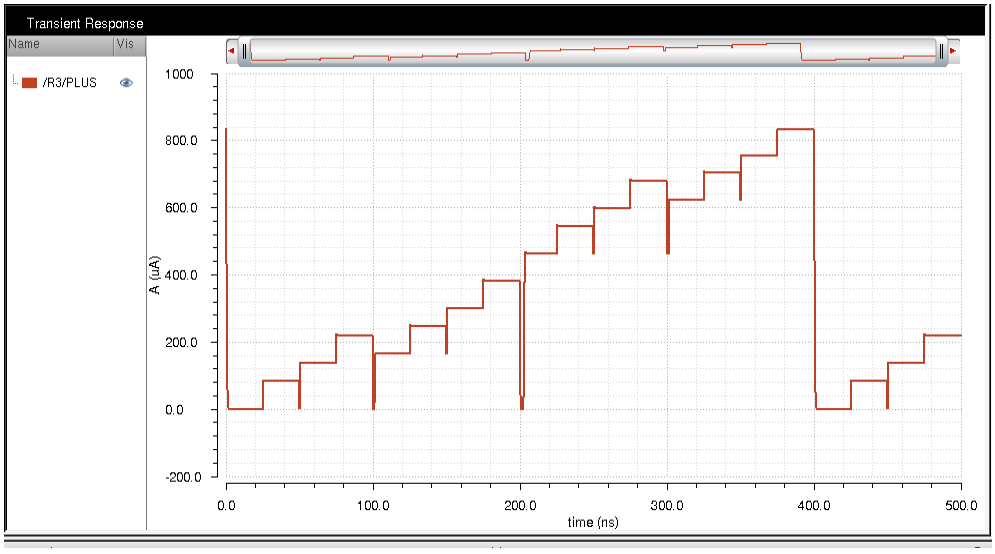

Figure 4. Current output of binary weighted DAC with NMOS switches

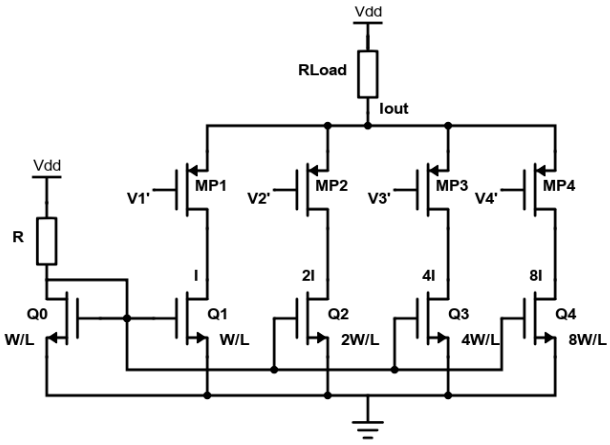

Figure 5. Architecture of binary weighted DAC with PMOS switches

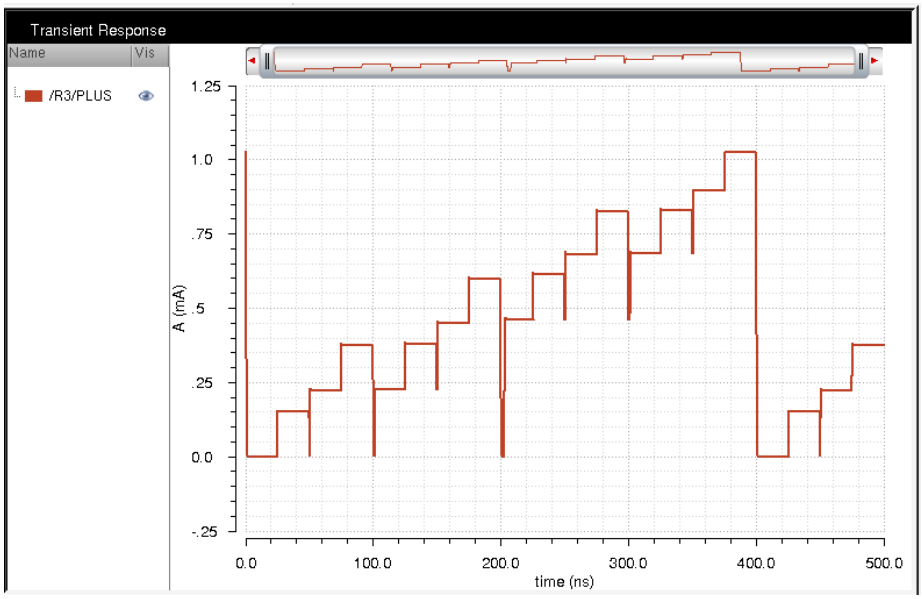

Figure 6. Current output of binary weighted DAC with PMOS switches

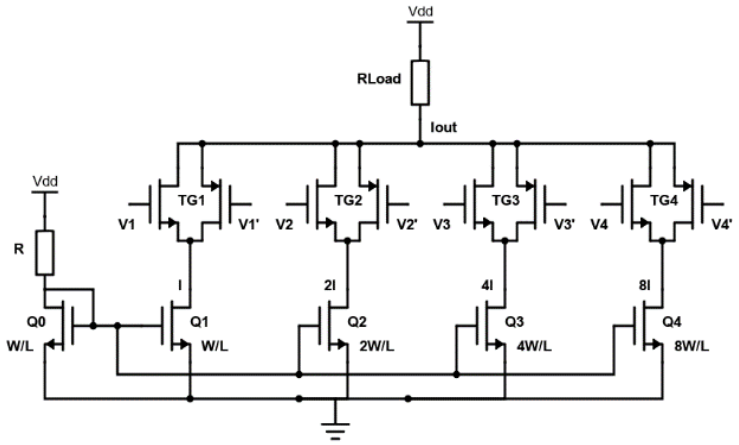

Figure 7. Architecture of binary weighted DAC with transmission gate switches

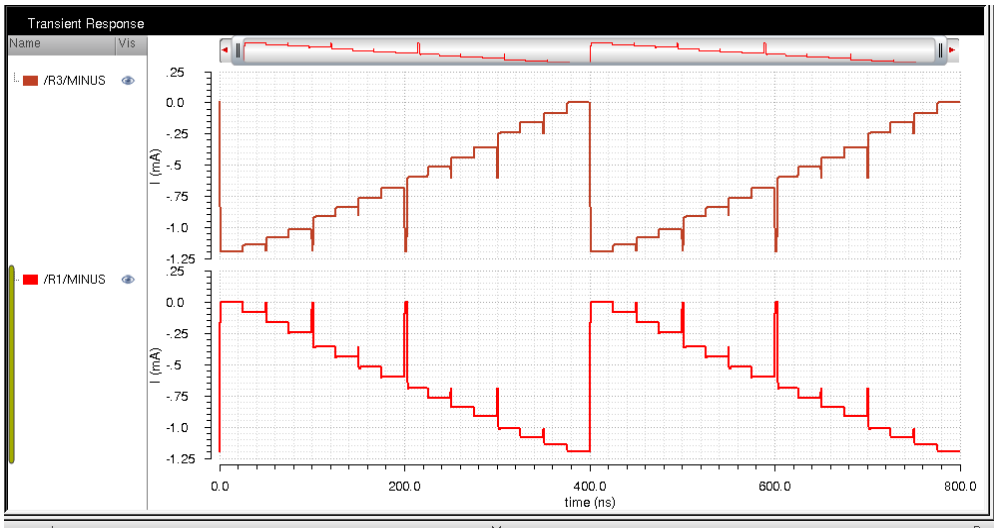

Figure 8. Current output of binary weighted DAC with transmission gate switches

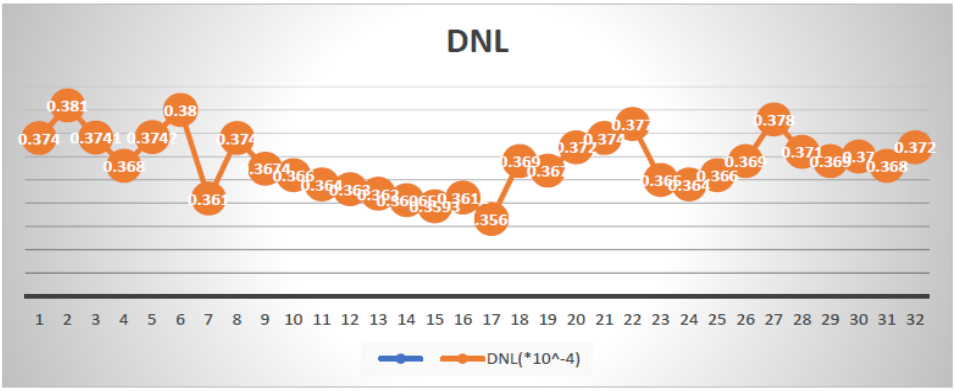

Figure 9. DNL graph of 4 bit binary weighted DAC having transmission gate

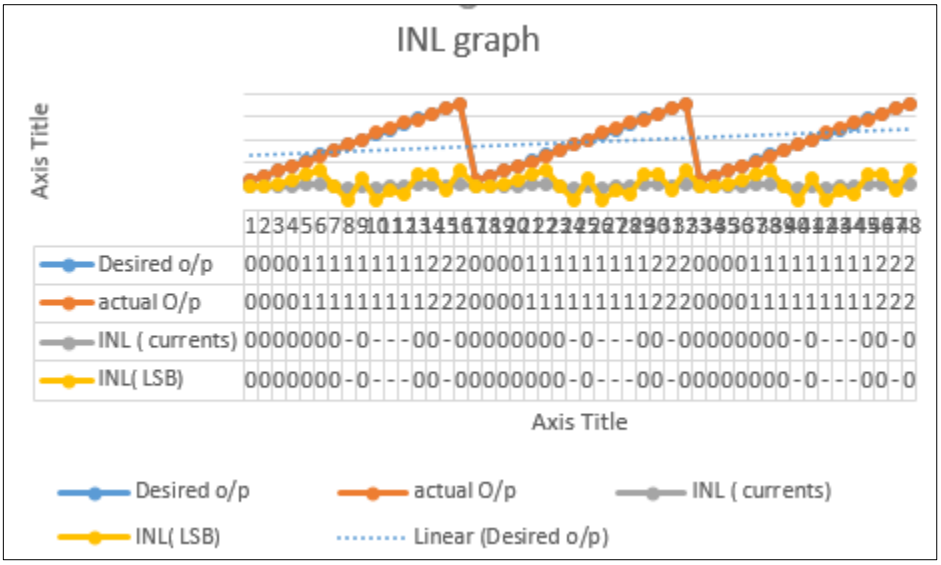

Figure 10. INL graph of 4 bit binary weighted DAC having transmission gate

Table 1. Simulated result of DAC

Parameters	Value	Parameters	Value
Technology	180	INL (Max)	0.34 LSB
Resolution	4-bit	DNL (Max)	0.38 LSB
Approach	Binary weighted	Power (Max)	22mW
Supply voltage	1.8 V	Frequency	200 Mhz

5. CONCLUSION

A binary weighted 4 bit current-mode digital to Analog converter (DAC) useful in the field of biomedical application designed and simulated using 180nm CMOS Process.In this implementation the authors have calculated INL and DNL of DAC having NMOS, PMOS and transmission gate as a switch. It is desired to have INL and DNL in the range of $\pm$0.5 LSB. Based on comparison. It has been observed that Digital to Analog convertor with transmission gate as a switch, DNL and INL are 0.38 LSB and 0.34 LSB respectively. Power consumption is observed as 22mW.

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BIOGRAPHIES OF AUTHORS

Jayeshkumar J. Patel is pursuing his Ph. d from Nirma University, Ahmedabad in the field of mixed signal circuit design. He obtained his M. Tech in EC (VLSI Design) from Institute of Technology, Nirma University, Ahmedabad in 2007. He did his B.E from BVM College of Engineering, Vallabh Vidyanagar. He has published many technical papers in national and international journals. He has more than 18 years of experience in teaching at UG & PG levl. He also worked for industry for about 5 years. His research interest includes Analog and Mixed signal VLSI

Dr. Amisha Naik is working as Associate professor at EC department, Nirma University, Ahmedabad since 2001. She teaches both at UG and PG level. She did B. E in Electronics from Regional Engineering College, Surat in the year 1997 and obtained M. Tech and Ph. D in VLSI Design area in the year 2006 and 2011 respectively from Nirma University, Ahmedabad. She has published many papers in national and international journals. She is guiding several Ph.D students in the area of analog and mixed signal circuit design.