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A two-stage power amplifier design for ultra-wideband applications

Idrees S. Al-Kofahi, Zaid Albataineh, Ahmad Dagamseh
Hijjawi Faculty for Engineering Technology, Al Yarmouk University, Jordan

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ABSTRACT

In this paper, a two-stage 0.18 μm CMOS power amplifier (PA) for ultra-wideband (UWB) 3 to 5 GHz based on common source inductive degeneration with an auxiliary amplifier is proposed. In this proposal, an auxiliary amplifier is used to place the 2nd harmonic in the core amplified in order to make up for the gain progression phenomena at the main amplifier output node. Simulation results show a power gain of 16 dB with a gain flatness of 0.4 dB and an input 1 dB compression of about -5 dBm from 3 to 5 GHz using a 1.8 V power supply consuming 25 mW. Power added efficiency (PAE) of around 47% at 4 GHz with 50 Ω load impedance was also observed.

Corresponding Author:

Zaid Albataineh,
Hijjawi Faculty for Engineering Technology,
Al Yarmouk University,
Irbid, Jordan.
Email: zaid.bataineh@yu.edu.jo

1. INTRODUCTION

Digital pulse wireless, more commonly known as ultra-wideband is a high bandwidth radio technology is used for short range and low-power communications [1-5]. UWB has come to be known as a direct competitor to bluetooth and WiMax as it can fully utilize high data rate along with wide spectrum efficiency while using less or very low power transmission [6-15].

There is a problem regarding the transmission of data up to 480 Mbps. Two solutions have been proposed by the IEEE802.15.3a. The first proposal is the multiband orthogonal frequency division multiplexing (MBOFDM) UWB and the second represents the direct sequence code division multiple access (DS_CDMA) UWB [16-25]. The first generation UWB system uses a low-frequency band of 3.5 to 5.1 GHz in its required approach. Under this set up the main application for ultra-wideband systems being WiMedia Alliance descriptions acts as short-range high-data communication systems. This is used in the consumer electronics field composed of mobile cellular phones, laptops, and digital cameras. Moreover, this is the foundational transport protocol used by bluetooth communication system v3.0 and Wireless USB-based system [26-32].

Transmitter designs are challenged by the power amplifier (PA) circuits because of the demands of high efficiency, appropriate output power, high system gain, and broad-band input matching system even when using lower power consumption. These criteria put challenges for transmitter design even when various topologies in the same manner with matching-based and resistive-shunt feedback topologies are used. For general purposes, the topology that is used is backed by the amplifier requirements and features. The main feature considerations are desirable efficiency level, power control and high linearity, and

efficiency. This paper uses a two-stage common sources (CS) inductive degeneration with feedback power amplifier for ultra-wideband front-end transceiver. The proposed amplifier uses 0.18 μm CMOS process. The cascode structure will be used for the first step of the power amplifier by optimizing process in order to get the maximum possible gain. A comon source amplifier which is employed as a second step to enhance the power added efficiency (PAE) by utilizing the feedback in the common source amplifier.

The rest of this paper is organized as follows. A characterization of ultra-wideband power amplifier circuit design is presented in section 2. In section 3, the experimental outcomes are shown. Finally, in section 4, conclusions are given.

2. UWB POWER AMPLIFIER CIRCUIT SCHEME

In this paper, the presented power amplifier design is based on the proposed amplifier design in [19] to optimize the circuit design process in terms of circuit gain and transmitted power as long as sustaining an ultra-wideband feature. Figure 1 presents the design circuit of the proposed method. In this design, we use two stages power amplifier to achieve the optimal power output. The first stage consists of a cascode circuit and a current mirror method. The second one employs a common source amplifier to adjust the gain and enhance the output power of the design circuit with inserted Lg inductor to enhance the lineraty and input matching of the design circuit. The presented power amplifier considers a power use of 20 mW while the voltage supply is a $1.6\,V$ dc voltage. The approxmited drain current would be of 26 milliampere (mA). By considering M_1 transistor of the first stage will draw a current of $8.8\,mA$ from the $1.6\,V$ dc source, one can approximately find the size of M_1 transistor about $160\,\mu m$ as follows:

$$I_{DD} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs1} - V_{Th}\right)^2 \quad (1)$$

where V_{gs1}= 0.75 V, V_{Th}= $0.5\,V$, μ_n = 0.03801 m^2/Vs and C_{ox}= $0.00946\,F/m^2$, for a $0.18\,\mu m$ CMOS technology.

One can determine the trans-conductance g_m as follows:

$$g_m = 2\sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}I_{DD}} \quad (2)$$

Then, one can find the input-impedance of transistor (M_1) as follows [18]:

$$\boldsymbol{Z_{in} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}} \quad (3)$$

Also, the resonance frequency of the presented circuit is given by:

$$\boldsymbol{\omega_0 \approx \sqrt{\frac{1}{(L_g+L_s)C_{gs}}}} \quad (4)$$

The stability and the lineraty of the presented circuit is improved by adding the degeration inductor (L_{g1}) at the source terminal of the main transistor (M_1). Moreover, the degeneration inductor employs to achieve the input impedance matching network.

In order to choose the appropriate value of the the degeration inductor (L_{g1}), one can pick a small one so that it would be less than $0.6\,nH$. This small-value inductor would be simpliychanged by a bond-wire inductor-type. This Also helps to minimize the chip (integrated-circuit) area.

The transistor (M_2) is used to form the cascade form so that the gain is enahanced. This also helps to increase the active load of the first stage so that the voltage gain increases. One also can add small-value inductor such as (L_{d1}) so that it is shunt inductor and causes the circuit to achieve the peaking resonate by lessen the effects of the parasitic capacitances of the CMOS technology. Moreover, one can reduce the power consumption by increasing the value of the L_{d1} inductor.

The input voltage for the first stage is:

$$v'_{in} = I_g L_g + v_{gs1} + g_{m1} v_{gs1} l_{s1} \quad (5)$$

where the gate current is:

$$I_g = g_{m1} v_{gs1} - g_{m4} v_{gs4} \quad (6)$$

and, the output voltage for the first stage is:

$$v'_{out} = g_{m1} v_{gs1} l_{s1} \quad (7)$$

If we substitute $\boldsymbol{I_g}$ from (6) into (5), and then divide (7) by (5), we get the gain:

$$A_{1st\ stage} = 1 + \frac{1}{g_{m1} l_{s1}} + \frac{l_{s1}}{l_{g1}} + \frac{g_{m1} v_{gs1}}{g_{m4} v_{gs4}} \frac{l_s}{l_g} \quad (8)$$

A second stage is a simple common source stage without cascade transistor and degeneration inductor (L_g). By doing the aforementioned procedures to assume a small current of $10\ mA$ to be used by CMOS transistor (M_3) of the presented circuit, then, one can estimate the size of the transistor (M_3) based on (1) is approximately 110 μm.

The input voltage for the second stage is:

$$v''_{in} = v_{gs3} + g_{m3} v_{gs3} l_{s2} \quad (9)$$

and, the output voltage for the first stage is:

$$\boldsymbol{v''_{out} = g_{m3} v_{gs3} l_{s2}} \quad (10)$$

The gain of the second stage is:

$$A_{second\ satge} = 1 + g_{m3} l_{s2} \quad (11)$$

A high frequency amplifier requires a high gain and output power transistor. The suggested size is a large transistor around M3. This is normally has a high parasitic capacitance and transconductance that draws on increasing power consumption. Therefore, it is better to optimize the size at $150\ um$ for suitable power consumption. In the presented circuit, the four resistors R_{b1} to R_{b4} be used as biasing network of the power amplifier. It has two-configrations of the current mirror circuits, M4 and M5.

These configrations works as to supply the presented circuit in additional to the bias-based resistors. The large-value of the resistance R_{b3} is employed to form a good isolation barrier between the RF signal and the output terminal. Biasing transistors can be varied based upon the required noise and bandwidth so that itsd job to flat the curve of the gain over a wide-bandwidth range. This can be done through sufficient shunting using large-value capacitors (C_{b1}-C_{b5}) as part of the presented circuit with dc-blockings formed by block capacitors C_{in}, C_{int} and C_{out}.

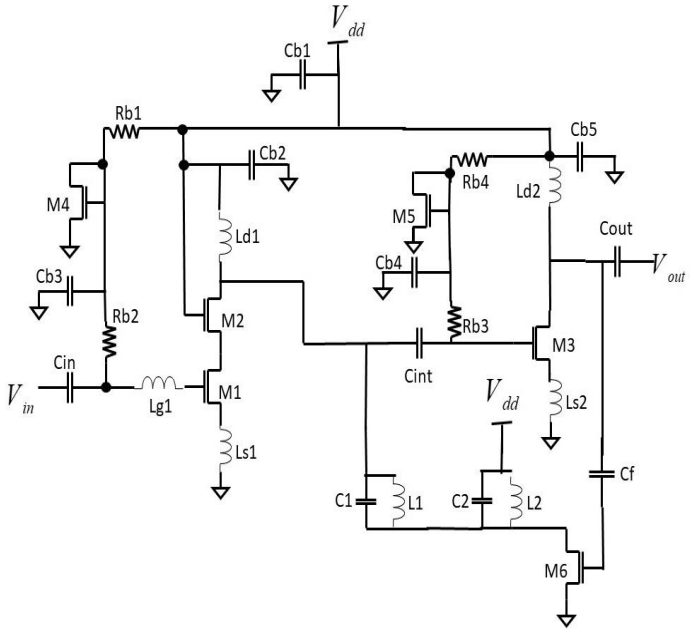

Figure 1. Schematic of the presented two-stage UWB power amplifier

The auxiliary injection circuit is designed using a Class–C amplifier. This amplifier is characterized by high efficiency and prevents decaying power gain curve through an increase of input power, in contrary to Doherty PA. This is similar to the Class B amplifier with its operating point transistor found in the cutoff region. However, the required threshold built-in voltage of the transistor should be passed by the voltage across the gate and source terminals. The RF cycle is reduced to less than half, that is is why Class C mode becomes a logical extension or the reduced angle concept.

3. EXPERMENTAL RESULTS

The presented ultra-wide power amplifier is designed based on the 0.18 μm CMOS technology for ultra-wideband (UWB) 3 to 5 GHz. To optimize the presented design and simulate it, Agilent technologies advanced design system (ADS) software was employs. The S-parameters is a tool to measue and study the performance of the presented design. One can emloy it to find the power and voltage gain (S_{21}), Input return loss (S11), the reverse isolation (S_{12}) and noise figure of the presented circuit (NF). Figure 2 shows the measured small signal S-parameters. It is clear that A PA gain of 16 $\pm$ 0.5 dB over the 3 to 4.9 GHz frequency range while maintaining a $3-dB$ bandwidth of 2.76 to 5.2 GHz is obtaind, in addition to an acceptable reverse isolation of more than 40 dB over the range of 1 to 8 GHz.The PA also achieves an output power up to +13 dBm and PAE of 47% in a 50 Ω load as shown in Figure 3.

Moreover, we have study the effect of changing the supply voltage on the gain cure. As Figure 4 shown, the gain as a function of supply voltage imples that the presented circuit has a good stability over the interested frequency bands. The added power of a DC source allows an amplifier to increase its input signal source. This is used to determine the amount of DC input power contributed to the amplification of an input signal as shown in by the PAE in Figure 5.

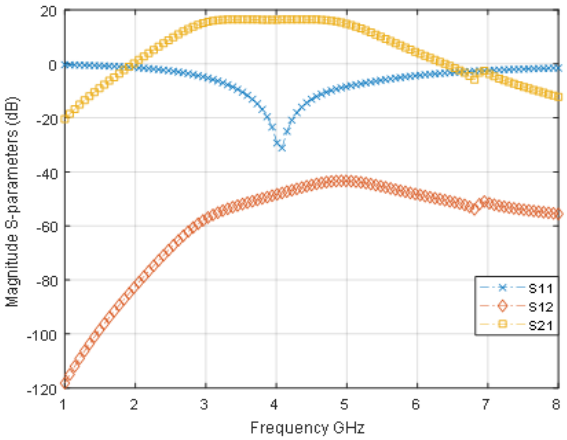

Figure 2. Measured S-parameter

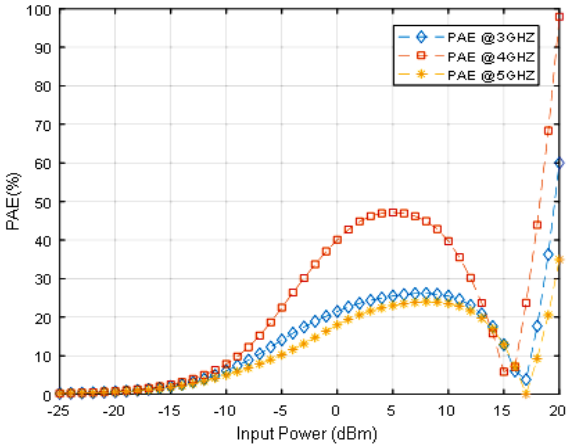

Figure 3. Measured PAE at 50 ohm load impedance

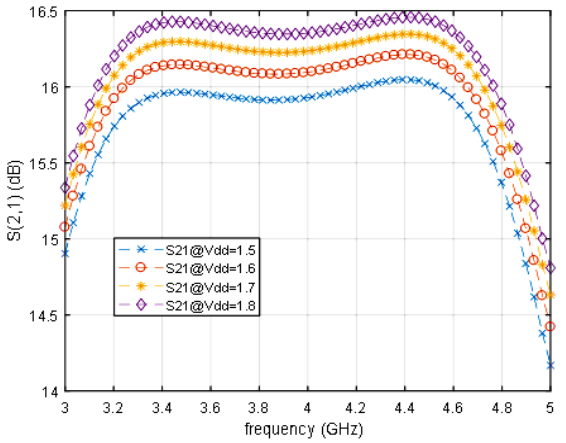

Figure 4. Gain vs Vdd

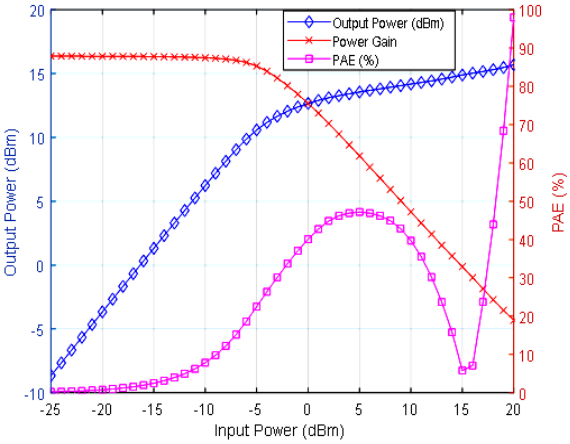

Figure 5. Output power vs Input power

Figure 6 shows the variation of PA power gain. It is clear that the gain increases to about 16.35 dB and then starts decreasing. This measurement is the ideal measurement and is often used as gauge to amplifier efficiency or inefficiency, making it a figure of merit. The simulated result of noise figure is shown in Figure 7. The minimum noise figure is 1.36dB at 3.7GHz and 2.4dB at 5GHz.

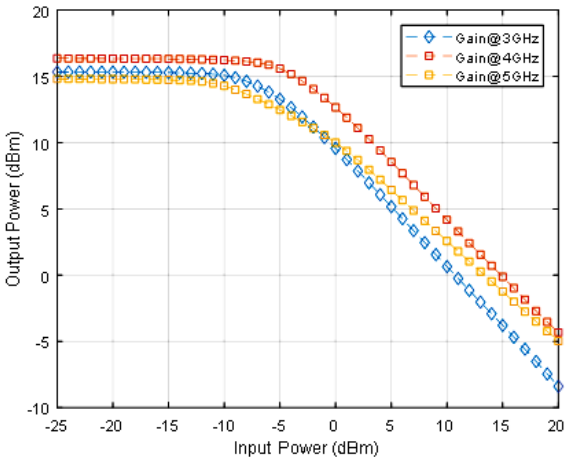

Figure 6. Power gain

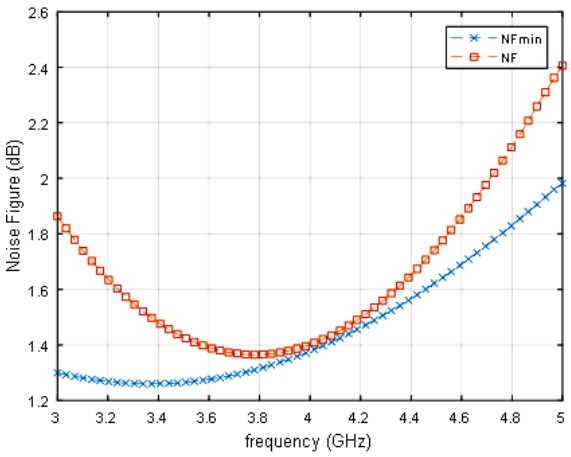

Figure 7. Noise Figure vs frequency

Linearity is also measured using IP3 or IP2 within a circuit based upon the 1-dB compression point. It is more directly measurable than IP3 since the measurement requires only one tone as opposed to the two tones required by the IP3 measurement. While the measurement may be completed in one tone, multiple tones may also be used for measurement purposes. 1-dB compression point refers to the input power level, where any power less than 1dB power is considered an ideal linear device. Figure 8 shows P1dB curves for linearity approximation. P1dB is about 11.2 dBm.

The output power versus input power for PA starts saturating at about 12 dBm, and it reaches 15 dBm as it shown in Figure 5. The stability-factor (K), depicted in Figure 9. It shows that the K is greater than one, among the required frequencies, as it shown in Figure 9.

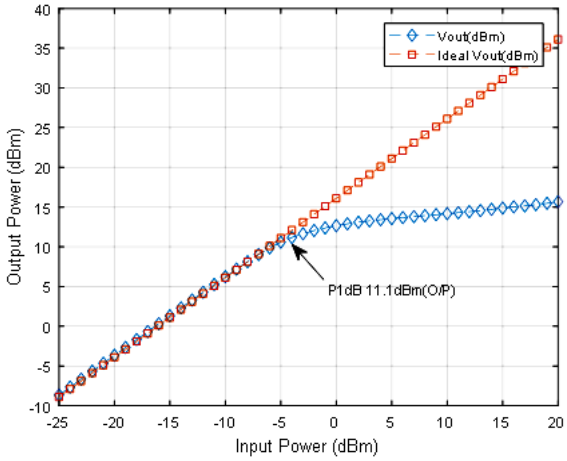

Figure 8. P1dB

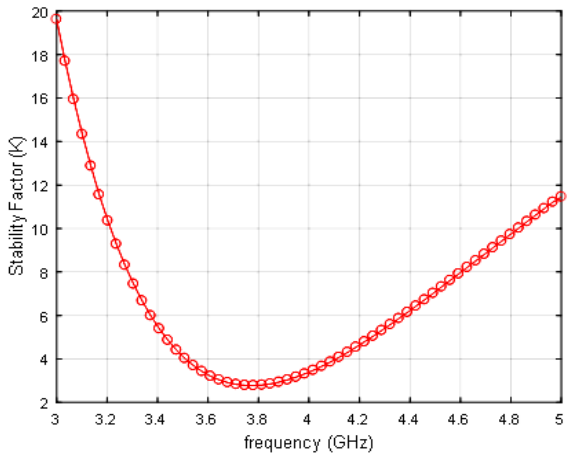

Figure 9. Stability factor (K)

One can define the factor μ to measure the stability; where the factor represents the shortest path from the center point in the Smith-chart to the point outside the stabe region in the load plane. As shown in Figure 10, mu (μ), and mu (μ) prime factors are greater than 1.

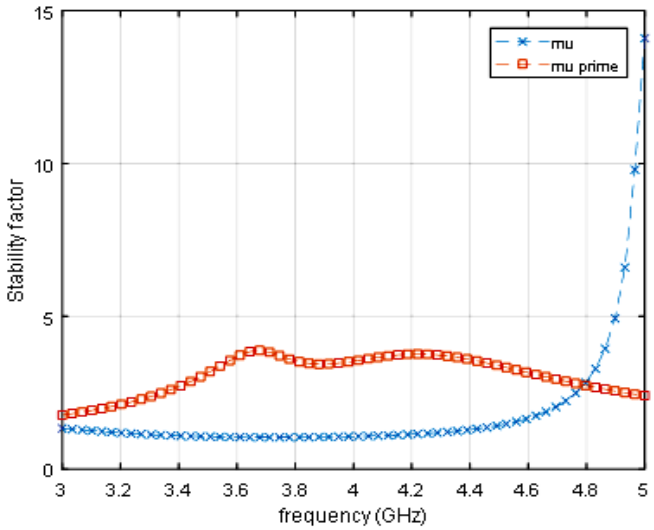

Figure 10. Stability factor (mu)

The voltage standing wave ratio (VSWR) is a tool to represnt +VE and real number of RF antennas. In general, a good antenna gives a small-value of the VSWR, as it provides more power in watt and matches the line of transmission of the antenna. For ideal case, the value of the VSWR equals to 1 where there is no waves (power) would be reflected. One can define the VSWR as the ratio of the max-value of the standing-wave to the min-value of it. In Figure 11, we show the values of the VSWR for the presented circuit. A group-delay is a tool to measure the device phase distortion, one can define the group-delay as a function of frequency where it represents the actual transit-time, and Figure 12 shows group-delay response for the PA.

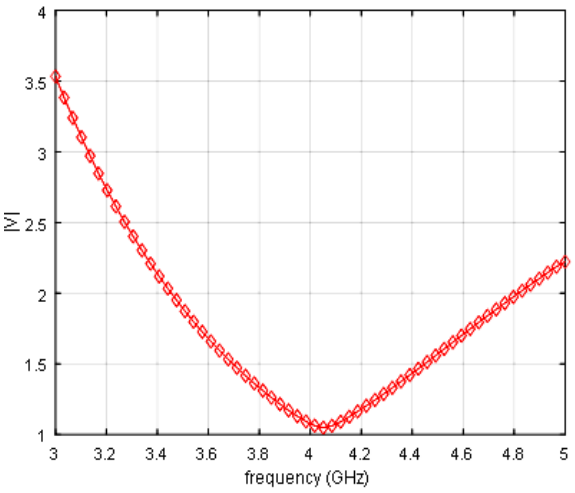

Figure 11. VSWR

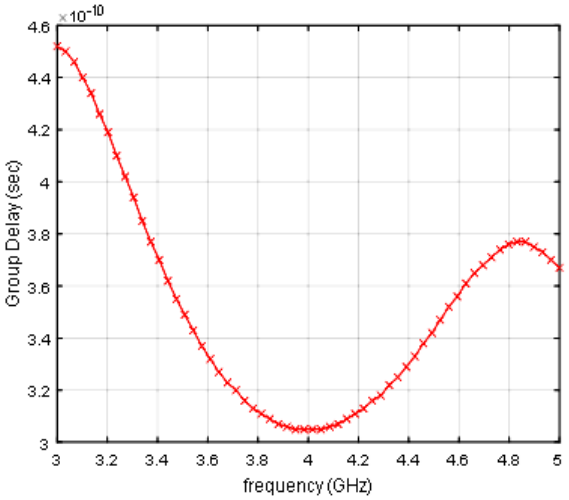

Figure 12. Group delay

4. CONCLUSION

A 0.18µm CMOS lower band UWB system (3 − 5 GHz) was recreated in this papaer. Using a CS inductive degeneration, two stage process via 2nd harmonic topology, a PA of +16 dB voltage gain, 0.5 dB tolarience gain, 11.1 dBm of output 1dB-compression and the power efficiency about 47% at 4 GHz, is achieved with power consumption of only 25 mW. The experimental results show that the low band UWB transmitter can be successfully implemented on portable and mobile devices on the UWB system.

APPENDIX

Ref	3 dB BW (GHz)	S11 (dB)	S22 (dB)	Gain@4GHz (dB)	P1dB@4GHz (dBm)	PAE@4GHz (%)	Power (mW)
[15]	3.1 to 4.8	<-10	<-8	19	-22.0 (input) -4.2 (output)	n/a	25
[16]	3.1 to 10.6	<-9	<-8	15	0 (output)	n/a	25.2
[17]	3 to 12	<-10	<-8	10.46	+5.6 (output)	n/a	84
[18]	3 to 4.6	<-10	<-10	17.5	+0.42 (output)	3.9%	n/a
[19]	2.6 to 5.4	<-5	<-6	15.8	-3.4 (input) +11.4 (output)	34%	25
This study	2.8 - 5.2	<-6	<-0.5	16.2	-3.8 (Input) 10.1 (Output)	47%	25

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Dr. Idrees S. Al-Kofahi received his MSc and Ph.D. in Microelectronics Engineering from the Liverpool John Moores University, UK in 1993 and 1997, respectively, and the bachelor degree in Electrical Engineering from Yarmouk University in 1986. Since 1997, he has been working with the Department of Electronics Engineering, Hijjawi Faculty for Engineering Technology, Yarmouk University, Jordan. During that time He left the university to join United Arab Emirates University (2002-2004) and Al Jouf University, KSA (2010 to date). He is currently an Associate Professor.

Zaid Albataineh received the B.S. degree in electrical engineering from the Yarmouk University, Irbid, Jordan, in 2006, and received the M.S. degree in the communication and electronic engineering from the Jordan University of Science and Technology JUST, Irbid, Jordan, in 2009. He received the Ph.D. degree in electrical and computer engineering department, Michigan State University (MSU), USA, in 2014. His research interests include Blind Source Separation, Independent Component analysis, Nonnegative matrix Factorization, Wireless Communication, DSP Implementation, VLSI, Analog Integrated Circuit and RF Integrated Circuit.

Ahmad Dagamseh received his bachelor degree in electronics engineering from Yarmouk University in Jordan in 2004, master degree in microelectronic engineering (solar cells) from Delft University of Technology in the Netherlands in 2007 and Ph.D. degree from the University of Twente in the Netherlands in 2011 in bio-inspired sensors' design using Micro-ElectroMechanical Systems (MEMS). Since February 2012 he was appointed as assistant professor at Department of Electronics Engineering at Yarmouk University in Jordan. His research interests include: thin-layers solar cells, biologically inspired micro-systems and sensors, micro electromechanical systems, interfacing electronics and related signal processing.