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# An area efficient memory-less ROM design architecture for direct digital frequency synthesizer

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**ABSTRACT**

This paper introduces a new technique of designing a read-only memory (ROM) circuit, namely; memory-less ROM as a novel approach to designing the ROM lookup table (LUT) circuit for use in a direct digital frequency synthesizer (DDFS). The proposed DDFS design uses the pipelined phase accumulator (PA) based on the kogge-stone (KS) adder. Verilog HDL programming is encoded on the architecture circuit of pipelined PA and contrasted with other PA based on various adders. The obtained results define the KS adder as having good capabilities for improving the throughput. In addition to the quarter symmetry technique, the built memory-less ROM to obtain the quarter sine amplitude waveform is proposed and implemented in the DDFS system. The implementation of the proposed technique replaces the necessary ROM registers (384 D flip-flops) and multiplexers with simple logic gate circuits instead of traditional ROMs. This technique would reduce the area size and cell count by 56% and 32.6% respectively.




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## 1. INTRODUCTION

The PA contributes to the speed performance of the DDFS. The PA speed performance is attributable to the pipelining technique and fast adders [1], therefore, improving these features will increase the PA operating frequency. Reducing the read-only memory (ROM) size and decreasing the power consumption are the common goals of research. The conventional ROM size requires a ($2^P \times P$), where P represents the addressing phase bits. The ROM size exponentially increases with the number of addressing phase bits. Quarter wave symmetry technique was applied in [2] and [3] to reduce 75% of the ROM size, by addressing the ROM with only quarter sine wave by P-2 phase bit, and to utilize the two highest, most significant bits (MSBs) for accomplishing the half and full ($\pi$ and $2\pi$) sine waveforms with 1'complement and 2'complement, respectively. Quad line approximation technique as another technique [4], to design a ROM circuit with a relatively small ROM bit size. An adder, multiplexer, and complementor were needed as additional hardware to convert the amplitude phase into a sine amplitude waveform. In addition to the mentioned ROM design approaches, several techniques such the ROM-DAC and ROM-less techniques were applied in [5-7] respectively, to architect the DDFS system.

The current paper presents a high-speed DDFS with pipelining PA based on clock shifting technique. In the proposed work, memory-less ROM is implemented as a novel phase-to-amplitude converter (PAC) method. PA is a generator that provides a digital phase with 0–2π range values. The PA architecture consists of the adder and register, as shown in Figure 1.

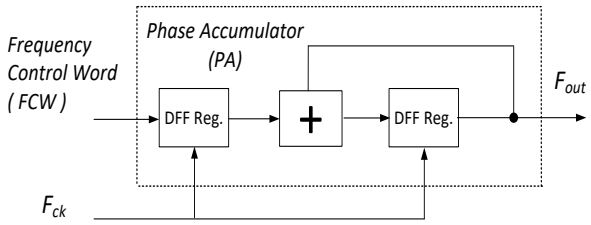



Figure 1. Phase accumulator architecture

Kogge-stone adder (KS adder) is a parallel prefix adder family that consists of groups of $p$ and $g$ cells. The arithmetic operation for a KS adder is as follows:

$$p_i = x_i \oplus y_i\,,\ g_i = x_i\ .\ y_i \tag{1}$$

In (2), (3), and (4) presents the sum and carry out of a 4-bit KS adder.

$$S_0 = p_0 \oplus c_{in.} \tag{2}$$

$$S_{2:1} = p_{2:1} \oplus C_{2:1} \tag{3}$$

$$C_{out} = (g_3 + p_3.\ g_2\ ) + p_3.p_2C_2 \tag{4}$$

The block circuit diagram of the proposed 4-bit KS adder in Figure 2 shows the groups of $p$ and $g$ cells. These cells connect with each other to achieve the summation outputs of the parallel prefix tree with minimum delay.

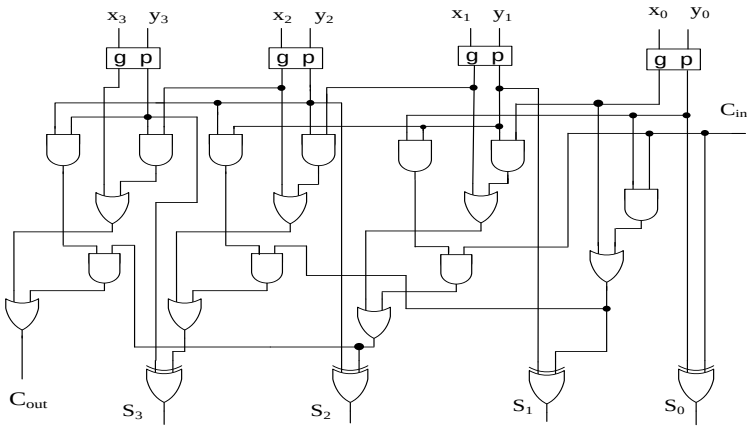



Figure 2. Block circuit diagram of 4-bit KS adder

Pipelining is a technique in which the given PA is partitioned into a number of subphase accumulators that should be sequentially performed. As a result, the frequency operation speed is multiplied (doubled) as much as the partitioned pipelining stage registers. Parallel prefix adders are fast adder circuits that can be used for PA binary addition. Parallel prefix adders, such as Sklansky [8], KS [9-12], Brent-Kung (BK) [13], Beaumont-smith (BS) [14] as well the carry look-ahead (CLA) [15] and ripple carry adder (RCA) [16] are applied in the conventional 12-bit pipelined PA design, as shown in Figure 3. The PAs'

designs are coded in Verilog hardware description language (HDL) code and verified with Cyclone III FPGA kit and Quartus II software. The frequency speed comparison result shown in Figure 4 demonstrates that the KS-based pipelined PA outperforms the other PA architectures.

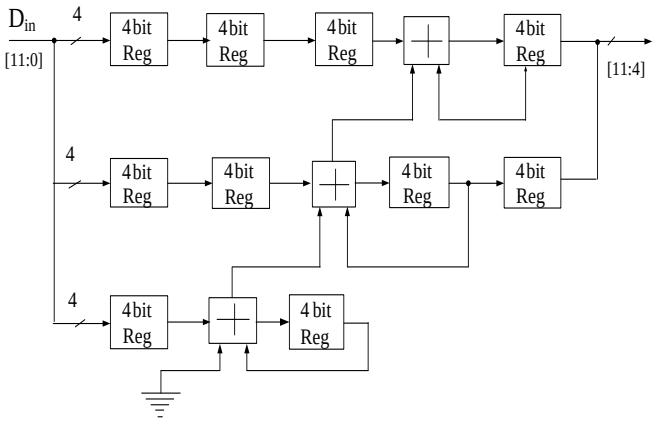



Figure 3. Pipelined PA design circuit diagram

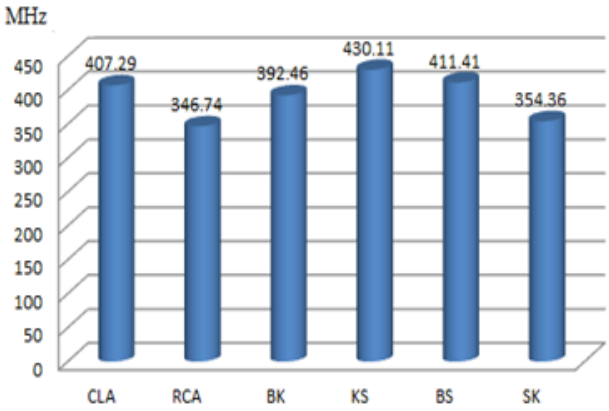



Figure 4. Frequency operating speed comparison of KS-based pipelined PA architecture and other PA architectures

## 2. PHASE TO AMPLITUDE CONVERTER (PAC)

PAC is a storage memory of the addressing data in the DDFS system, and it is used to provide the required digital sine amplitude waveform for representing the PA output. The ROM size area exponentially increases with number of addressing input bits. Moreover, 75% of the ROM size can be saved using the quarter symmetry technique in this design, which can be achieved by addressing the ROM with only quarter sine wave by P-2 phase bit. The two highest MSBs are utilized to achieve the half (π) and full sine (2π) waveforms with the 1'complement and 2'complement, respectively. The 2'complement is achieved by adding a full adder at the output gate to accomplish the full sine wave. Adding half of the LSB offset to the stored memory address of the display values eliminates the 2'complement full adder hardware from the proposed design and replaces them with only 1'cmplement.

The phase mapping address values are mathematically calculated based on the following equation:

$$sin\ A\ =\ (2^A - 1) \times\ sin\left(\frac{\pi}{2} \times \frac{[0:(2^A-1)]}{2^A}\right) \quad (5)$$

where A is the number of the addressing phase bits of the ROM input. The achieved fraction values (0–0.99) of $sin\ A$ (5) are converted using MATLAB into 6-bit binary numbers (0–63) to collect the memory-less ROM circuit based on BCD-to-7-segment display technique.

## 3. MEMORY-LESS DESIGN ARCHITECTURE

The basic concept of BCD-to-7-segment decoder is explained as follows: BCD is used to provide the (0–9) numbers listed in the binary digits' rows, whereas the listed column lines based on the binary digits' rows is used to provide the segment display. The memory-less ROM replacement circuit is designed on the basis of the 7-segment display and the technique applied in [17-19]. The suggested quarter sinewave values, which are listed in 6-bit binary digits in rows 0–63 ($X_5$:$X_0$), are used as a counter of the memory-less ROM circuit. The required ROM output bits are listed in the column line ($A_5$:$A_0$) on the basis of the binary digit rows as showon in Figure 5.

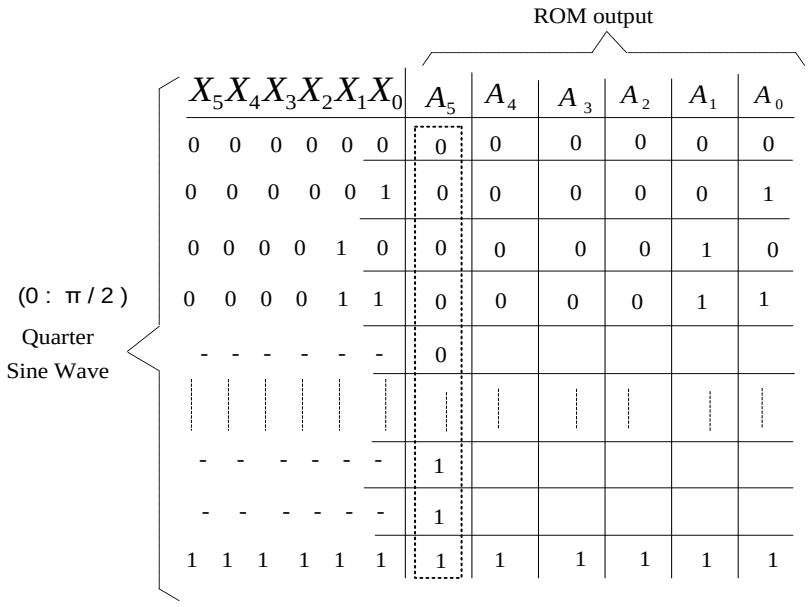



Figure 5. Memory-less design concept

Karnaugh map and Boolean expression were used to simplify the ($X_5$: $X_0$) created logic circuits. On this basis, the *sin A* equation for $A_5$ and $A_4$ are expressed as follows:

$$A_5 = X_0 + \overline{X_0}\,X_1\,(X_2 + X_3X_4) \quad (6)$$

$$A_4 = X_0(X_3 + X_2 + X_1) + \overline{X_0}X_1\overline{X_2}\left(\overline{X_3} + X_3\overline{X_4}\right) + \overline{X_0}\,X_2\,\left(X_3 + \overline{X_3}X_4X_5\right) \quad (7)$$

and so on for the rest of the equations ($A_3$, $A_2$, $A_1$ and $A_0$).

The existence of ROM look-up-table in the DDFS system is necessary to convert the phase signal into an amplitude sine waveform. To achieve the desired values of the ROM circuit, it must involve a number of registers and multiplexers equal to the number of required points of the amplitude sine waveform. Based on the Karnaugh map, the equations of the obtained values are simplified and presented in basic AND, OR, and XOR logic gates. The conventional 6-bit ROM requires 64 6-bit registers (384 D flip-flops (DFFs)) and six multiplexers (64×1). Applying the memory-less ROM circuit in the proposed design as shown in Figure 6 replaces 139 of AND, OR, and XOR logic circuits instead of the 384 DFF registers and multiplexers. Table 1 lists the comparison results between the conventional ROM LUT and the proposed memory-less ROM circuit.

Table 1. Comparison results of conventional and memory-less ROM logic gates

| (6-bit) ROM | Register /bit | Multiplexer /bit | Logic gates |
|---|---|---|---|
| Conventional | 64 × (6- bit) = 384 | 6 × (64×1) + (6×1) = 390 | 1536 + 780 = 2316 |
| Memory-less | --- | --- | 139 |

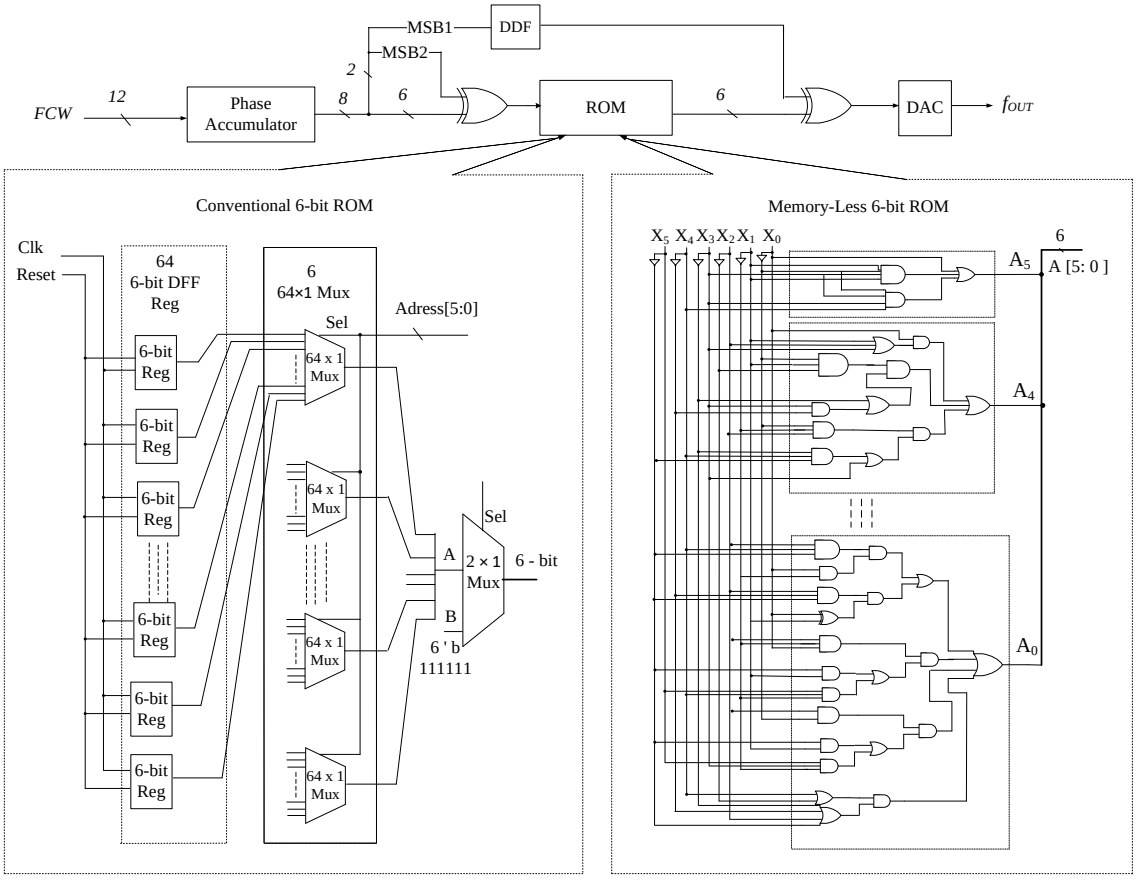



Figure 6. Conventional-memoryless 6-bit ROM circuit comparison

The 6-bit ROM requires 64 6-bit registers, six 64×1 multiplexers, and an extra 6×1 multiplexer to accomplish the sine amplitude waveform. The designed circuits of memory-less and conventional ROMs were synthesized in Synopsys software to obtain the optimized register transfer level (RTL) viewer, number of slices, and area dimension. Replacing the memory-less ROM circuit instead of conventional 6-bit ROM circuit reduces 56% of the lower area dimension and 32.6% of the number of cells. Table 2 shows the comparison of the number of cells, nets, and area dimension between the conventional ROM LUT and memory-less ROM. Comparison of the number of cells, nets, and area dimension of conventional and memory-less ROM.

Table 2. Comparison results of conventional and memory-less ROM logic gates

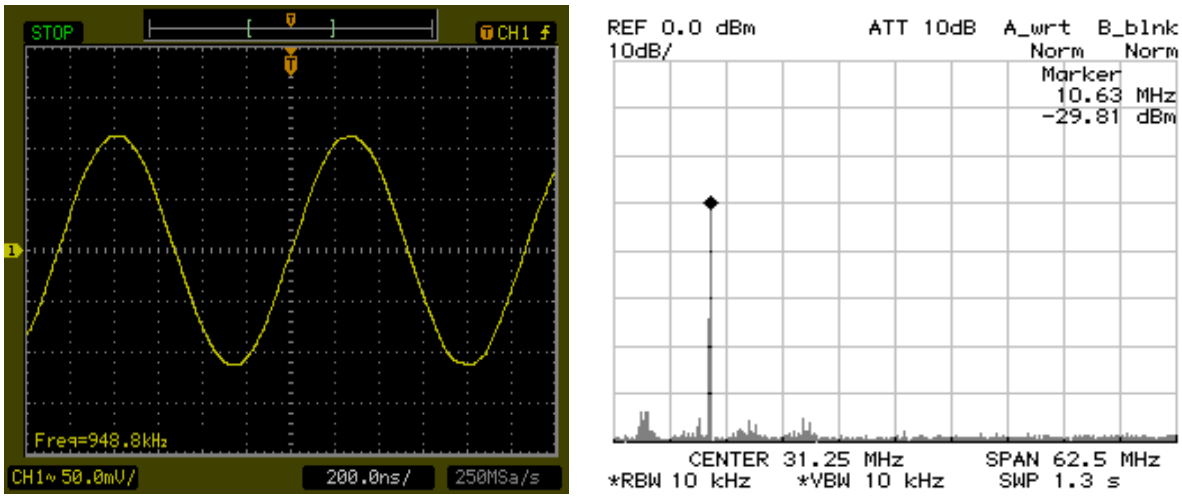
| (6-bit) ROM | No. Nets | No. Cells | Area (μm2) |
|---|---|---|---|
| Conventional | 98 | 106 | 2105.6112 |
| Memory-less | 66 | 72 | 924.739 |

## 4. RESULTS AND ANALYSIS

The proposed DDFS system was programmed on the Cyclone III FPGA kit board and connected to the DAC hardware. The measured results of the frequency waveform and spectrum shown in Figures 7(a) and (b), respectively, are consistent with the expected results. The signal-to-noise ratio (SNR) is mathematically calculated using the following equation:

$$SNR = 6.02M + 1.76\,dB \quad \text{[20-22]} \tag{8}$$

As shown in (8), the $SNR$ value depends on the number DAC input bits (M). M=6 bits in this study; hence, SNR=37.88 dB. The spectrum analyzer image shows that the measured DDFS output waveforms exhibit an SNR of approximately 45 dB as shown in Figure 7(b).




(a) (b)

Figure 7. (a) Sine waveform of the DDFS, (b) Measured SNR waveform of DDFS output

Table 3 presents the comparison of the ROM size technique, spurious-free dynamic range (SFDR), and additional hardware used in the proposed design with several other parameters. The proposed design has no (DFF register) ROM bit size. The comparison between the proposed DDFS system and previous works is given in Table 2.

Table 3. Comparison results of conventional and memory-less ROM logic gates

| Ref. | PA (bit) | Amp. | ROM Size (DFF (Reg.) | ROM Technique | Additional Hardware | SFDR (dB) |
|---|---|---|---|---|---|---|
| [4] | 11 | 9 | 368 | Quad Line Approximation Tech. | 5 Adders +1Mux + complementor | 55 |
| [5] | 9 | 6 | NA | ROM-DAC | NA | 35 |
| [6] | 9 | 8 | NA | ROM-Less | 3:8 thermometer decoder | 42 |
| [7] | 9 | 8 | NA | ROM-less | NA | 44 |
| [23] | 8 | 6 | 112 | Quadrat Decompos. Tech. | 1 Adder + 1 Multiplier + (3:8) Decoder | 30 |
| [24] | 12 | 9 | 224 | 2 Splitted ROM | NA | 40.7 |
| [25] | 8 | 6 | NA | Nonlinear DAC | 3:8 thermometer decoder | 37.5 |
| Proposed | 12 | 6 | 0 | Memory-Less ROM | 139 Logic cells + 6-bit DFF Register | 45 |

## 5. CONCLUSION

Multiple types of parallel prefix adders used in pipelined PA designed circuits are coded using Verilog HDL code and verified in Quartus II software. The KS-based PA outperforms other conventional PA architectures. Therefore, KS-based PA is used in this research to improve the PA throughput. In addition to the quarter wave symmetry that reduces 75% of the ROM size, the memory-less circuits have been applied as a novel approach for ROM design instead of the conventional 6-bit ROM. This technique replaces 384 DFF registers and multiplexers with 139 AND, OR, and XOR logic circuits, thereby reducing the lower area dimension and number of cells by 56% and 32.6%, respectively. The proposed DDFS system is coded in Verilog HDL, successfully simulated and implemented with Cyclone III FPGA kit board, and connected to the DAC circuit for verification using waveform and spectrum analyzer devices. The measured results of the frequency waveform and spectrum analyzer are compared with the expected results. These performances provide the present DDFS design with further flexibility for applications in wireless communication systems.

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