

Novel hybrid framework for image compression for supportive hardware design of boosting compression

Premachand D. R., U. Eranna

Department of Electronics and Communication Engineering, Ballari Institute of Technology and Management, Ballari, India

Article Info

Article history:

Received Nov 10, 2019

Revised Oct 12, 2020

Accepted Nov 1, 2020

Keywords:

Encoding
Hardware acceleration
Image compression
Segmentation
VLSI architecture

ABSTRACT

Performing the image compression over the resource constrained hardware is quite a challenging task. Although, there has been various approaches being carried out towards image compression considering the hardware aspect of it, but still there are problems associated with the memory acceleration associated with the entire operation that downgrade the performance of the hardware device. Therefore, the proposed approach presents a cost effective image compression mechanism which offers lossless compression using a unique combination of the non-linear filtering, segmentation, contour detection, followed by the optimization. The compression mechanism adapts analytical approach for significant image compression. The execution of the compression mechanism yields faster response time, reduced mean square error, improved signal quality and significant compression ratio performance.

This is an open access article under the [CC BY-SA](https://creativecommons.org/licenses/by-sa/4.0/) license.



Corresponding Author:

Premachand D. R.
Department of Electronics and Communication Engineering
Ballari Institute of Technology and Management
Ballari, India
Email: premchandbitm@gmail.com

1. INTRODUCTION

Performing different forms of processing over a complex form of an image is a challenging task when it comes to hardware-based implementation. In this aspect, image compression is one such process that significantly offers overhead in the hardware realization. All the problems starts with the memory system of the hardware component while processing large number of image pixels. It is believed that the performance of the memory management solely depends upon the pattern of its accessing mechanism. It is essential that analysis of the traces of the memory is required to be investigated in order to improve the memory management of the hardware. The image compression mechanism aims to optimize the size of image for smooth transmission and storage [1]. The presence of artifacts in the images can also remove through image compression [2]. But, there is challenging situation in achiving significant image compression for the area and enegy constrained devices [3].

In order to perform an efficient image compression, there are various conditions that are required to be catered up. The primary conditions to be satisfied are that the usage of lossless compression is important for resisting loss of traced data in memory system. The secondary condition to be satisfied is that there should be higher degree of throughput and increased speed for higher bandwidth suportabilty. With the increasing frequency of operation and the higher data bandwidth, there is a need of higher rate of throughput too. The main reason behind this is that in order to offer better analysis of memory traces there is a need of developing acceleration system of the compression with respect to hardware modeling and not the software-based symptomatic approach. Another important finding is that software-based compression approach is

always slower in comparison to the hardware-based compression approach that downgrades the compression performance. Therefore, there is a significant tradeoff between hardware-based approach and software-based approach in order to achieve the target of compression efficiency. The increased use of Internet-of-Things (IoT) can lead to more usage of resource constraint devices connected each other through different networks [4]. The image compression can be achieved through software/hardware based approaches [5-7].

Most of the software approaches are depended on vector multiplication and other matrix operations [8]. But, these operations are not feasible for the resource constrained devices due to increased computational complexity. The existing mechanisms are not much efficient to handle these problems and offer better support to provide hardware efficient solution for compression techniques [9, 10]. Hence, this paper offers a cost effective solution providing balance between signal quality and compression through hybrid compression technique in wireless sensor network (WSN). The section 2 of the paper explains the existing research analysis and problem description in section 3. The proposed technique along with the algorithm implementation is elaborated in section 5. The results discussion with comparative analysis is highlighted in section 6 and conclusion in section 7.

The study of various existing compression techniques for digital image is discussed in this section. In Cabronero *et al.* [11], a Hybrid compression approach is adapted for transformation-operation is carried out over colored mosaic image. A subjective optimization process with supervised learning algorithms is introduced in Amirjanov and Dimililer [12] over medical image. In Wang *et al.* [13], a line-buffer scheme is introduced for compression over the processing circuits. A work of Chen *et al.* [14] provided a color filter array along with an improved Golomb-Rice code to achieve significant on-chip compression. A hardware acceleration approach for integrated circuits compression is introduced in Halawani *et al.* [15]. Choi *et al.* [16] have considered hardware throughput approach for on-chip compression. A compression scheme for image sensors is presented in Kaur *et al.* [17] by using interpolation operation over the on-chip hardware design. In Onishi *et al.* [18], a multimedia encoder approach is introduced over single-chip design and achieved scalable compression process. The implementation of transform-based compression scheme for compression is described in Zhu *et al.* [19] by using block coding.

A VLSI architecture with tree-based approach for towards image encoder based compression is given in Hsieh *et al.* [20]. An energy efficient implementation of VLSI architecture for image compression is introduced in Chen *et al.* [21] considering ultra-high definition frame. Gradient-based approach towards improving compression performance is seen in the work of Kim *et al.* [22]. Lucas *et al.* [23] have used predictive-based scheme for the purpose of performing lossless compression scheme. The work carried out by the Yin *et al.* [24] have used an integral histogram based approach to accelerate the mechanism of the feature extraction process for controlling better computational operation over the memory access in hardware. Parikh *et al.* [25] have used latest encoders for performing maximized compression performance for the complex form of an image. The study has used the partitioning process for better memory management during compression over parallel architecture. Adoption of color filter array was also proven to be better solution for performing compression especially in the case of application that demands live compression operation to be taking place. Work in this direction has been carried out by Chen *et al.* [26] where Golomb Rice is considered for implementation for enhancing the compression efficiency. The problems associated with color compression is carried out by Peter *et al.* [27] where the authors have used diffusion-based approach along with inpainting phenomenon for offering superior quality of reconstructed image.

Zhang *et al.* [28] where a definitive transformation scheme has been presented. This approach has been presented for the upgrading the existing JPEG compression performance. Therefore, there are various approaches towards image compression where hardware approach has been considered. Study focusing over the energy efficiency as well as constraint area of the circuit design connecting with the concept of image compression has been discussed by Zeinolabedin *et al.* [29]. Kim *et al.* [30] has used encoding-based approach for carrying the compression operation where the preliminary encoding computes the bitstream length while the secondary encoder is responsible for generation of streams of the data packets over VLSI architecture. Study considering the VLSI architecture towards the compression approach has been carried out by the next section outlines the research issues.

The overview of existing studies suggests that the compression schemes are failed to adopt the VLSI implementation effectively. Some of the research issues are:

- Lack of hardware efficient schemes to minimize computational complexity
- Least consideration of filtering process in low-quality image compression
- Complete selection of signal processing is not considered in previous works
- Insignificant selection of compression features to yield cost effectiveness solution

The study develops the computational model to address the above stated research problems. The flow of the proposed compression approach is illustrated in Figure 1. The proposed system adapts analytical

approach where input image is processed for cost effective image compression. The significant aspect of this solution is that it follows hybrid compression technique of lossless and lossy compression over selected image sector and compression over regions of the image respectively.

The proposed system makes use of the simplified modeling that initiates by performing filtering operation. This operation assists in eliminating possibility of any further artifacts that could be possibly present during the transmission process of the image in the wireless communication medium. The filtered image is subjected to next process where uniquely not the complete image is subjected to the compression. The complete image is hypothetically classified into two parts where one sector of the image is considered to be critically important whereas other part of the image is not that important. From application as well as communication viewpoint, it is essential that important sector the image is subjected for lossless compression scheme while the not so important part of an image is subjected to the lossy compression scheme. The proposed scheme uses contours detections and optimization process. Another essential part of the implementation of the proposed system is its segmentation process and the contour detection process. This process contributes towards the extraction of the features that is used for minimizing the dimensions of an image. This characteristics of the contours are further optimized where concatenation operation is carried out over the extracted red green and blue components of an image which maintains similar dimensions of an image but with more effective information of the contours. The finally obtained optimized contours are subjected for the wavelet compression this renders the process of compression acceleration swifter over the hardware. The next section discussion of the all the essential process blocks shown in Figure 1.

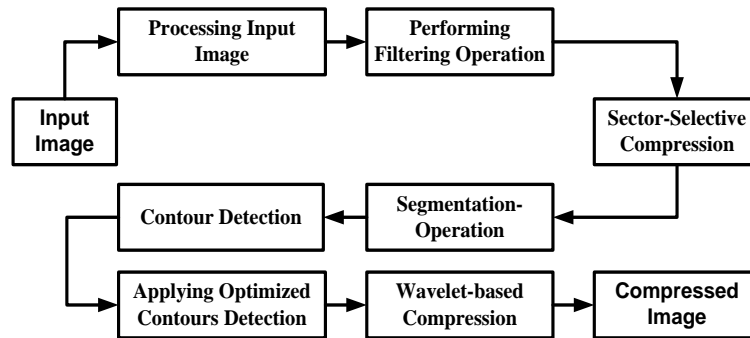


Figure 1. System architecture

2. DESIGN PRINCIPLE OF IMPLEMENTATION

Design plays a significant role in developing architecture. It should be noted that an effective design for VLSI architecture demands a suitable computational model that performs management and structurization of all the processes in efficient manner. This section briefs strategies followed in image compression where it maintains reconstructed image quality and computational complexity. The quality image is considered to transmit in the *primary assumption* and it is characterized with artifacts. The elimination of the artefacts are considered *secondary assumption* by upgrading new compression process. The lossless compression is aimed in *tertiary assumption* over specific region of image.

2.1. Strategy for Implementation

The proposed system planned stragically to provide the cost effective image compression and obtain the quality image after decompression. To achive this, some part of the image are considered to select the sector of the image for compression. The strategy also offers better approach for hardware viewpoint, where the memory allocations over the hardware image compression is considered that can reduce the complexity. The algorithm able to provide the compressed image with following steps:

Algorithm of sector-selective compression approach

Input: Input Image (I)

Output: Compressed image (ϕ)

Start

Step-1: initialize \rightarrow I

Step-2: $K \leftarrow f_1(I)$

Step-3: $I_4 \leftarrow f_2(I)$

Step-4: $BW \rightarrow f_3(I_4)$

Step-5: $R \rightarrow$ concatinate (r_1 g_1 b_1)

Step-6: $C_r \rightarrow$ concatinate (r g b)
 Step-7: $C_p \rightarrow$ concatinate (R G B)
 Step-8: $\phi \rightarrow f_4(C_p)$
End

The algorithm is expressed as below:

- a. Input image processing: The matrix (I) is generated after processing image for digitization (Step-1) by converting RGB to greyscale image (image processing stages are illusted in Figure 2).

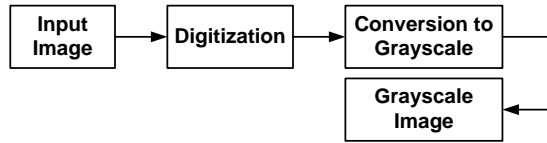


Figure 2. Stages of input image processing

- b. Filtering process: This process is applied to eliminates the noise in the image before subjecting to compression. A function $f_1(x)$ is introduced to perform non-linear filtering that also improves the image processing stage (Step-2) (Non linear filtering stages are given in Figure 3).



Figure 3. Stages of non-linear filtering

- c. Sector-selective compression: This kind of compression is achieved through specific sector of image (I) and is need to go lossless compression while sector subjected to lossy compression. This combination of compression technique helps to exteact the significances of both techniques which eliminates the issues of the compression process. The manual section of the sector is critical concern and it can be eliminated by formulating the function $f_2(x)$ that does the automated sector selection (Step-3). The algorithm applies involuntary thresholding on image (I) and then converts it into binary form. The process results an image (I₄) after multiplication of threshold image (The process of this process is illustrated in Figure 4).

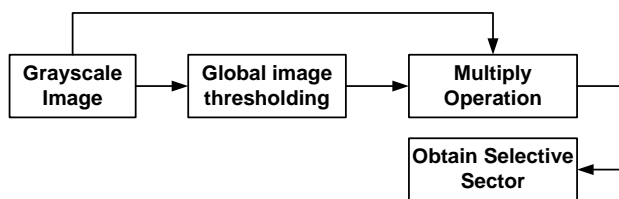


Figure 4. Stages of sector selective compression

- d. Segmentation-operation: To the selected image sectors (I₄), the segmentation process is applied (Step-4) where explicit function $f_3(x)$ is used for multi-scale segmentation operation. The function " $f_3(x)$ " uses fuzzy *c*- clustering for binarized image "I₄". Later, summation of all the pixel labels is performed. Finally, the segemented image parts are combined through multiplication and it will helps to generate the segmented image (BW) (The segementation process is represented in Figure 5).

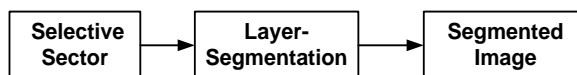


Figure 5. Stages of segmentation operation

- e. Contour detection: During this stage, a matrix is formed to retain the corner metric obtained for the input image and is considered for feature extraction (Step-5). An index is constructed after finding the positive corner sets. Further, the inputs and outputs are matched to form the red (r_1), green (g_1), and blue (b_1) components. The “r1” components are initiated with 255 and other components like “g1” and “b1” are initialized with 0. Further, these components are concatenated to get the actual corner points “R”. During each stage maximum regions of the image are identified to detect the peaks of the corners. Further, the input and outputs are matched by which the new components of the “r”, “g” and “b” components are concatenated to get the suppressed corner (C_r) points (Step-6). The contour detection algorithm is also used to multiply the grayscale image with the contour index so that the contours of complete image can be generated (Stages of this implementation is given in Figure 6).

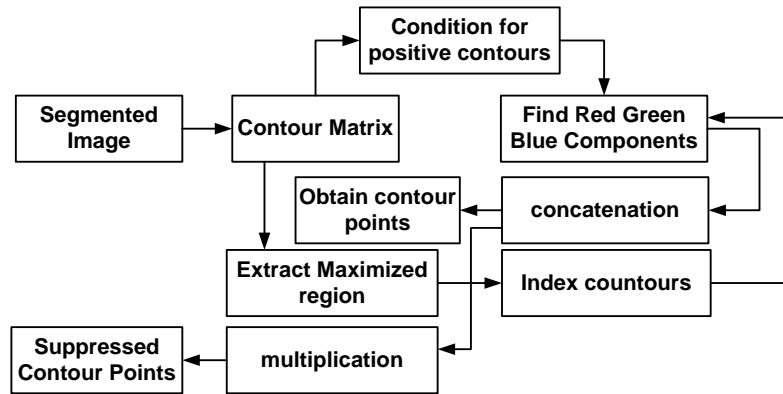


Figure 6. Stages of contour detection

- f. Optimized contours detection: The performance of the contour detection is optimized in this part of the implementation. During this, the prior information of contour matrix will be accessed and then an S-shaped curve function is producing the individual matrix. The values between probability limit is collected for the concatenation of final contours leading to optimized contour points (C_p) (Step-7). The final process of compression is to apply wavelets where function $f_4(x)$ is considered over the image with contour points (C_p). The operation helps to generate the final form of compressed image ϕ (Step-8) and this process is shown in Figure 7.

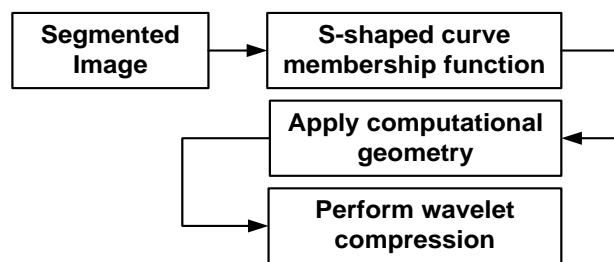


Figure 7. Stages of optimized contours detection

3. RESULT ANALYSIS

The core idea of the outcome analysis is to ensure that proposed computational model should offer streamlined facilitation for the hardware realization of the image compression. A part of the image is considered for the lossless compression over different forms of images. The visual results of the filtered image (after applying non-linear filter), sector image, multi-scale segmented image, contour detection and optimized counter is given in Figure 8. The analysis of the system is performed for both selective regions and for complete image by considering Mean Square Error (MSE), Peak Signal-to-Noise Ratio (PSNR) and Compression Ratio (as represented in Figures 9-11 respectively).

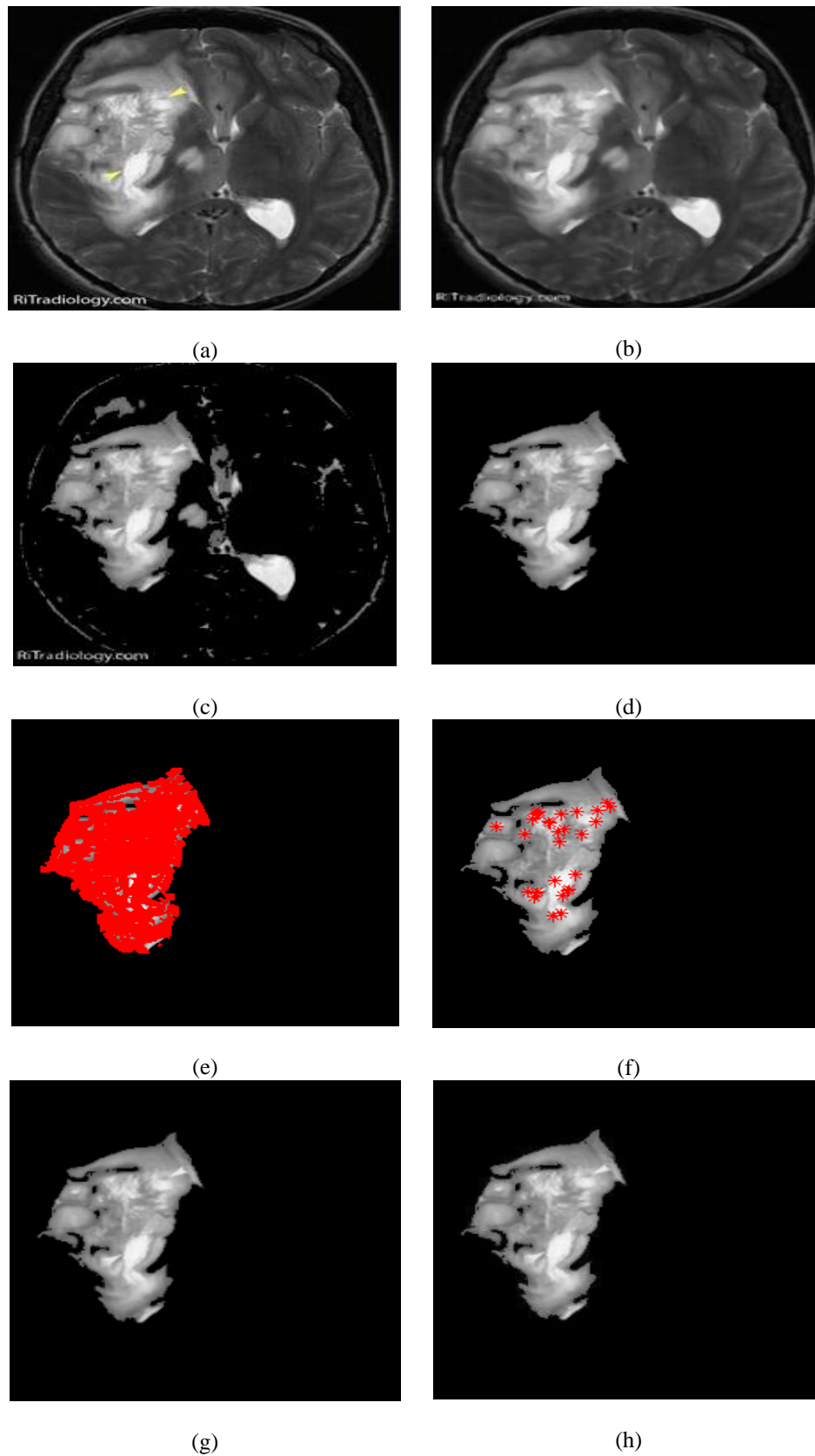


Figure 8. Visual outcomes of sample image, (a) original image, (b) filtered image, (c) selected sector, (d) segmented image, (e) contour points, (f) fuzzy corner points, (g) optimized compression, (h) wavelet compression

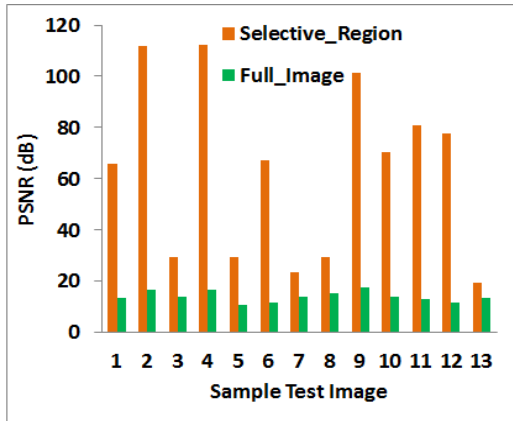


Figure 9. PSNR performance

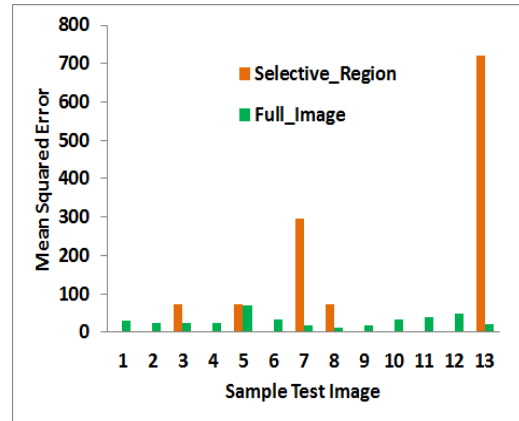


Figure 10. Mean squared error performance

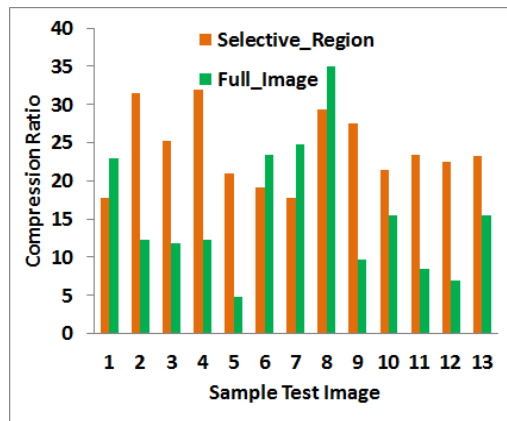


Figure 11. Compression ratio

The analysis of above factors indicates that the PSNR performance of system is improved in SR than FI. The signal quality of the system also improved at reduced dimension. The algorithm takes about 0.9877secs to respond to the execution which is considered as instantaneous to offer cost effective solution for the compression operations.

4. CONCLUSION

This paper has presented a discussion of the computational model for facilitating hardware acceleration while performing image compression. The significant contribution of this paper is to bridge the trade-off between the hardware-based and software-based compression acceleration process with respect to the VLSI architecture. The contributions of the proposed system towards the image compression are as follows: i) the proposed system is cost effective as it doesn't use complete resource for compression as only the selective sector is subjected for the lossless compression, ii) the proposed system is also cost effective as the compression is carried out over the lightweight contour feature that not only offers storage optimization but also retains better signal quality, and iii) the implementation of the proposed system doesn't include maximum dependencies of resource to carry out the task.

REFERENCES

- [1] T. Lin and P. Hao, "Compound image compression for real-time computer screen image transmission," *IEEE transactions on Image Processing*, vol. 14, no. 8, pp. 993–1005, 2005.
- [2] H. G. Myung, J. Lim, and D. J. Goodman, "Single carrier FDMA for uplink wireless transmission," *IEEE Vehicular Technology Magazine*, vol. 1, no. 3, pp. 30–38, 2006.
- [3] N. Javaid, Z. Abbas, M. S. Fareed, Zahoor Ali Khan, and N. Alrajeh, "M-ATTEMPT: A new energy-efficient routing protocol for wireless body area sensor networks," *Procedia Computer Science*, vol. 19, pp. 224–231, 2013.

- [4] B. Guo, D. Zhang, Z. Wang, Z. Yu, and X. Zhou, "Opportunistic IoT: Exploring the harmonious interaction between human and the internet of things," *Journal of Network and Computer Applications*, vol. 36, no. 6, pp. 1531–1539, 2013.
- [5] L. Atzori, A. Iera, and G. Morabito, "Siot: Giving a social structure to the internet of things," *IEEE communications letters*, vol. 15, no. 11, pp. 1193–1195, 2011.
- [6] R. M. Dyas and B. Tang, "Software, method and apparatus for rate controlled image compression," U.S. Patent 6,504,494, Jan. 7, 2003.
- [7] S. J. Wee and M. P. Schuyler, "Image compression featuring selective re-use of prior compression data," U.S. Patent 6,697,061, Feb. 24, 2004.
- [8] S. Chatterjee and S. Sen, "Cache-efficient matrix transposition," in *Proceedings Sixth International Symposium on High-Performance Computer Architecture, HPCA-6* (Cat. No. PR00550), 2000, pp. 195–205.
- [9] J. L. Bentley, D. D. Sleator, R. E. Tarjan, and V. K. Wei, "A locally adaptive data compression scheme," *Communications of the ACM*, vol. 29, no. 4, pp. 320–330, 1986.
- [10] A. Jas, J. Ghosh-Dastidar, M. E. Ng, and N. A. Touba, "An efficient test vector compression scheme using selective Huffman coding," *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 22, no. 6, pp. 797–806, 2003.
- [11] M. Hernández-Cabrero, V. Sanchez, I. Blanes, F. Aulí-Llinàs, M. W. Marcellin and J. Serra-Sagristà, "Mosaic-Based Color-Transform Optimization for Lossy and Lossy-to-Lossless Compression of Pathology Whole-Slide Images," in *IEEE Transactions on Medical Imaging*, vol. 38, no. 1, pp. 21–32, Jan. 2019.
- [12] K. Dimililer and A. Amircanov, "Image Compression System with an Optimisation of Compression Ratio," *IET Image Processing*, vol. 13, 2019.
- [13] H. Wang, T. Wang, L. Liu, H. Sun, and N. Zheng, "Efficient Compression-Based Line Buffer Design for Image/Video Processing Circuits," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 10, pp. 2423–2433, Oct. 2019.
- [14] C. Chen, S. Chen, C. Liao, and P. A. R. Abu, "Lossless CFA Image Compression Chip Design for Wireless Capsule Endoscopy," in *IEEE Access*, vol. 7, pp. 107047–107057, 2019.
- [15] Y. Halawani, B. Mohammad, M. Al-Qutayri, and S. F. Al-Sarawi, "Memristor-Based Hardware Accelerator for Image Compression," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 12, pp. 2749–2758, Dec. 2018.
- [16] J. Choi, B. Kim, H. Kim, and H. Lee, "A High-Throughput Hardware Accelerator for Lossless Compression of a DDR4 Command Trace," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 1, pp. 92–102, Jan. 2019.
- [17] A. Kaur, D. Mishra, S. Jain, and M. Sarkar, "Content Driven On-Chip Compression and Time Efficient Reconstruction for Image Sensor Applications," in *IEEE Sensors Journal*, vol. 18, no. 22, pp. 9169–9179, Nov. 2018.
- [18] T. Onishi *et al.*, "A Single-Chip 4K 60-fps 4:2:2 HEVC Video Encoder LSI Employing Efficient Motion Estimation and Mode Decision Framework With Scalability to 8K," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 1930–1938, Oct. 2018.
- [19] Z. H. Zhu, X. Meng, J. Zhou, and B. Zeng, "Compression-Dependent Transform-Domain Downward Conversion for Block-Based Image Coding," in *IEEE Transactions on Image Processing*, vol. 27, no. 6, pp. 2635–2649, Jun. 2018.
- [20] J. Hsieh, M. Shih, and X. Huang, "Algorithm and VLSI Architecture Design of Low-Power SPIHT Decoder for mHealth Applications," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 6, pp. 1450–1457, Dec. 2018.
- [21] Q. Chen, H. Sun, and N. Zheng, "Worst Case Driven Display Frame Compression for Energy-Efficient Ultra-HD Display Processing," in *IEEE Transactions on Multimedia*, vol. 20, no. 5, pp. 1113–1125, May. 2018.
- [22] K. Kim, C. Lee, and H. Lee, "A Sub-Pixel Gradient Compression Algorithm for Text Image Display on a Smart Device," in *IEEE Transactions on Consumer Electronics*, vol. 64, no. 2, pp. 231–239, May. 2018.
- [23] L. F. R. Lucas, N. M. M. Rodrigues, L. A. da Silva Cruz, and S. M. M. de Faria, "Lossless Compression of Medical Images Using 3-D Predictors," in *IEEE Transactions on Medical Imaging*, vol. 36, no. 11, pp. 2250–2260, Nov. 2017.
- [24] S. Yin, P. Ouyang, T. Chen, L. Liu, and S. Wei, "A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 4, pp. 1305–1318, Apr. 2016.
- [25] S. S. Parikh, D. Ruiz, H. Kalva, G. Fernández-Escribano, and V. Adzic, "High Bit-Depth Medical Image Compression With HEVC," in *IEEE Journal of Biomedical and Health Informatics*, vol. 22, no. 2, pp. 552–560, Mar. 2018.
- [26] S. Chen, T. Liu, C. Shen, and M. Tuan, "VLSI Implementation of a Cost-Efficient Near-Lossless CFA Image Compressor for Wireless Capsule Endoscopy," in *IEEE Access*, vol. 4, pp. 10235–10245, 2016.
- [27] P. Peter, L. Kaufhold, and J. Weickert, "Turning Diffusion-Based Image Colorization Into Efficient Color Compression," in *IEEE Transactions on Image Processing*, vol. 26, no. 2, pp. 860–869, Feb. 2017.
- [28] S. Zhang, X. Tian, C. Xiong, and J. Tian, "Unified VLSI architecture for photo core transform used in JPEG XR," in *Electronics Letters*, vol. 51, no. 8, pp. 628–630, Apr. 2015.

- [29] S. M. A. Zeinolabedin, J. Zhou, X. Liu, and T. T. Kim, "An Area- and Energy-Efficient FIFO Design Using Error-Reduced Data Compression and Near-Threshold Operation for Image/Video Applications," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 11, pp. 2408–2416, Nov. 2015.
- [30] S. Kim, M. Kim, J. Kim, and H. Lee, "Fixed-Ratio Compression of an RGBW Image and Its Hardware Implementation," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 6, no. 4, pp. 484–496, Dec. 2016.

BIOGRAPHIES OF AUTHORS



Premachand D. R., currently working as Associate Professor, Department of Electronics and Communication Engineering, Ballari Institute of Technology and Management, Karnataka, India. He has industrial experience of 2 years and teaching experience of 17 years. He has nearly published 3 journals and 3 conference paper. His areas of interest are in VLSI, Image processing and Micro electronics.



Dr. U. Eranna, currently working as Professor and HOD in the Department of Electronics and Communication Engineering, Ballari Institute of Technology and Management. He has published 8 conference papers and 20 journal papers. His area of research was Communication, Control System.