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A new structure of a wide band bridge power limiter

Khalifa Echchakhaoui[1], Elhassane Abdelmounim[2], Jamal Zbitou[3], Hamid Bennis[4]
[1,2]ASTI Laboratory FSTS, Hassan 1st University, Morocco
[3]LMEET Laboratory, FST of Settat, Hassan 1st University, Morocco
[4]Graduate School of Technology of Meknes, Moulay Ismail University, Morocco

Article Info

ABSTRACT

In this work, new design and simulation of a microstrip power limiter based on Schottky diode is presented. The proposed circuit is a zero bias power limiter built by associating a transmission line in parallel to a four Schottky rectifier bridge circuit. The first circuit using a single stage rectifier is analyzed and simulated. To improve this single stage, a second and final limiter is designed with two stages rectifier. Simulation results for the final circuit show an ideal limiter behavior and good performance of limiting rate up to 20dB for a threshold input power varying from 5 dBm to 30 dBm. While insertion loss remains low at small signal.

Corresponding Author:

Khalifa Echchakhaoui,
ASTI Laboratory,
Faculty of Sciences and Techniques,
Hassan 1st University, Settat, Morocco.
Email: k.echakhaoui@gmail.com

1. INTRODUCTION

In Microwave systems, Power limiters prevent high incident signal from saturating or damaging sensitive receivers such as rectenna systems and low noise amplifier [1-5] and also allow the receiver to function properly in presence of small signals. The most used limiter technologies are based on solid state components such as PIN diodes [6-8], FET transistors [9-12], and Schottky diodes [13-16]. Other solutions to achieve power limiters are provided by MEMS components [17], vacuum diodes [18] and gas discharge tubes [19].

In this work, commercial HSMS286B Zero-Bias Schottky diode [20] are used to design a low cost microstrip power limiter operating at a frequency of 2.45 GH. The proposed power limiter can reduce the amplitude of a large input signal of 30 dBm by 10 to 20 dB. Two types of microwave limiter can be distinguished: active power limiter that requires external current and self-biased limiter operating without DC bias.

The proposed microwave limiter is a self-biased limiter built on two microstrip lines. The first linear line transmits the main signal while the other line is associated to a rectifier bridge constituted of four Schottky diodes. When an incoming signal exceeds Schottky diodes threshold, the rectifier bridge is self-biased causing the drop of diodes impedance and consequently a portion of incoming signal is diverted to ground. The designed circuit has been optimized to provide more than 15dB attenuation rate at high signal power while assuring a minimum insertion loss at small signal state.

2. DESIGN APPROACH

A simplest solid state limiters consists of one stage diodes or MESFET transistors connecting a line transmission to ground as presented in Figure 1 [21]. In order to take advantage of the variation of its

impedance as a function of the electric current flowing through it, the diode used to limit the power is placed in anti-parallel form between the transmission line and the common ground. Consequently, when the input power increases, the diode impedance drops down, and some of the received power is diverted to ground. These limiters must present minimal losses for incoming signals under certain threshold power, however beyond this threshold level, losses must be proportional to the incident power [22].
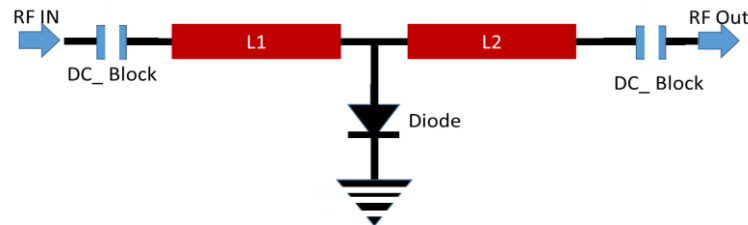

Figure 1. Basic power limiter topology

Such circuit must be equipped with a bias voltage which allows the diode or the MESFET transistors to switch to forward state. The implementation of a bias voltage in microwave system could generate noise and be a source of uncontrolled behavior. However, it is possible to generate the necessary DC biasing current by choosing Zero-Bias diodes [21, 22] and using a detector diode as shown in Figure 2. The detector diode will transform a part of incident signal to DC current as used in rectenna systems [23, 24]. On the other hand, the return DC current is ensured by an RF Choke or by the limiter diode itself.
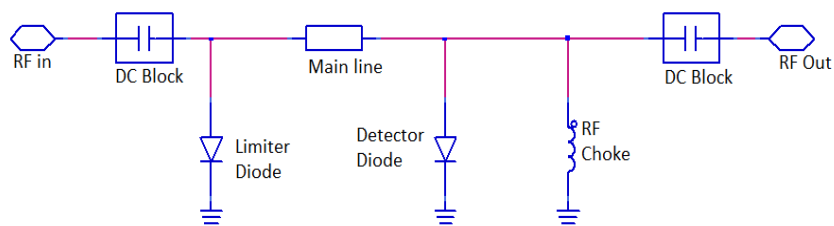

Figure 2. Toplogy of zero bias limiter

In the proposed circuit, we use full wave rectifier bridge circuit topologies optimized for microwave circuit operating at ISM band and using four Schottky diodes. This technique is widely used for rectenna systems and for remote energy harvesting [25, 26] and power detector [27]. As mentioned previously, we chose the Avago HSMS286B commercial diode for validation and design of the proposed circuit. This diode is a surface-mount Schottky RF diode presented in the SOT23/143 package [20].

The HSMS286x family data sheet shows that these diodes are optimized for RF applications from 915 MHz to 5.8 GHz. They are used for large signals detection, modulation and rectification of RF signals [20, 24]. Since Advanced Design System (ADS) software is suitable for RF design and natively contains the different HSMS286x families in its library, we used it to validate and simulate the proposed circuit. We validated two circuits in terms of frequency band, insertion loss in small signal mode and attenuation rate when the power received exceeds the threshold limit of the limiter. The circuit is designed by using microstrip technology, based on FR4 substrate with the following parameters:
- Relative dielectric constant: 4.4
- Substrate thickness: 1.6mm
- Dielectric Loss tangent: 0.025

3. CIRCUIT OPERATION
The proposed circuit introduces a new design of a solid state power limiter. The circuit uses a power divider of two lines: The main transmission line in parallel with a second line where we insert a full wave bridge rectifier as depicted in Figure 3.
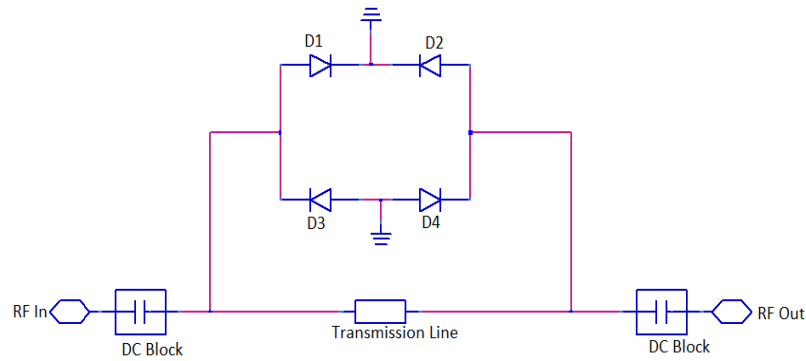
Figure 3. New designed topology

At low power incoming signal, the Schottky diode impedance remains very high because the bridge doesn't activate the rectification. Consequently, the input signal is transmitted to the load with a minimum insertion loss. When the circuit is exposed to a high amplitude signal which exceeds the detection threshold of the Schottky diode, a DC current generated will force the diode impedance to drop down. As a result, part of the incident signal is deflected to the ground.

In order to increase the attenuation level of the circuit, the length of the central line is chosen equal to half wavelength while the diodes are implanted at a distance of half wavelength from the point of derivation. This structure makes a phase shift of $3\lambda/2$ between the signal crossing the main transmission line and the signal crossing the rectifier bridge. The microstrip layout of the circuit is illustrated below in Figure 4.
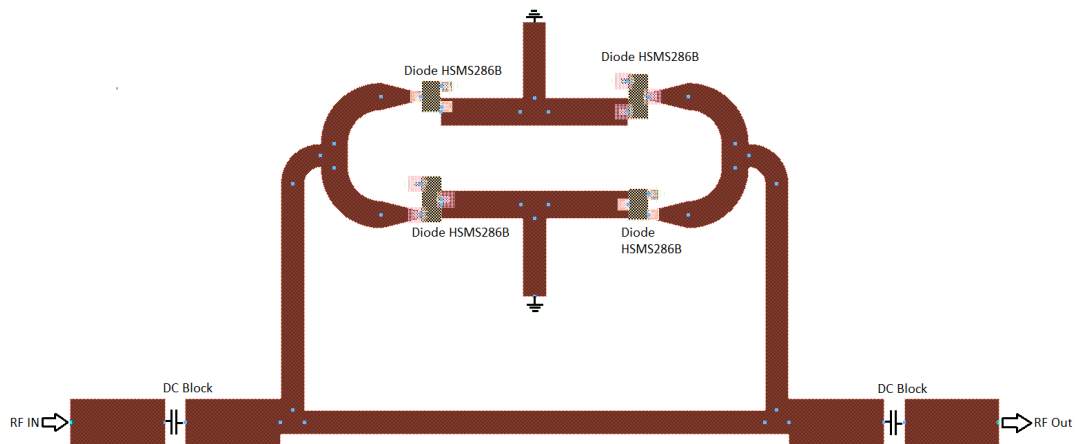

Figure 4. Microstrip structure of the circuit

3.1. Modelisation of rectifier structures

Rectifiers are implemented in this limiter circuit to generate DC current required to bias Schottky diode. Generally, RF-DC conversion circuits are based on Schottky diodes. Schottky diodes are selected due to their low junction capacity and low threshold voltage. To analyze the rectifier structure, we consider the equivalent layout of the second line as presented in Figure 5.

Before analyzing this circuit, we need to replace Schottky diodes D1 to D4 by their equivalent lumped circuit. When diodes D1 and D3 receive a positive half cycle Up*sin(ωt), D2 and D4 will be under negative half cycle Up*sin(ωt+π) because the distance between D1 and D2 is equal to $\lambda/2$. Since D1 and D2 are in opposite each to other, they will both be in forward bias, while D3 and D4 will be in reverse bias. This above description will be applied for the negative cycle of the signal reaching the diodes D1 and D3. In this situation, diodes D3 and D4 will be the forwarding state and the diodes D1 and D2 will be in the reverse state.

In conclusion, the full wave bridge can be replaced by two diodes at forwarding state and two diodes at reverse state. Hence the bridge in Figure 5 is equivalent to the circuit presented in Figure 6. In Figure 6,

Z_F stands for the equivalent impedance of Schottky diode at forwarding state and Z_R stands for the equivalent impedance of Schottky diode at reverse state. Figure 7 shows a simplified equivalent circuit of a Schottky diode in forward and reverse bias state.
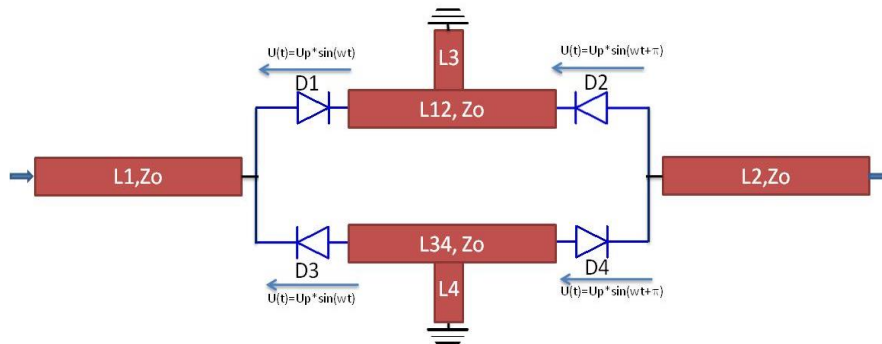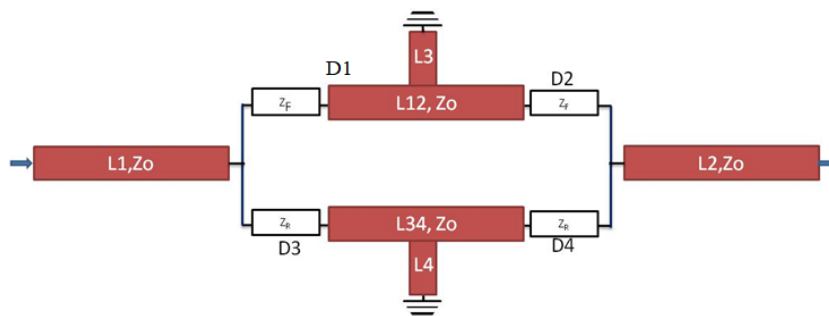

Figure 5. Second line layout
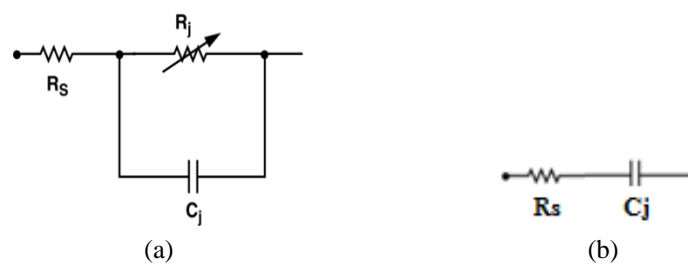

Figure 6. Equivalent circuit of full wave bridge

Figure 7. Simplified equivalent circuit of Schottky diode under (a) forward and (b) reverse bias

Where:
R_s: series resistance
R_j: variable resistance as a function of current flowing through the diode
C_j: the junction capacity

4. SIMULATION RESULTS
4.1. Circuit with one stage

The circuit presented in Figure 4 has been optimized and validated using ADS software. Figure 8 shows the s-parameters simulation. The output power versus input power is presented in Figure 9. At an input power of 30dBm, the limiting rate is almost 12dB.
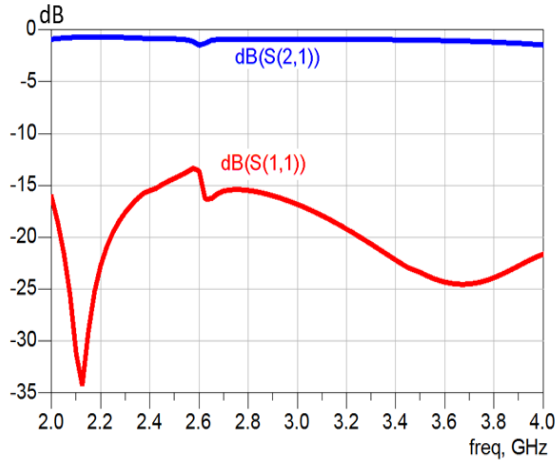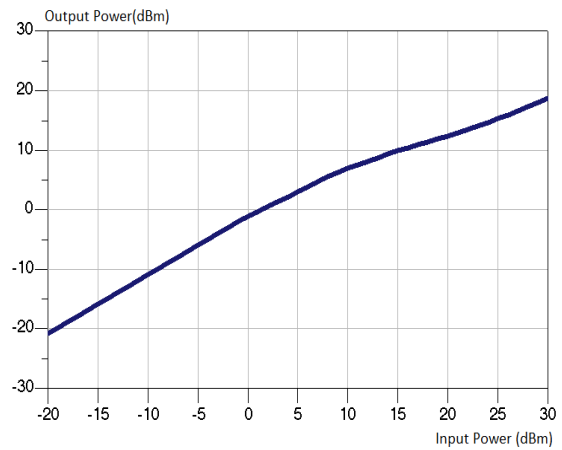
Figure 8. S-parameters simulation

Figure 9. Output power versus Input power at 2.45 Ghz

S-parameters simulation illustrated in Figure 5 shows that the limiter has good matching input impedance in the ISM band. The insertion loss is established at approximately 0.9 dB from 2 to 4 GHz. However, this structure has certain limitations:
-    High limiting power threshold: the device block high power input signal it reaches 10dBm.
-    Attenuation obtained at large signal (12 dB at Pin=30 dBm) is not sufficient to protect sensitive devices.
In order to overcome the above mentioned limitations, we have designed a second circuit consisting of two rectifying bridges.

4.2. Circuit with two stages
The improved circuit is formed by two rectifier bridges in parallel with a microstrip transmission line. However, the antidopal lines are replaced by a semicircle in order to reduce circuit dimension. The final circuit is presented in Figure 10. The S-parameters results simulations at small signal and limiting characteristics simulations at high input power are presented in Figure 11.
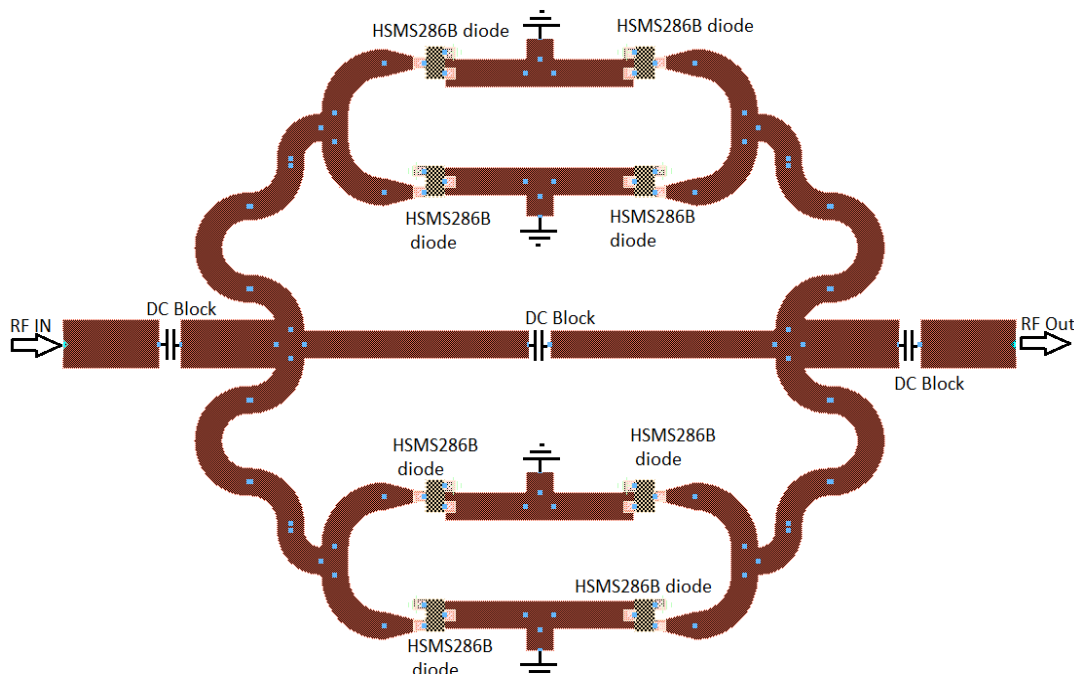

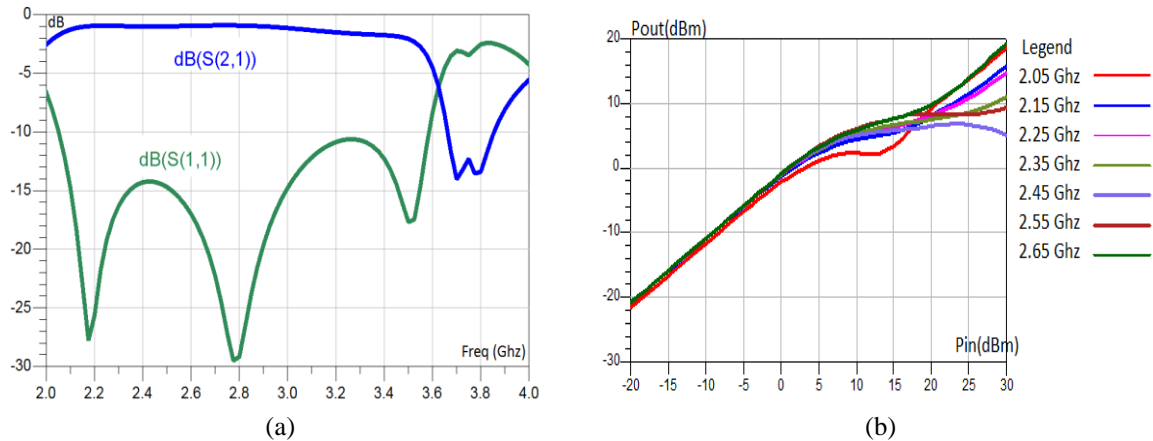Figure 10. Final circuit with two rectifiers bridges (2 stages)

Figure 11. (a) S-parameters simulation (b) Output Power vs Input Power at [2.05, 2.65] GHz

The two-stage circuit has a better isolation rate compared to the single-stage circuit, while the insertion loss remains in the same level:
- Broadband frequency range of 1GHz from 2 to 3.6 GHz
- Low insertion loss (-0.9 dB)
- The isolation rate reaches 23 dB at 2.45 GHz.

5. COMPARISON TO SIMILAR LIMITER IN LITERATURE

Table 1 summarizes a comparison of the proposed circuit with similar limiters reported in scientific literature. It can be seen that the circuit proposed in this paper achieves a small-signal insertion loss below 1 dB and an attenuation up to 23 dB over 1.6 GHz frequency band. In terms of power management, the proposed circuit supports 30 dBm exceeding the performance of MMIC circuits. The proposition in [28] presents nearly similar limitation rate, but with a very small bandwidth (300 MHz). While propositions in [29] and Zhou et al., present MMIC limiters with a high reflection rate and low limitation rate compared to the proposed circuit [30].

Table 1. Comparison between the proposed circuit and similar circuits in literature

	The proposed circuit	Reference [28]	Reference [29]	Reference [30]
Description and devices used	Planar circuit based on Schottky diode	Contiguous-Channel Double Multiplexer Topology.	180 nm SiGeBiCMOS Technology	Balanced Limiter associated to Low Noise Amplifier chip
Frequency band	2-3.6 GHz	1-1.3 GHz	4-6 GHz	8-12GHz
Insertion loss	-0.9 dB	-1.8 dB	-2 dB	NA
Reflection rate	-11 dB	-15 dB	-10 dB	-7.8 dB
Limitation rate	23 dB	22 dB	13.6 dB	NA
Maximum input power	30 dBm	30dBm	20 dBm	43 dBm

6. CONCLUSION

In this work, we have designed and validated by simulation two microstrip microwave power limiter circuits based on Zero-Bias Schottky diodes. At small signal power, the limiter based on one stage rectifier bridge permits a very low insertion loss around 0.9 dB over 2-4GHz. At High power input, this circuit presents a limitation of 12dB. To improve the isolation at high signal, a two rectifier bridge stages limiter has been designed and validated. This limiter presents quasi-ideal limiting power characteristic and achieves 23 dB of isolation rate and a limiting power threshold observed at 0dBm. The dimensions of the layout generated for this circuit are 58.54 mm x 37.05 mm.

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BIOGRAPHIES OF AUTHORS

Khalifa Echchakhaoui was born in BenGuérir, Morocco, in 1971. He is a Ph.D. student. His research interests include modeling, design and realization of microwave power control and protector systems.He received the Engineer degree in Computer Science and Telecommunication from the National Post and Telecommunication Institute, Rabat, Morocco, in 1995. He is currently Responsible of Core engineering Department at Morocco Telecom. He is involved in the design and evolution of Mobile Networks Solution and the implementation of 5G technology.

Elhassane Abdelmounim received his PhD in applied Spectral analysis from Limoges University at science and technical Faculty, France in 1994. In 1996, he joined, as Professor, the applied physics department of the science and technical faculty of Hassan 1st University, Settat, Morocco. His current research interests include digital signal processing and machine learning. He is currently coordinator of a Bachelor of Science in electrical engineering and researcher in "ASTI" System Analysis and Information Technology Laboratory at science and technical faculty, Hassan 1st University, Settat, Morocco.

Jamal Zbitou was born in Fes, Morocco, in June 1976. He received the Ph.D. degree in electronics from Polytech of Nantes, the University of Nantes, Nantes, France, in 2005. He is currently an associate Professor of Electronics in FST, University Hassan 1st, Settat, Morocco and the head of Computing Networks and telecommunication in LMEET Laboratory in FSTS. He is involved in the design of hybrid, monolithic active and passive microwave electronic circuits.
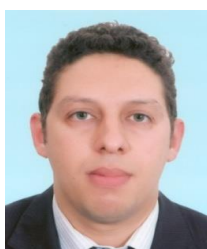
Hamid Bennis was born in Meknes, Morocco, in September 1977. He received the Ph.D. degree in Computer Science and Telecommunication from the University of Mohammed V Agdal, Rabat, Morocco, in 2011.He is currently a Professor of Computer Science and Computing Network in Graduate School of Technology of Meknes (EST-Meknes), Moulay Ismail University, Meknes, Morocco. He is involved in the design of hybrid, monolithic active and passive microwave electronic circuits.