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Design and analysis of optimized CORDIC based GMSK system on FPGA platform

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ABSTRACT

The gaussian minimum shift keying (GMSK) is one of the best suited digital modulation schemes in the global system for mobile communication (GSM) because of its constant envelop and spectral efficiency characteristics. Most of the conventional GMSK approaches failed to balance the digital modulation with efficient usage of spectrum. In this article, the hardware architecture of the optimized CORDIC-based GMSK system is designed, which includes GMSK Modulation with the channel and GMSK Demodulation. The modulation consists of non-return zero (NRZ) encoder, an integrator followed by Gaussian filtering and frequency modulation (FM). The GMSK demodulation consists of FM demodulator, followed by differentiation and NRZ decoder. The FM Modulation and demodulation use the optimized CORDIC model for an In-phase (I) and quadrature (Q) phase generation. The optimized CORDIC is designed by using quadrant mapping and pipelined structure to improve the hardware and computational complexity in GMSK systems. The GMSK system is designed on the Xilinx platform and implemented on Artix-7 and Spartan-3EFPGA. The hardware constraints like area, power, and timing utilization are summarized. The comparison of the optimized CORDIC model with similar CORDIC approaches is tabulated with improvements.

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1. INTRODUCTION

In the current era of high-speed communication, the prime objective of the system is to achieve modulation that has a power spectrum with a constant amplitude and adequate bandwidth. Out of all, some of the efficient techniques are minimum shift keying (MSK) and GMSK. They are derived from the constant-phase frequency shift keying (CPFSK) family of modulation operating at a constant envelope [1, 2]. As a modulated signal has the characteristic of constant amplitude, the power utilization will be low by using a class CRF amplifier. Employing an amplifier is necessary for battery operated units. The GMSK is well suited digital modulation type and used in the GSM standard. The spectral efficiency and constant envelope are two unique characteristics in GMSK are credited in enhancing result despite the adjacent channel interference (ACI) and non-linear amplifiers presence. The GMSK signal is an extended form of MSK signal by performing pre-filtering over it and also converts a particular case in the CPFSK or a filtered offset-quadrature phase shift keying (O-QPSK). The GMSK signal is generated from the various methods [3-10] and is classified as high-resolution synthesizer indirect modulation, and voltage controlled oscillator (VCO) direct modulation and quadrature amplitude modulation (QAM). The GMSK modulation technique is well known partial response continuous phase modulation (CPM) and suitable for the non-linear power amplifier. The GMSK system is used in many applications as a modulation technique, which includes the automatic

identification system (AIS) receiver for ship-based radio-data transmission systems, spectrum sensing for cognitive radio (CR) and vessel monitoring using status data transmitting model [11].

Section 2 describes the proposed optimized CORDIC based GMSK system with detailed architecture and also explains the optimized CORDIC model adopted in GMSK systems. Section 3 explains the simulation results of the GMSK system and analyzes the hardware constraints of optimized CORDIC based GMSK systems and comparison of the optimized CORDIC model with existing techniques. Section 4 concludes the overall work with improvements.

This section discusses the existing work of GMSK systems and its applications and also discussion of existing CORDIC techniques. The Babu et al. [12] describes the GMSK modulator for GSM applications, which includes differential encoder followed by pre-calculated gaussian values for pulse shaping, an IQ generation using a lookup table (LUT) based sine-cosine generator. Walter et al. [13] explain about GMSK Modulator, which performs the modulation using a delta-sigma frequency discriminator based synthesizer to produce the RF modulated signal and also prototyped the GMSK Modulator for GSM transmitter standards. The Gao et al. [14] presents the GMSK Demodulation using the general processing unit (GPU) on the ompute Unified Device Architecture (CUDA) programming platform and mainly includes Read-only memory (ROM) modules for Waveform generation, low pass FIR filter followed by multiplication and addition. Ghnimi et al. [15] present GMSK modulation under radio mobile propagation environments with different channels on a software-based environment. Supriya et al. [16] present reconfigurable coordinate rotation digital computer (CORDIC) based on rotating, vectoring mode for circular and hyperbolic trajectory. The designs use more coordinate calculation unit for recursive and pipelined architecture in both the modes of the CORDIC, which consumes more chip area.Chen et al. [17] present multiple rotation CORDIC for configurable fast fourier transform (FFT) accelerator, the FFT twiddle factors calculation based on the CORDIC rotation, which saves the hardware cost and CORDIC model designed using compression iteration with four rotations, twiddles direction prediction and segmented parallel iteration. However, this process utilizes much time in the FFT process. Chung et al. [18] present the FPGA based biped robot angles and distance calculation using pipelined CORDIC based inverse kinematic. To reduce the hardware cost, hardware sharing machine techniques are adopted and replaced the multipliers and dividers by adders and shifters. The biped robot angle design uses 18-stages pipelined architecture to increases the operating frequency of the model. Chinnathambi et al. [19] present the area efficient CORDIC algorithm, which uses six stages with four different methods includes without and with a pipelined method, unrolled CORDIC, and mux based CORDIC. The Tiwari et al. [20] presents the hybrid CORDIC algorithm which includes mixed two CORDIC processor of same angle input and another partitioned hybrid CORDIC algorithm, which includes two CORDIC processors of divided angle inputs. However, these architectures utilize more time process and consume more power. Torres et al. [21] present FPGA based optimized CORDIC based atan2 computation, which includes z-path implementation using LUT and cascaded carry chain. Wang et al. [22] present 16-bit CORDIC algorithm implementation, which calculation the full range calculation of angles for sine, cosine, and tangent. The CORDIC algorithms used in many applications for angle calculation includes quick response (QR) Decomposition multiple input multiple output (MIMO) channel detection [23], online spike time-dependent plasticity (STDP) learning with neurons [24].

From the review of recent literature, it has been noticed that the amount of work carried on GMSK systems is majorly based on software approaches and few on hardware-based approaches. In the available existing hardware-based approaches carried neither on GMSK Modulator nor on GMSK Demodulator, and not the complete framework. The available existing works are facing hardware complexity, performance degradation, and more chip area consumption with huge power consumption. The ROM based LUT table is used for IQ generation, and Local oscillators or VCO are used IQ Modulation in all the approaches, which consumes more chip area and affect the system performance. To compute the IQ generation efficiently by incorporating the CORDIC method in GMSK systems. The existing CORDIC methods are highly conventional, uses more iterations, ROM based table used tangent generation. Thus there is a need for "*Optimized CORDIC method for cost-effective GMSK systems*."

2. OPTIMIZED CORDIC BASED GMSK SYSTEM

In this section, the proposed GMSK system using the optimized CORDIC model is explained with its hardware architectures. The design flow of the proposed GMSK system is represented in Figure 1. It mainly consists of a GMSK modulator and demodulator along with the channel. The GMSK modulator mainly consists of hardware blocks of NRZ (non-return-zero) encoder, integrator, Gaussian filter, and frequency modulation (FM) using optimized CORDIC and digital frequency synthesizer (DFS). Similarly, the GMSK demodulator mainly consists of hardware blocks of FM demodulation using optimized CORDIC

and DFS, differentiator, and NRZ decoder. In this design, 1-bit GMSK input is considered and generate the 1-bit GMSK output.

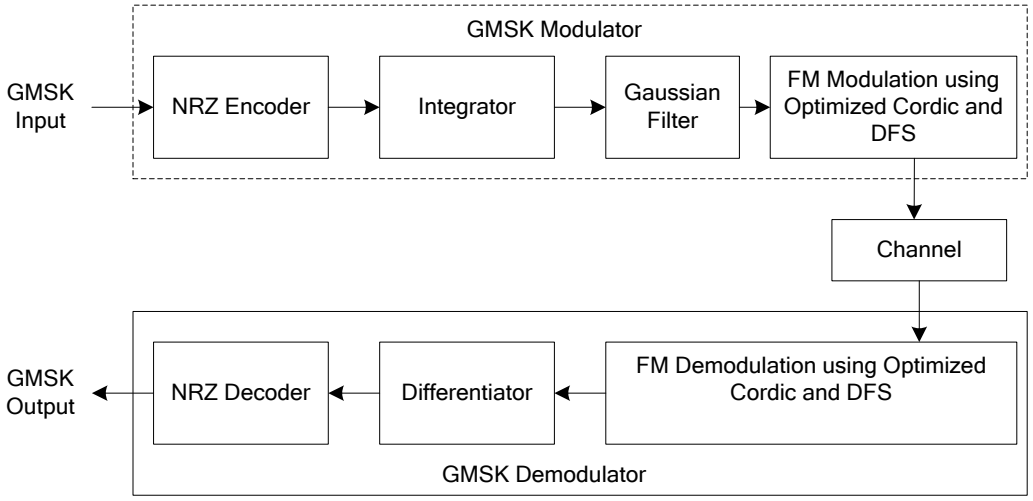

Figure 1. Design flow of proposed GMSK system

2.1. GMSK modulator

The GMSK modulator process the 1-bit input information in NRZ encoder. The XOR module receives the GMSK 1-bit input along with the data flip-flop (D-FF) output as an input in feedback form and grants the 1-bit output, which is input to integrator block, The integrator block mainly has four temporary registers which store the integrator data serially and add the last temporary data with first input to generate the integrator 1-bit output. The Gaussian filter is designed using finite impulse response (FIR) filter. The Gaussian filter is designed for 8-tap and targets to generate 16-bit output. It mainly uses 8-multipliers to multiply 8 FIR coefficients with integrator output, 15-delay flip-flops, and 7-adders. The 7th adder output generates the Gaussian filter output, which is input to FM Modulation. The FM Modulation hardware architecture is represented in Figure 2.

The FM modulation mainly contains an optimized CORDIC model for IQ generation and two DFS for IQ Modulation along with Control unit and Adder module. The optimized CORDIC model generates in-phase (I) for cosine (cos1) waveform and quadrature (Q) for sine (sine1) waveform based on the phase input (phase_in). The detailed optimized CORDIC model is explained in section 2.4. The CORDIC model outputs are inputs to two DFS module. The two DFS is used to generate the arbitrary waveforms for the corresponding CORDIC outputs. The cosine (cos2) and sine (sine2) waveforms are generated for IQ modulation. The control unit is used to control the cos2 and sine2 waveforms using integrator output. If the integrator output is '1', then cos2 as an output (I) and integrator output is '0', then sine2 as an output (Q). The adder adds I and Q signals and frame the 12-bit GMSK modulation output (Gmsk_mod = I+Q).

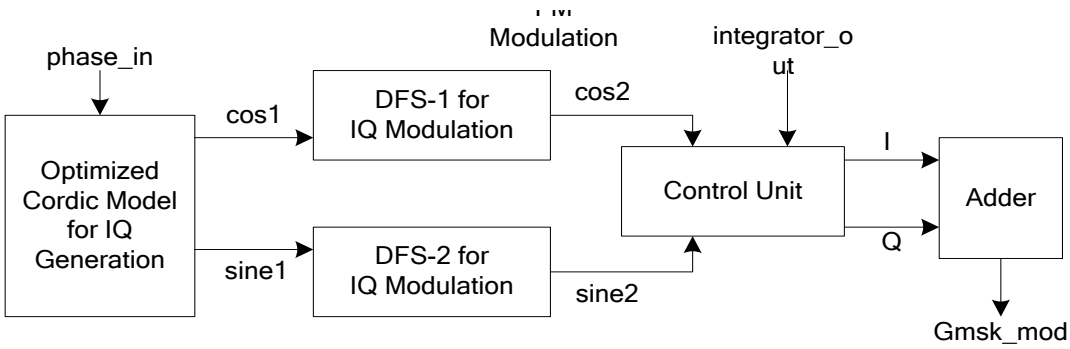

Figure 2. Hardware architecture of FM modulation

2.2. Channel

The channel is used to generate the random sequence generation that is called noise. The GMSK modulated output is mixed with the channel output to generate the randomized output, which is input to the GMSK demodulator. The channel module is designed using pseudorandom (PR) or maximum length (m) sequences based on the Galois field (GF) theory.

The m-sequences are generated from the linear feedback shift register (LFSR) and which is commonly known as Galois-LFSR. For high-speed hardware implementation, Galois-LFSR is a better option than Fibonacci-LFSR because it consumes fewer clock cycles to clock delay path than Fibonacci-LFSR. In design, The Galois-LFSR for a 5^{th} order generating polynomial is considered in GF (2). The 5^{th} order generator polynomial of the designed LFSR is

$$G(x) = x^5 + x^2 + 1 \quad (1)$$

The Galois-LFSR design uses 6-multipliers, 6-delay elements, and 5-adders. The six coefficient are used in the generator polynomial is G= [1, 0, 0, 1, 0, 1]. The two LFSR of the same polynomial is considered; add the two LFSR outputs to generate the random sequence. The random sequence is similar to the additive white gaussian noise [AWGN] generation in real-time considerations.

2.3. GMSK demodulator

The GMSK demodulator is mainly incorporating FM Demodulator along with Differentiator and NRZ decoder. The 12-bit channel output is input to GMSK Demodulator. The Hardware architecture of FM Demodulation is represented in Figure 3. The CORDIC model generates the cosine and sine output based on the phase inputs. In that, consider the cosine (cos1) for the DFS module, which generates the updated output (cos2). The control unit receives the delayed DFS output and channel output, perform the comparison to generate the FM demodulated output.

The differentiator receives the 1-bit FM demodulated output as an input, and it mainly consists of four temporary registers and subtract or units. It performs the differentiator operation to generate the 1-bit output. The NRZ decoder decodes the differentiator output and generates the 1-bit GMSK demodulated output. The GMSK output must match with GMSK input in order to ensure that the GMSK system is working correctly.

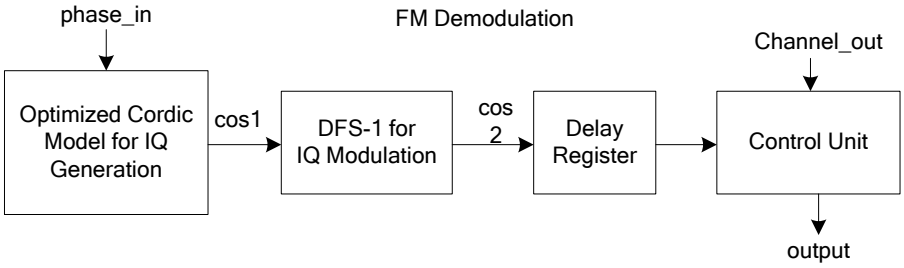

Figure 3. Hardware architecture of FM demodulation

2.4. Optimized CORDIC model

The optimized CORDIC model overcomes the conventional CORDIC problems like rotational angle coverage, more iterative stages, and less convergence speed. The proposed CORDIC model will be used for optimizing the angle range, computational and hardware complexity, usage of read-only memory (ROM) resources for LUT updation. The optimized CORDIC model is a preprocessing unit, pipelined CORDIC, a delay unit, and a post-processing unit is represented in Figure 4. The preprocessing unit has an 8-bit phase input and allocates the first 2-bit of MSB, i.e., phase input [7:6] has a 1^{st} quadrant and the same 2-bit inputs to delay unit. In design, the delay unit is used for the synchronization process. The preprocessing unit finds the quadrant location based on the MSB 2-bits. The preprocessed 8-bit output is input to the pipelined CORDIC module. The delay unit output and pipelined CORDIC module output generates parallelly to maintain the synchronization.

The hardware architecture of the pipelined CORDIC module is represented in Figure 5. For a high-speed CORDIC module with cosine and sine, a calculation is done by a single step pipelined technique. The preprocessed output (phase value) is input to Z_0 and set the initial values to X_0 and Y_0. In the design, six

iteration stages are used with pipeline structure. For each iteration stage, the angle (a) value updated directly to eliminate the ROM LUT table. Each stage, a set of outputs like X_1, Y_1, and Z_1 are obtained in each clock cycle, and processing speed of it will not affect the CORDIC calculation in stages because of the pipeline structure. The pipeline structure is directly proportional to the accuracy calculation. The sign (S) value will be updated based on the MSB (7^{th}) bit of Z input value or next stage values like Z1... Z6. The addition or subtraction will be performed by using Sign (S) value. The 6^{th} stage outputs are final cosine and sine values of pipeline CORDIC. The post preprocessing unit is used to convert the pipelined CORDIC output results based quadrants of the input values. In optimized CORDIC model, the input quadrant will be set "00" for input angle [0^o, 90^o], "01" for angle [90^o, 180^o], "10" for angle [180^o, 270^o] and "11" for angle [270^o, 360^o].

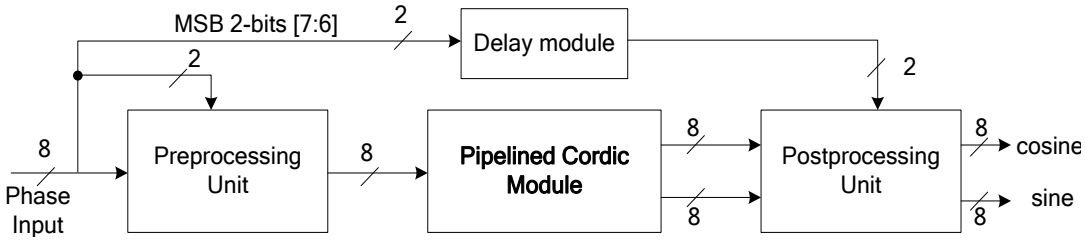

Figure 4. Optimized CORDIC model

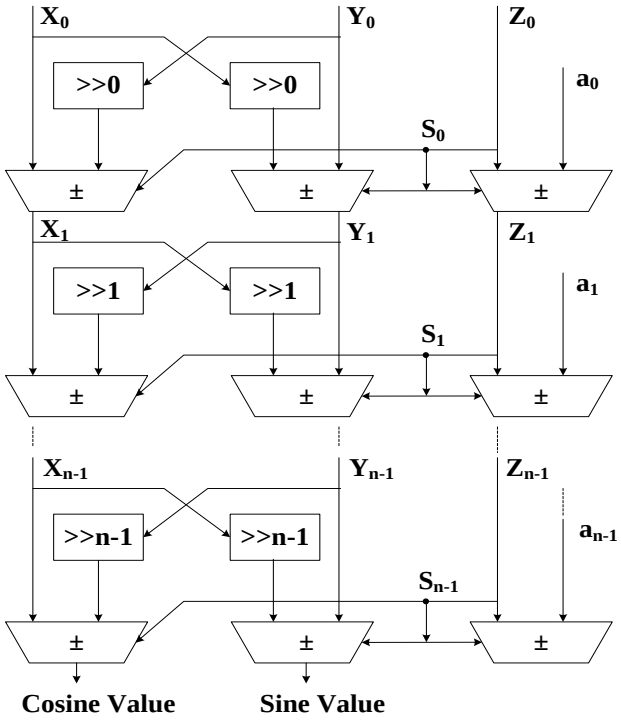

Figure 5. Hardware architecture of pipelined CORDIC module

3. RESULTS AND ANALYSIS

The optimized CORDIC based GMSK System results are analyzed in the below section. The proposed work is designed using Xilinx ISE 14.7 tool using Verilog-HDL language, and modelsim 6.5f is used for simulation. The proposed design is prototyped and implemented on the both Spartan3E and Artix-7 FPGA platform by considering devices-XC3S250E-4FT256 and XC7A100T-3CSG324 respectively.

The optimized CORDIC based GMSK system simulation results are represented in Figure 6. The global clock (clk) signal is activated with a positive edge along with active-low reset (rst). The control signals like enable (en) and start signals are activated high and used in the GMSK modulation process. Assign the 1-bit GMSK input (gmsk_in) according to the user's interest. The GMSK system process starts according to the design process. The GMSK input assigned randomly with long delays to visualize

the GMSK modulation output. Based on the GMSK inputs in modulation, 12-bit GMSK modulated output (gmsk_mod_out) is generated. When the gmsk_in is high, the GMSK Modulated output works at 1.72 MHz, and when gmsk_in is low, the gmsk_mod_out output works at 485.43 kHz frequency for one sinusoidal wave signal. The demodulated output (gmsk_out) is generated after the GMSK demodulation process. The GMSK output is the same as the GMSK input with the delay of 1 clock cycle. This simulation result indicates that the GMSK systems work effectively with low latency.

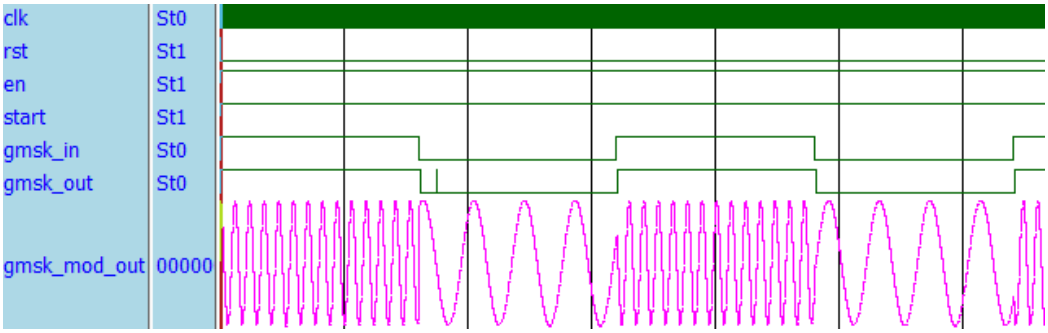

Figure 6. Simulation results of optimized CORDIC based GMSK system

The optimized CORDIC based GMSK System is synthesized, and after a place and route operation, the hardware resource utilization in terms of area, time, and power are summarized in Table 1. The GMSK system utilizes less chip area in terms of 271 slices, 331 Slice Flip-flops, and 499four-Input LUTson FPGA. The GMSK system operated a maximum frequency of 89.068 MHz with a minimum period of 11.227ns on Spartan-3EFPGA. The power consumption report is generated using the X-Power analyzer tool with an FPGA system frequency of 100 MHz. The GMSK system consumes the 0.052W total power.

The optimized CORDIC model is synthesized separately, and after a place and route operation, the hardware resource utilization in terms of area and time are summarized in Table 2. The optimized CORDIC model utilizes 88 slices, 119 Slice flip-flops, and 157four-Input LUTs on FPGA. The optimized CORDIC operated at 156.937 MHz maximum frequencies with a minimum period of 6.372ns on Spartan-3EFPGA.

Table 1. Hardware utilization summary of optimized CORDIC based GMSK system on Spartan-3EFPGA

	Hardware Resources	Optimized CORDIC based GMSK system
Area	Number of Slices	271
	Slice Flip-Flops	331
	4-input LUTs	499
Time	Minimum Period (ns)	11.227
	Max.Frequency (MHZ)	89.068
Power	Total power (W)	0.052

Table 2. Hardware resource utilization of optimized CORDIC module on Spartan-3EFPGA

Resource Utilization	Optimized CORDICDesign
Number of Slices	88
Slice Flip-Flops	119
4-input LUTs	157
Max.Frequency (MHZ)	156.937

The proposed optimized CORDIC model is compared concerning previous CORDIC methods like general unrolled CORDIC, Pipelined unrolled, and mux based CORDIC [25] in terms of performance parameters like area (Slice flip-flops, number of slices) and Latency (Number of clock cycles) are tabulated in Table 3. The performance parameter results are analyzed on the Spartan-3E FPGA for all the CORDIC methods.

The proposed method improves the area overhead around 36.36% in Slice-FF's 46.98% in slices and 36.36% in latency concerning pipelined unrolled CORDIC method. Similarly, compared with pipelined

mux based CORDIC method, around 4.8 % in slice-FF's, 33.83% in slices, and 12.5% in latency improvements. The above results, the proposed CORDIC is reduced the hardware complexity and improves the performance with area optimization in GMSK systems. To improve the design constraints using FPGA technology, here, Atrix-7 FPGA is considered, which is 28nm Technology compared with Spartan-3E FPGA, which works at 90nm Technology. The hardware utilization of Optimized CORDIC based GMSK system on Artix-7 FPGA is tabulated in Table 4, and the hardware resource utilization of only optimized CORDIC Module on Artix-7 FPGA is tabulated in Table 5.

Table 3. Performance comparison of optimized CORDIC module with previous [25]

CORDIC Method	Slice Flip-flops	No. of Slices	Latency(Clock cycles)
General Unrolled CORDIC [20]	134	160	7
Pipelined Unrolled CORDIC [20]	187	166	11
Pipelined Mux based CORDIC [20]	125	133	8
Proposed Optimized CORDIC	119	88	7

Table 4. Hardware utilization summary of optimized CORDIC based GMSK system on Artix-7FPGA

	Hardware Resources	Optimized CORDIC based GMSK system
Area	Slice Registers	145
	Slice LUTs	321
	LUT-FF pairs	133
Time	Minimum Period (ns)	3.854
	Max.Frequency (MHZ)	259.477
Power	Dynamic power (W)	0.008
	Total power (W)	0.09

Table 5. Hardware resource utilization of optimized CORDIC module on Artix-7 FPGA

Resource Utilization	Optimized CORDICDesign
Slice Registers	98
Slice LUTs	114
LUT-FF pairs	81
Max.Frequency (MHZ)	509.71

4. CONCLUSION

The optimized CORDIC based GMSK systems are designed and implemented on Spartan-3E and Artx-7FPGA. The GMSK systems mainly contain NRZ-Encoder and decoder, integrator-differentiator, Gaussian filter, and FM-modulation-demodulation along with channel. In FM modulation and demodulation, the optimized CORDIC model is incorporated for IQ generation, and DFS has used IQ modulation. The optimized CORDIC reduces the computational and hardware complexity by using pipeline structure along with quadrant mapping in GMSK systems. The GMSK system is simulated and synthesized on the Xilinx platform. The GMSK system resource constraints like area, time, and power utilization are tabulated. The GMSK systems operate at 89.068 MHz and consume less power of 0.052W on sparatn-3E FPGA.

Similarly, on Artix-7 FPGA, the GMSK systems operate at 259.477 MHz and consume less power of 0.09W. The optimized CORDIC model is compared with other CORDIC methods with improvements in area and latency. The optimized CORDIC model utilization shows improvements around 33.83% in slices and 12.5% in latency than pipelined-Mux based CORDIC technique.

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