

Subthreshold swing model using scale length for sub-10 nm junction-based double-gate MOSFETs

Hakkee Jung

Department of Electronic Engineering, Kunsan National University, Republic of Korea

Article Info

Article history:

Received Jun 24, 2019

Revised Oct 16, 2019

Accepted Oct 30, 2019

Keywords:

Double gate

Junction-based

Junctionless

Scale length

Subthreshold swing

ABSTRACT

We propose an analytical model for subthreshold swing using scale length for sub-10 nm double gate (DG) MOSFETs. When the order of the calculation for the series type potential distribution is increased it is possible to obtain accuracy, but there is a problem that the calculation becomes large. Using only the first order calculation of potential distribution, we derive the scale length λ_1 and use it to obtain an analytical model of subthreshold swing. The findings show this subthreshold swing model is in concordance with a 2D simulation. The relationship between the channel length and silicon thickness, which can analyze the subthreshold swing using λ_1 , is derived by the relationship between the scale length and the geometric mean of the silicon and oxide thickness. If the silicon thickness and oxide film thickness satisfy the condition of $(L_g - 0.215)/6.38 > t_{si}(=t_{ox})$, it is found that the result of this model agrees with the results using higher order calculations, within a 4% error range.

Copyright © 2020 Institute of Advanced Engineering and Science.
All rights reserved.

Corresponding Author:

Hakkee Jung,

Department of Electronic Engineering, Kunsan National University,

558 Daehangro, Gunsan, Chonbuk 54150, Republic of Korea.

Email: hkjung@kunsan.ac.kr

1. INTRODUCTION

The increasing importance of various multi-gate MOSFETs has been recognized as the development and commercialization of sub-10 nm transistors has become a reality [1-4]. A double gate (DG) MOSFET, which is the simplest structure among multiple gate devices, has been studied as a device capable of reducing the short-channel effect [5-7]. Although a two-dimensional simulation method is used to analyze the short-channel effect of sub-10 nm DGMOSFETs, a simple analytical model for circuit analysis has the focus of many studies [8-10]. However, most analyses using the analytical model are performed on DGMOSFETs of 20 nm or larger [11-13]. In this paper, we present an analytical model of the subthreshold swing (SS) that can be applied at 10 nm or less. The channel potential model used to derive the subthreshold swing model mainly uses a hyperbolic model, but it is difficult to satisfy the two-dimensional Poisson equation and this results in problems such as ambiguous dependence of the scale length λ_1 on silicon thickness [14].

In this paper, we present an analytical model of the subthreshold swing using Xie's two-dimensional potential model [15] and analyze the subthreshold swing according to scale length for junction-based double-gate (JBDG) MOSFETs. Xie et al. presented a two-dimensional potential distribution model of a series type, and concluded that it is sufficient to use the first term of the series potentials to analyze the short channel effect when the channel length is greater than 1.5 times the scale length ($L_g > 1.5 \lambda_1$). However, Xie et al. only analyzed cases in which channel length is relatively long, about 25 nm. In this study, we will analyze whether the above-mentioned conditions are applicable to sub-10 nm junction-based DGMOSFETs, and we will determine the range of scale length that can use this analytical subthreshold swing model. This paper is arranged as follows. The analytical subthreshold swing model is described in Section 2. We then present the effects of scale length and channel dimension on the subthreshold swing in Section 3 and discuss results in Section 4.

2. THE STRUCTURE OF JBDG MOSFET AND SUBTHRESHOLD SWING

Figure 1 shows a schematic diagram of the DGMOSFET used in this paper. The source and the drain were doped with a high concentration ($N_d^+ = 10^{20}/\text{cm}^3$) and the channel was lightly doped with $N_a = 10^{16}/\text{cm}^3$. The work-function of gate metal is ϕ_m , the dielectric constant of the oxide film ϵ_{ox} , the dielectric constant of silicon ϵ_{si} , the channel length L_g , the silicon thickness t_{si} , and the oxide film thickness t_{ox} . The potential distribution derived by Xie et al. can be expressed for the junction-based DGMOSFET as the following series [15].

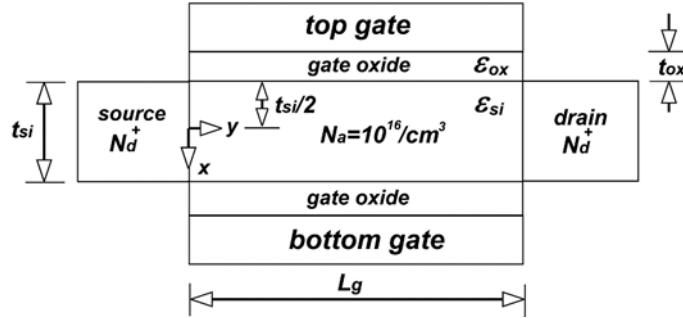


Figure 1. Schematic cross-sectional diagram of a Junction-based double gate MOSFET

$$\phi(x, y) = \frac{qN_a x^2}{2\epsilon_{si}} + V_{gs} - \Delta\phi - \frac{qN_a t_{si}^2}{8\epsilon_{si}} \left(1 + \frac{4\epsilon_{si} t_{ox}}{t_{si}} \right) + \sum_{n=1}^{\infty} \frac{b_n \sinh \left[\frac{\pi(L_g - y)}{\lambda_n} \right] + c_n \sinh \left[\frac{\pi y}{\lambda_n} \right]}{\sinh \left[\frac{\pi L_g}{\lambda_n} \right]} \cos \left(\frac{\pi x}{\lambda_n} \right) \quad (1)$$

$$b_n = \left[\frac{\left(\frac{2\lambda_n^2}{\pi^2 t_{ox}} \right) \tan \left(\frac{\pi t_{ox}}{\lambda_n} \right) \sin \left(\frac{\pi t_{si}}{2\lambda_n} \right) \left(\frac{E_g}{2q} - \phi_0 \right) - \left(\frac{\lambda_n^2 q N_a t_{si}}{\pi^2 \epsilon_{si}} \right) \cos \left(\frac{\pi t_{si}}{2\lambda_n} \right) \left(1 - \frac{2\lambda_n}{\pi t_{si}} \tan \left(\frac{\pi t_{si}}{2\lambda_n} \right) + \left(\frac{t_{si}}{4t_{ox}} \right) \tan \left(\frac{\pi t_{si}}{2\lambda_n} \right) \tan \left(\frac{\pi t_{ox}}{\lambda_n} \right) \right)}{\frac{t_{si}}{2} + t_{ox} \sin \left(\frac{\pi t_{si}}{\lambda_n} \right) / \sin \left(\frac{2\pi t_{ox}}{\lambda_n} \right)} \right]$$

$$c_n = \left[\frac{\left(\frac{2\lambda_n^2}{\pi^2 t_{ox}} \right) \tan \left(\frac{\pi t_{ox}}{\lambda_n} \right) \sin \left(\frac{\pi t_{si}}{2\lambda_n} \right) \left(\frac{E_g}{2q} + V_{ds} - \phi_0 \right) - \left(\frac{\lambda_n^2 q N_a t_{si}}{\pi^2 \epsilon_{si}} \right) \cos \left(\frac{\pi t_{si}}{2\lambda_n} \right) \left(1 - \frac{2\lambda_n}{\pi t_{si}} \tan \left(\frac{\pi t_{si}}{2\lambda_n} \right) + \left(\frac{t_{si}}{4t_{ox}} \right) \tan \left(\frac{\pi t_{si}}{2\lambda_n} \right) \tan \left(\frac{\pi t_{ox}}{\lambda_n} \right) \right)}{\frac{t_{si}}{2} + t_{ox} \sin \left(\frac{\pi t_{si}}{\lambda_n} \right) / \sin \left(\frac{2\pi t_{ox}}{\lambda_n} \right)} \right]$$

where E_g is the energy band gap of silicon, V_{ds} the drain voltage, V_{gs} the gate voltage, $\Delta\phi$ the work function difference between the gate metal and channels, and ϕ_0 the center potential at $x=y=0$. The λ_n is the eigenvalue that satisfies the following eigenvalue equation [9]

$$\epsilon_{si} \tan \left(\frac{\pi t_{ox}}{\lambda_1} \right) - \epsilon_{ox} \cot \left(\frac{\pi t_{si}}{2\lambda_1} \right) = 0 \quad (2)$$

$$\lambda_n \approx \lambda_1 / n \quad (n = 1, 3, 5, \dots)$$

In the case of a symmetrical DGMOSFET, the potential distribution can be obtained by assigning $\lambda_1, \lambda_3, \lambda_5, \lambda_7 \dots$ to (1) because λ_n is zero in cases where n is even for the symmetric structure. In general, it has been reported that analyzing the short-channel effects by only using λ_1 called the scale length is sufficient if $L_g > 1.5 \lambda_1$ [15,16]. Therefore, we want to obtain an analytical model of the subthreshold swing for $n=1$. In the first case, rewrite (1) for $n=1$ as follows.

$$\phi(x, y) = \frac{qN_a x^2}{2\epsilon_{si}} + V_{gs} - \Delta\phi - \frac{qN_a t_{si}^2}{8\epsilon_{si}} \left(1 + \frac{4\epsilon_{si} t_{ox}}{t_{si} \epsilon_{ox}} \right) + \frac{b_1 \sinh \left[\frac{\pi(L_g - y)}{\lambda_1} \right] + c_1 \sinh \left[\frac{\pi y}{\lambda_1} \right]}{\sinh \left[\frac{\pi L_g}{\lambda_1} \right]} \cos \left(\frac{\pi x}{\lambda_1} \right) \quad (3)$$

The subthreshold swing is a measure of the gate voltage change with respect to the drain current (I_{ds}) change. If the electron density constituting the drain current can be approximated by a Boltzmann distribution such as $n = (n_i^2/N_a) \exp(q\phi_{\min}/kT)$, the subthreshold swing can be expressed in the following equation [17,18].

$$SS = \frac{\partial V_{gs}}{\partial \log(I_{ds})} = \ln(10) \left(\frac{kT}{q} \right) \left(\frac{\partial \phi_{\min}}{\partial V_{gs}} \right)^{-1} \quad (4)$$

Here, k is the Boltzmann constant and T is absolute temperature. To obtain ϕ_{\min} , in (4) we find $y=y_{\min}$ that satisfies $\partial\phi(x, y)/\partial y=0$ and substitute the y_{\min} into (3). The y_{\min} thus obtained is as follows [19].

$$y_{\min} = \left(\frac{\lambda_1}{\pi} \right) \cosh^{-1} \frac{b_1^2}{\sqrt{b_1^2 - \left[b_1 \coth \left(\frac{\pi L_g}{\lambda_1} \right) - c \operatorname{csch} \left(\frac{\pi L_g}{\lambda_1} \right) \right]^2}} \quad (5)$$

Additionally, the value of x in (3) is the center of conduction, x_{eff} obtained as follows [20,21].

$$x_{\text{eff}} = \lambda_1 \cos^{-1} \left(\frac{\int_{x=0}^{x=t_{si}} \cos \left(\frac{x}{\lambda_1} \right) e^{q\phi(x, y_{\min})/kT} dx}{\int_{x=0}^{x=t_{si}} e^{q\phi(x, y_{\min})/kT} dx} \right) \quad (6)$$

That is, by substituting $y=y_{\min}$ and $x=x_{\text{eff}}$ into (3), the ϕ_{\min} can be obtained. Then by substituting the derivative of ϕ_{\min} by V_{gs} into (4), the subthreshold swing SS can be obtained. In this paper, we will test the validity of the subthreshold swing of (4) to obtain with this calculating process.

Figure 2 shows the change of the potential energy distribution for the channel length of 5 nm and 10 nm in the cases of $n=1$ and $n=11$ at $x=x_{\text{eff}}$. According to the results of Ding et al., the potential distribution converges sufficiently at $n=11$ [22]. As shown in Figure 2, when the channel length is 10 nm, the width of the potential energy distribution is different, but the maximum value of the energy that has the greatest effect on the drain current is equal regardless of n . However, when the channel length is reduced to 5 nm, it can be observed that not only is the width of the potential energy different, but also the maximum values are different. Such a difference will affect the drain current. In this paper, the tunneling current which occurs in the sub-10 nm DGMOSFET is ignored. With the tunneling current neglected, the drain current can be expressed by the following current continuity equation [23].

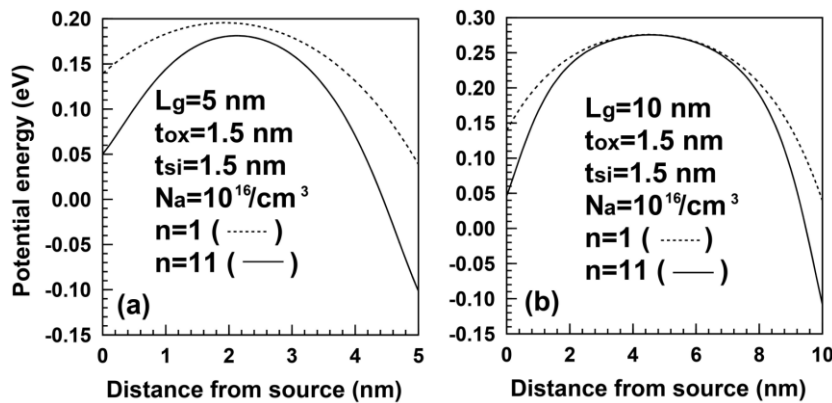


Figure 2. Potential energy distributions for the channel length of (a) 5 nm and (b) 10 nm

$$I_{ds} = \frac{n_i \mu_n W k T \left[1 - \exp\left(\frac{-qV_{ds}}{kT}\right) \right]}{\int_0^{L_g} \frac{dy}{\int_{-t_{si}/2}^{t_{si}/2} \exp\left(\frac{-q\phi(x,y)}{kT}\right) dx}} \quad (7)$$

Here, W is the channel width, which is the same as the channel length in this paper, and μ_n is the electron mobility.

Figure 3 shows the relationship between the drain current and the gate voltage from (8) according to the different values of n as described in Figure 2, using (7). As shown in Figure 3, when the channel length decreases to about 5 nm, the drain current-gate voltage relationship shows a large difference depending on n when the channel length decreases to about 5 nm. However, the slope, which is a measure of the subthreshold swing, did not show a large difference. As the channel length increases, the results obtained by using the potential energy distribution at $n=1$ and $n=11$ gradually coincide with each other. This means that even when the potential energy distribution of $n=1$ is used to analyze the subthreshold swing, it can be analyzed without a large error. Therefore, in this paper, we analyze the subthreshold swing according to the scale length λ_1 to verify the validity of the analysis when $n=1$.

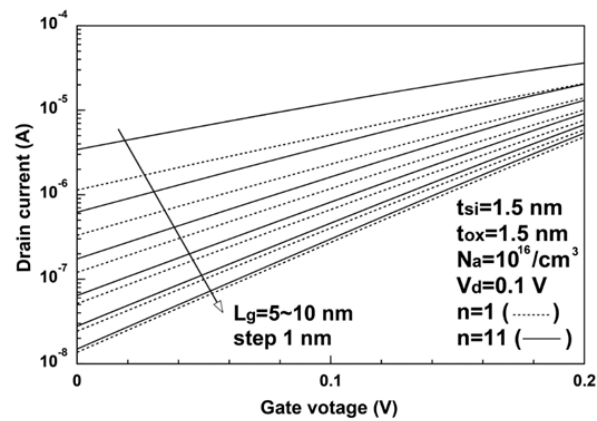


Figure 3. Relations of drain current and gate voltage for the different channel lengths

3. ANALYSIS OF SUBTHRESHOLD SWING USING SCALE LENGTH

First, in order to analyze the validity of the subthreshold swing model of (4) obtained hermetically at $n=1$, the range of channel length to satisfy the condition of $L_g > 1.5\lambda_1$ is obtained from Figure 4 when $t_{si}=1.5$ nm and $t_{ox}=1.5$ nm, and $t_{si}=1.0$ nm and $t_{ox}=1.0$ nm. As shown in Figure 4, the condition of $L_g > 1.5\lambda_1$ is satisfied for the range of $L_g > 10$ nm when $t_{si}=1.5$ nm and $t_{ox}=1.5$ nm. If the oxide and silicon thicknesses are reduced to 1.0 nm, the channel length to satisfy the condition of $L_g > 1.5\lambda_1$ must be reduced to 7 nm. Therefore, if the channel length is reduced below 7 nm, the oxide and silicon thicknesses must reduce below 1 nm to analyze the subthreshold swing, using this analytical subthreshold swing model. Note the oxide and silicon thickness as well as the channel length, become the important parameters which can use (4) to analyze the subthreshold swing for the DGMOSFETs.

The subthreshold swings by the slope of the drain current-gate voltage derived from the potential distributions obtained by $n \geq 5$ in (1) and those from (4) at $n=1$ were compared with the 2D simulation value [24] in Figure 5. As shown in Figure 5, it can be seen that when the channel length is more than 6 nm, there is a good agreement with the 2D simulation value regardless of n . It can be seen that those from (4) matches well with 2D simulation within a 4 % error even in the range of 10 nm or less, which does not satisfy the condition of $L_g > 1.5\lambda_1$. Note this analytical subthreshold swing model can be sufficiently used to analyze the short channel effects of the sub-10 nm DGMOSFETs.

To obtain the relationship of silicon and oxide thicknesses and channel length to satisfy the condition of $L_g > 1.5\lambda_1$, the contours of the minimum channel length to be able to calculate the subthreshold swings by this analytical model for the corresponding silicon and oxide thicknesses are shown in Figure 6. Firstly to sustain constantly the minimum channel length, the silicon thickness is inversely proportional to oxide thickness as shown in Figure 6. Also, the minimum channel length to be able to use this

analytical subthreshold swing model is increasing with the increase of silicon and oxide thicknesses in the range of $L_g > 1.5\lambda_1$. Therefore to analyze the subthreshold swings for the short channel DGMOSFETs using this model, silicon and oxide thicknesses must be also reduced with the decrease of the corresponding channel length. Especially if the channel length is below 10 nm, silicon and oxide thicknesses have to be determined carefully because two structural parameters are very thin to below 1.5 nm.

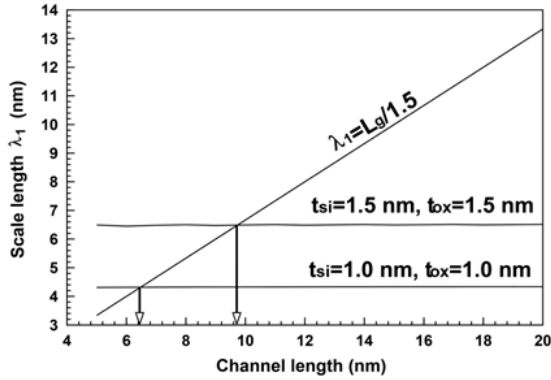


Figure 4. The relationship with scale length and channel dimensions to satisfy the condition of $L_g > 1.5\lambda_1$

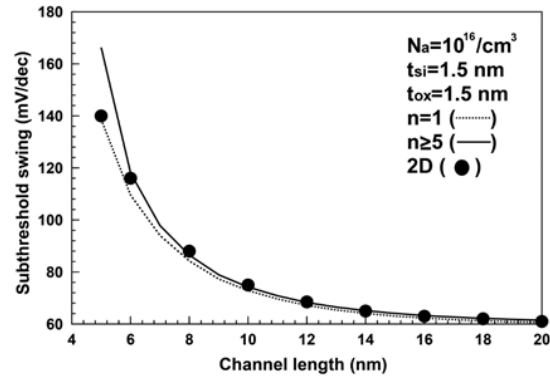


Figure 5. Comparisons of the subthreshold swings according to n in (1) for channel length. The dots denote the results of 2D simulation [24]

It can be found that the silicon and oxide thickness is 1.5 nm or less in Figure 6 in the range of channel length of 10 nm or less if silicon thickness and oxide thickness is equal. As shown in Figure 6, the scale length λ_1 is known to be proportional to the geometric mean of silicon thickness and oxide thickness [25]. Figure 7 shows the change in scale length for the geometric mean of the two parameters when the silicon thickness changes from 0.5 to 1.5 nm and the oxide thickness changes from 0.5 to 1.5 nm. The linear approximation function of the calculated points is as follows:

$$\lambda_1 = 4.255\sqrt{t_{si}t_{ox}} + 0.143 \text{ [nm]} \tag{8}$$

In (8), the scale length is 6.53 nm when the channel length is 10 nm and the silicon thickness and oxide thickness are 1.5 nm, and this satisfies the condition of $L_g > 1.5\lambda_1$. That is, in the case of a DGMOSFET having this size, it can be seen that even if the first term is only used in (1), a reasonable subthreshold swing can be obtained by (4). Using (8), the relationship between channel length, silicon thickness, and oxide thickness can be obtained to reasonably analyze the subthreshold swing. In other words, if the channel length is reduced to 5 nm, the silicon thickness and the oxide thickness will decrease to 0.75 nm according to the scale theory, and scale length will be 3.33 nm from (8). We then know that this scale length satisfies the condition of $L_g > 1.5\lambda_1$. In this way, even if the channel length is reduced to 10 nm or less, the short channel effect, such as the subthreshold swing, can be sufficiently analyzed using only λ_1 , adjusted with channel and oxide film thicknesses. Using the condition of (8) and $L_g > 1.5\lambda_1$, the relationship between the silicon thickness (or oxide film thickness) and the channel length for analyzing the subthreshold swing by using only $n = 1$, can be obtained as follows:

$$\frac{L_g - 0.215}{6.38} > t_{si} (= t_{ox}) \tag{9}$$

If the silicon thickness and the oxide film thickness satisfy the relation of (9), the subthreshold swing can be effectively analyzed with only $n = 1$ for the sub-10 nm DGMOSFETs. In this paper, the channel length of 10 nm, silicon thickness and oxide thickness of 1.5 nm were used as a reference point in order to observe the relationship between scale length and short channel effect in sub-10 nm DGMOSFETs. At this time, when the channel length is 5 nm, the silicon thickness and the oxide thickness should be reduced to 0.75 nm according to scaling theory.

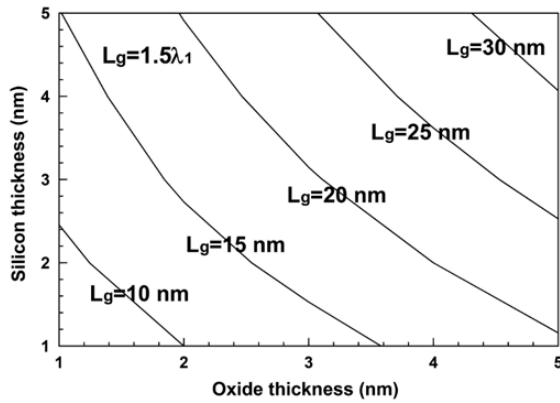


Figure 6. The contours of the minimum channel length to be able to use this analytical subthreshold swings

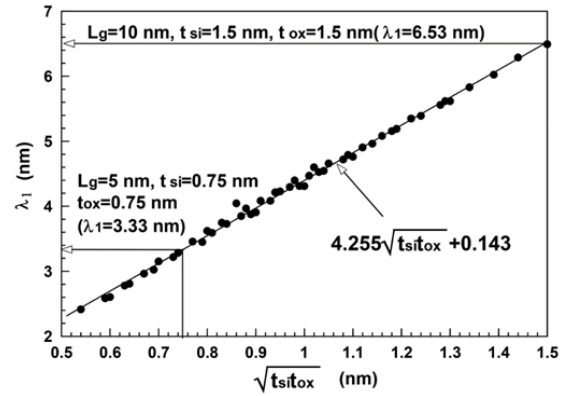


Figure 7. Relationship of scale length and the geometric mean of silicon thickness and oxide thickness in the range of 0.5 nm to 1.5 nm. The dots denote the scale lengths calculated by (2), and the line represents the linear approximation

According to the scaling theory, the geometric mean of the silicon thickness and the oxide thickness will decrease with decreasing channel length. In this case, the deviations of the subthreshold swings between $n=1$ and $n=5$ are shown in Figure 8. In Figure 8, the x -axis is the geometric mean of the silicon thickness and the oxide thickness at corresponding channel lengths, and the y -axis represents the difference of the subthreshold swings between $n=1$ and $n=5$, as a percentage. As shown in Figure 8, when the silicon thickness and the oxide thickness decrease with decreasing channel length according to the scaling theory, it is found that the value obtained by the analytical model of the subthreshold swing at $n=1$ satisfies a 4% error range. Therefore, in the case of a sub-10 nm DGMOSFET, if a λ_1 satisfying $L_g > 1.5\lambda_1$ is obtained and the corresponding silicon thickness and oxide thickness are obtained, the sufficiently satisfactory subthreshold swing can be analyzed using the model of (4).

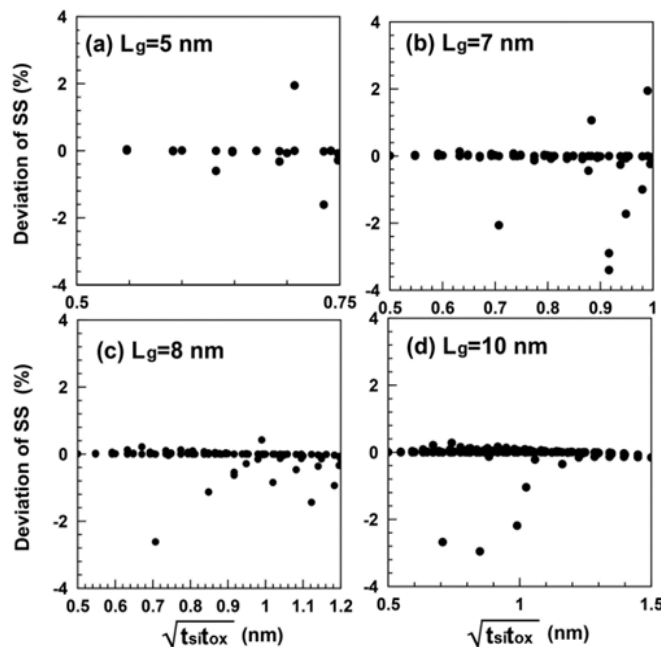


Figure 8. Deviation of subthreshold swings for $n = 1$ and $n = 5$ when (a) $L_g=5$ nm, (b) $L_g=7$ nm, (c) $L_g=8$ nm, and (d) $L_g=10$ nm for the geometric mean of silicon thickness and oxide thickness

4. CONCLUSION

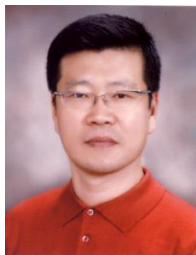
The analytical model for the subthreshold swing was presented for sub-10 nm DGMOSFETs and the validity of this model was investigated. To obtain the analytical model of the subthreshold swing, we used the series type potential distribution model derived from the Poisson equation. The analytical subthreshold swings obtained by using only the first term in the series type potential distribution model was in good agreement with those obtained by using terms of $n \geq 5$ and was also in good agreement with the two-dimensional simulation value. The appropriate silicon thickness and oxide thickness should be used in order that the subthreshold swings obtained using only the scale length λ_1 have a deviation of less than 4% from those obtained using $n \geq 5$. It is sufficient to analyze the subthreshold swings using only scale length λ_1 when $n=1$ if channel length and silicon thickness satisfying the condition of $(L_g-0.215)/6.38 > t_{si}(=t_{ox})$ are used when the silicon thickness and the oxide thickness are the same. We can conclude that the subthreshold swing can be sufficiently analyzed by using only the scale length λ_1 if the above condition is satisfied.

REFERENCES

- [1] X. Xiao, M. Chen, J. Zhang, T. Zhang, L. Zhang, Y. Jin, J. Wang, K. Jiang, S. Fan and Q. Li, "Sub-10 nm Monolayer MoS₂ Transistors Using Single-Walled Carbon Nanotubes as an Evaporating Mask," *ACS Appl. Mater. Interfaces*, vol. 11, no. 12, pp. 11612-11617, 2019. 10.1021/acsami.8b21437
- [2] L. T. Clark and V. Vashishtha, "Design with sub-10 nm FinFET technologies," 2017 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA. 30 April-3 May 2017. 10.1109/CICC.2017.7993720
- [3] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain and A. F. Roslan, "Geometric and process design of ultra-thin junctionless double gate vertical MOSFETs," *International Journal of Electrical and Computer Engineering*, vol. 9, no. 4, pp. 2863-2873, 2019. 10.11591/ijece.v9i4.pp2863-2873
- [4] T. B. Hook, "Power and Technology Scaling into the 5 nm Node with Stacked Nanosheets," *Joule*, vol. 2, no.1, pp. 1-4, 2018. 10.1016/j.joule.2017.10.014
- [5] R. Vaddi, R. P. Agarwal, S. Dasgupta S and T. T. Kim, "Design and Analysis of Double-Gate MOSFETs for Ultra-Low Power Radio Frequency Identification (RFID): Device and Circuit Co-Design," *J. Low Power Electron. Appl.*, vol. 1, no.2, pp. 277-302, 2011. 10.3390/jlpeal020277
- [6] Z. Ramezani and A. A. Orouji, "A novel double gate MOSFET by symmetrical insulator packets with improved short channel effects," *International Journal of Electronics*, vol. 105, no.3, pp. 361-374, 2018. 10.1080/00207217.2017.1357206
- [7] R. Guatam, M. Saxena, R. S. Gupta and M. Gupta, "Analytical Model of Double Gate MOSFET for High Sensitivity Low Power Photosensor," *J. of Semiconductor Technology and Science*, vol. 13, no. 5, pp. 500-510, 2013. 10.5573/JSTS.2013.13.5.500
- [8] C. Jiang, R. Liang, J. Wang and J. Xu, "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs," *AIP ADVANCES*, vol. 5, no. 5, pp. 057122-1-13, 2015. 10.1063/1.4921086
- [9] A. Nandi, A. K. Saxena and S. Dasgupta, "Analytical Modeling of a Double Gate MOSFET Considering Source/Drain Lateral Gaussian Doping Profile," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3705-3709, 2013. 10.1109/TED.2013.2282632
- [10] F. Yu, G. Huang, W. Lin and C. Xu, "An analytical drain current model for symmetric double-gate MOSFETs," *AIP ADVANCES*, vol. 8, no. 4, pp. 045125-1-12, 2018. 10.1063/1.5024574
- [11] A. Marzaki, V. Bidal, R. Laffont, W. Rahajandraibe, J-M. Portal, E. Bereret and R. Bouchakour, "On the Investigation of a Novel Dual-Control-Gate Floating Gate Transistor for VCO Applications," *Bulletin of Electrical Engineering and Informatics*, vol. 2, no. 3, pp. 212-217, 2013. 10.11591/eei.v2i3.206
- [12] B. Mehrdel, A. A. Aziz and M. H. Ghadiri, "Effect of Device Variables on Surface Potential and Threshold Voltage in DG-GNRFET," *International Journal of Electrical and Computer Engineering*, vol. 5, no. 5, pp. 1003-1011, Oct. 2015. 10.11591/ijece.v5i5.pp1003-1011
- [13] R. Fahiha, C. N. Saha and M. S. Islam, "Analytical modelling and performance analysis for symmetric double gate stack-oxide junctionless field effect transistor in subthreshold region," 2017 IEEE Region 10 Humanitarian Technology Conference (R10-HTC), Dhaka, Bangladesh, 21-23 Dec. 2017. 10.1109/R10-HTC.2017.8288963
- [14] Q. Xie, J. Xu and Y. Taur, "Review and Critique of Analytic Models of MOSFET Short-Channel Effects in Subthreshold," *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1569-1579, 2012. 10.1109/TED.2012.2191556
- [15] Q. Xie Q, Z. Wang and Y. Taur, "Analysis of Short-Channel Effects in Junctionless DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3511-3514, 2017. 10.1109/TED.2017.2716969
- [16] X. Lang and Y. Taur, "A 2-D Analytical Solution for SCEs in DGMOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1385-1391, 2004. 10.1109/TED.2004.832707
- [17] K. E. Kaharudin, F. Salehuddin, A. H. Hamidon, A. S. M. Zain, M. N. I. A. Aziz and I. Ahmad, "Variability Analysis of Process Parameters on Subthreshold Swing in Vertical DG-MOSFET Device," *ARNP J. of Engineering and Applied Sciences*, vol. 11, no. 5, pp. 3137-3142, March 2016.
- [18] T. Bentricia, F. Djeflal and M. Meguellati, "Analytical Investigation of Swing Factor for Nanoscale Double Gate MOSFET Including Gate-work-function Effect," *Proc. of the World Congress on Engineering*, London, U.K., 1-3 July, 2015.

- [19] H. K.Jung, "Analysis of Threshold Voltage Roll-off and Drain Induced Barrier Lowering in Junction-Based and Junctionless Double Gate MOSFET," *J. Korean Inst. Electr. Electron. Mater. Eng.*, vol. 32, no. 2, pp. 104-109, March 2019. 10.4313/JKEM.2019.32.2.104
- [20] Q. Chen, B. Agrawal and J. D. Meindl, "A Comprehensive Analytical Subthreshold Swing(S) Model for Double-Gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1086-1090, 2002. 10.1109/TED.2002.1003757
- [21] P. K. Tiwari and S. Jit, "A Subthreshold Swing Model for Symmetric Double-Gate (DG) MOSFETs with Vertical Gaussian Doping," *Journal of Semiconductor Technology and Science*, vol. 10, no. 2, pp. 107-117, 2010.
- [22] Z. Ding, G. Hu, J. Gu, R. Liu, L. WanL and T. Tang, "An analytic model for channel potential and subthreshold swing of the symmetric and asymmetric double-gate MOSFETs," *Microelectronics J.*, vol. 42, no. 3, ,pp. 515-519, 2011. 10.1016/j.mejo.2010.11.002
- [23] B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar and S. Jit, "Analytical modeling of subthreshold characteristics of ion-implanted symmetric double gate junctionless field effect transistors," *Material Science in Semiconductor Processing*, vol. 58, pp. 82-88, Feb. 2017. 10.1016/j.mssp.2016.10.051
- [24] D. Munteanu and J. L. Aufran, "Two-dimensional modeling of quantum ballistic transport in ultimate double-gate SOI devices," *Solid-State Electronics*, vol. 47, no. 7, pp. 1219-1225, 2003. 10.1016/S0038-1101(03)00039-X
- [25] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie and Y. Arimoto, "Scaling Theory for Double-Gate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2326-2329, 1993. 10.1109/16.249482

BIOGRAPHY OF AUTHOR



Prof. Hakkee Jung received the B.S. degree from Ajou University, Korea, in 1983, the M.S. and Ph.D. degrees from Yonsei University, Seoul, Korea, in 1985, 1990, respectively, all in electronic engineering. In 1990, he joined Kunsan National University, Chonbuk, Korea, where he is currently a Professor in the department of electronic engineering. From 1995 to 1995, he held a research position with the Electronic Engineering Department, Osaka University, Osaka, Japan. From 2004 to 2005, and 2016 to 2017, he was with the School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia. His research interests include semiconductor device physics and device modeling with a strong emphasis on quantum transport and Monte Carlo simulations.