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Accurate leakage current models for MOSFET nanoscale devices

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ABSTRACT

This paper underlines a closed form of MOSFET transistor's leakage current mechanisms in the sub 100nmparadigm.The incorporation of drain induced barrier lowering (DIBL), Gate Induced Drain Lowering (GIDL) and body effect (*m*) on the sub-threshold leakage (I_{sub}) was investigated in detail. The Band-To-Band Tunneling (I_{BTBT}) due to the source and Drain PN reverse junction were also modeled with a close and accurate model using a rectangular approximation method (RJA). The three types of gate leakage (I_G) were also modeled and analyzed for parasitic (I_{GO}), inversion channel (I_{GC}), and gate substrate (I_{GB}). In addition, the leakage resources due to the aggressive reduction in the oxide thickness (<5nm) have been investigated. Simulation results using HSPICE exhibits a tremendous agreement with the BSIM4 model. The dominant value of the sub-threshold leakage was due to the DIBL and GIDL effects. Various recommendations regarding minimizing the leakage current at both device level and the circuit level were suggested at the end of this paper.

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1. INTRODUCTION

Recently, nanoscale CMOS devices have a tremendous demand for low power/high-performance applications [1]. This demand will remain increasing because of the promising electrochemical properties of Si semiconductor, among those properties, low power, high-performance operation, high-speed switching, and its immunity to physical variation [2]. Meanwhile, various literatures studied the nanoscale CMOS transistor's behavioral and proposed fast models for circuit simulations [3]. The leakage current is the main unwanted rate of current flow through the three main terminals of MOSFET transistor (Source, Gate, and Drain). This current is caused by the Short Channel Effect (SCE) and affects the overall behavior of the transistor.

There are five types of gate leakage which are the parasitic gate leakage from the Gate to S/D Overlap region (I_{GO}) and which creates two currents (I_{GSO}) and (I_{GDO}), the Gate to the Inverted Channel Leakage (I_{GC}) which have two parts (I_{GCS}) and (I_{GCD}), and the Gate to the Substrate Leakage current (I_{GB}) [4]. The Band-to-Band tunneling current is caused by the high electric field during the standby node between the drain and the depletion layer. The higher value of the drain voltage (> depletion layer voltage) allows the electrons to tunnel from the reverse PN junction between the drain and depletion layer with a density depends on the applied voltages, the depletion layer depth, doping concentrations, and other factors that are discussed later. The higher complexity of calculating the integrals to find the value of tunneling leakage makes the importance of various approximations such as the rectangular approximation to find the values of the electric field and leakage current at any point of the irregular PN junction [5].

There are two types of Band-to-Band Tunneling current (I_{BTBT}), one flows from the source to the substrate (I_{BTBTS}) and the other current flows from the drain to the substrate (I_{BTBTD}). The sources of leakage current in the MOSFET transistor due to the nanoscale are shown in [5]. Kaushik Roy et *et. al*. [5] had various contributions in the modeling of leakage current in micro and nanoscale devices, K. M. Cao [6] proposed a model for gate current (I_G) in BSIM4 model with a good agreement compared with the simulation model. Udit Monga and others [7] proposed a model for subthreshold current in short channel effect and double-gate MOSFET by assuming that the electrostatic fields are dominated by the coupling capacitances, J. P. Sun [8] proposed a model for gate current and capacitance for CMOS device in the nanoscale paradigm considering the full consistent solution for Schrodinger-Passion Equation, a unified and accurate study for the gate structure to model its current and capacitance. A. Rastogi and his team in [9] proposed a model for total leakage at Sub-Micron paradigm with the inclusion of some of its sources such as the sub-threshold leakage and Band-To-Band Tunneling (BTBT). However, with the scaling down of the device dimensions, other types of leakage will be dominant and need to be modeled.

In this paper, accurate models of leakage current for nanoscale CMOS transistors using simple equations are proposed. The proposed models applied using different SPICE parameters under various conditions and showed their superiority in comparing with other models. The rest of the paper is organized as follows: Section 2 presents the modeling mechanisms for leakage components. Section 3 presents the simulations and results. Finally, section 4 concludes the paper.

2. RESEARCH METHOD

The main barrier of the nanoscale transistor is the leakage current, lowering the length of the channel to less than 90 nm causes several challenges such as the heat and the power dissipation. The power dissipation is caused by the leakage currents. These leakages are Sub-Threshold leakage (I_{sub}), Gate leakage (I_G), and Band-to-Band Tunneling (I_{BTBT}) respectively. In order to analyze and adopt new models to measure these leakage currents, special tools were used, these tools are the HSPICE and the MATLAB. The HSPICE is needed to measure the leakages using different types of transistors, while the MATLAB is used to extract the proposed models and to verify their effectiveness compared with other models submitted from different references. The proposed models seemed to be more accurate than the previous models shown in different references.

2.1. Modeling of subthreshold leakage

The dominant type of leakage current in the nanoscale MOSFET devices is caused by the Short Channel Effect (SCE). The simulation result showed fora channel length of 22 nm and the Drain to Source applied voltage (V_{DS}) equals to 0.8 V by using source voltage (V_{CC}) at 0.2 V is equal to ($0{,}25\times10^{-7}$) A. This type of leakage is caused by the reverse biasing voltage of the transistor at the standby mode. There are four significant parameters that affect directly its value and speed; these parameters have occurred at weak inversion region effect which is the Drain Induced Barrier Lowering (DIBL), the Gate Induced Drain Lowering (GIDL), and the Body Effect Factor (m). Simulation results showed that these factors are assumed to be less sensitive than the terminal voltages and other parameter variations in the long channel models. The variations of these effective parameters are modeled and added in the subthreshold equation. The weak inversion current which is the main part of the subthreshold current that initializes when the gate voltage is lower than the threshold voltage (V_{th}) is analyzed too. The lower variation of the potential across the inverted channel causes a small variation in the Effective Electric Field. In the weak inversion region, most of the carrier concentration is large, so the drain voltage drops across the reverse-biased drain-substrate PN junction and the drift component is ignored. Carriers move along the surface like the charge transport, and the subthreshold conductions are limited by the diffusion current. The weak inversion current equation is expressed in [10]. Figure 1 shows the main MOSFET transistor terms (Source, Gate, and Drain) and the locations of each leakage currents sources.
The drain current for the higher drain voltage is given by the following formula:

$$I_{ds}(V_{dsH}) = \left\{ I_0 . exp(\frac{V_{gs}-V_{TH}}{\gamma v_T}) \times [1 - exp(V_{dsH}/v_T)] \right. \quad (1)$$

where: γ is body effect, v_T is the thermal voltage and it is equal to kT/qand the drain current with the lower drain voltage is given by the equation:

$$I_{ds}(V_{dsL}) = \left\{ I_0 . exp\frac{(V_{gs}-V_{TH}}{\gamma v_T}) \times [1 - exp(V_{dsL}/v_T)] \right. \quad (2)$$

but the highest drain voltage is equal to its lowest value plus the difference in between. Dividing equation 4 by 6 and substituting the value of the drain voltage with respect to the lowest value will give the following formula:

$$\frac{I_{ds}(V_{dsH})}{I_{ds}(V_{dsL})} = \left\{\frac{I_0.\left(exp\frac{V_{gs}-V_{th}}{\gamma v_T}\right)}{I_0.\left(exp\frac{V_{gs}-V_{th}}{\gamma v_T}\right)} \times \left(\frac{1-exp(V_{dsL}+\Delta V_{ds}/v_T)}{1-exp(V_{dsL}/v_T)}\right)\right. \quad (3)$$

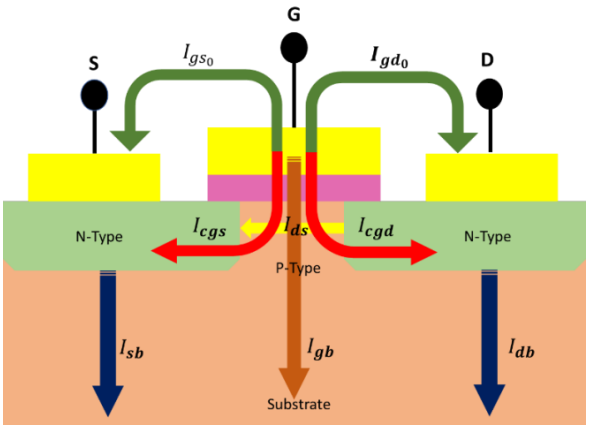

Figure1. Leakage current sources in a transistor

Simplifying the equation above then taking the *log* for both sides, then doing some mathematics we will get the ΔV_{ds}, reference [11] has more details and explanations regarding the extraction and derivation of the above equations. The final expression for the DIBL equation can be determined by the equation below:

$$D = \left\{\frac{qt_{ox}N_B W_{dm} r_j\left(\sqrt{1+\frac{(2W_{dm}}{r_j})}-1\right)}{C_{ox}\gamma V_T L_{ch}^2 \, ln[\left[\frac{I_d(V_{dsh})}{I_d(V_{dsl})}\right]]}\right\} \quad (4)$$

where: V_{dsH}, V_{dsL} is the higher and the lower drain voltage. W_{dm} is the width of the depletion layer, r_j junction depth for the drain and source. t_{ox} is the oxide thickness. It can be observed from equation 4 above that most of the significant nanoscale parameters that affect DIBL is considered with direct relationship and simple equations. The GIDL is another factor that affects the subthreshold current because of the higher potential across the overlapping region of the gate and drain. A significant amount of current and decaying delay is adding to the subthreshold current because of GIDL. This amount of leakage is caused by the reduced thickness of the gate insulator and the higher electric field through the device. As a result, the parasitic and the oxide capacitance allow the current to tunnel from the gate to the channel and drain. This current density can be described as shown in [12] where more analysis and descriptions of the model's extraction and explaining the parameter equations are found there. After adding these factors to the total subthreshold leakage, the leakage current values can be formulated as the following:

$$I_{sub} =$$

$$\left\{\frac{W_{eff}}{L_{eff}}\mu\sqrt{\frac{q\varepsilon_{si}N_{ceff}}{4\phi_R}}.\left(\frac{kT}{q}\right)^2 \times exp\left(\frac{V_{gs}-V_{th}-\Upsilon V_{bs}}{\frac{\gamma kT}{q}}\right) \times \left(1-exp\left(-\Xi\frac{qV_{ds}}{kT}\right)-exp\left(-\Theta\frac{qV_{ds}}{kT}\right)\right)\right\} \quad (5)$$

where $\varphi_R = (\varphi_B - \Delta\varphi_B)$ is the real barrier height, Υ is the linearization factor for the body effect, Θ is the GIDL term, Ξ is the DIBL term.

2.2. Modeling of the gate to inverted channel leakage

Leakage current, in general, flows from the gate to the channel through the forbidden energy gap at the S_{iO2} layer when the potential of the oxide is lower than the barrier height (φ_{ox}). The calculation of the gate leakage is started by assuming that the gate voltage is equal to zero and based on the analytical model presented in [10]. The Gate to the inverted channel (I_{GC}) modeling contains two types of electrons tunneling mechanisms Fowler–Nordheim (FN) tunneling and direct tunneling. The current density described in equation (6) can be

approximated using the current density direction and continuity equations in [6] to have a simple density equation with a high accuracy when the position of tunneling *x* and the applied voltage is larger than the length *L* as follow:

$$\left\{J_G \approx G_0 E_{ox}^2 \, exp\left[\frac{-G_1}{E_{ox}}\right] \approx G_0 E_{ox}^2 \, exp\left[\frac{-G_1 t_{ox}}{(V_{oxs}-V)}\right] \equiv J_{G0} \, exp(-G_1^* V)\right\} \quad (6)$$

where G^*_1 is modeled from the current density equation with $V_{oxs} \approx V_{GS}$ to be $G_1^* = P_{\text{gcd}} G_1 t_{ox} / V_{oxs}$ with P_{gcd} a fitting parameter, V is the voltage at any point of the channel length, which is described as in [8]. The final model for the gate to an inverted channel is described as:

$$\left\{Iox_{gs_{eff}} {}_{eff} \left.\frac{dV_1}{dx}\right|_{X=0} {}_{gcd} = -J_{G0} W_{eff} L_{eff} \left(\frac{[(G_1^* KL_{eff})(exp(-G_1^* KL_{eff}))]+(exp(-G_1^* KL_{eff})-1)}{(G_1^* KL_{eff})^2}\right)\right\} \quad (7)$$

where $V_1(x)$ is approximated as in [12]. It is observed that the gate to the inversion channel current is affected by the oxide thickness and gate voltages, width, electric field, and length, for more details and analysis regarding the mathematical equations and parameters; they are explained in [13].

2.3. Modeling of gate to source and drain overlapping leakage

This type of leakage occurs due to the coupling capacitance at the overlapping region between the gate and the drain or sources. Its value is significant at nanoscale technology with the short channel effect and thin oxide insulator. In 2011 a model based on trap assisted tunneling model has been proposed by [10]. As it is explained in [14], the flowing of electrons from the silicon to the oxide causes an image charge at the interface between the Si and SiO_2 on the oxide region, this cause also a remarkable reduction at the Oxide Electrostatic Potential (OEP) and causes an increasing in the gate current by the value of ($\Delta\Phi_{ox}$). According to the cancellation of negative and positive trap charge at the edge of the overlapping region near the gate side, the term of the flat band voltage will cancel each other, more details regarding this flat band voltage equation of the electric field for the overlapping region is given by [11, 12] The total leakage overlapping leakage will be as in the equation (8) [11, 12, 15].

$$I_{gd/s0} = \left\{W_{eff} L_{eff} A_G \left(\frac{V_{d/s}}{t_{ox}}\right)^2 \times exp\left(\frac{-B_G\left(1-\left(1-\frac{V_{s/d}}{\phi_{ox}-\left[\sqrt{\frac{q^3(V_{th}^2/2+V_{FB}-\rho_b V_{s/d})}{4\pi t_{ox}\varepsilon_{ox}}}\right]}\right)\right)}{V_D} t_{ox}\right)\right\} \quad (8)$$

2.4. The gate to substrate leakage current modeling

This type of current tunnels from the gate through the oxide insulator to pass the inversion layer then leads into the depletion layer. The values of I_{GB} are very low in comparison with the other types of gate leakage especially for higher doping concentration and reverse biasing at nanoscale technology. The value of I_{GB} becomes significant in the next generation technologies when the transistor dimensions are reduced to be lower than 5 nm. The method for calculating the base current can be calculated as the same method of calculating the previous types of gate leakage.

2.4.1. Modeling of band to band tunneling

This type of leakage occurs at reverse biasing with a high electric field, these allow a remarkable amount of tunneling current flows through the reverse p-n junction due to the motion of electrons from the valence of the junction to the conduction region. BTBT current includes the phonons distribution of the electrons, and it occurs when the bandgap voltage is less than the voltage drop across the p junction. Many works of literature treat the problem of expressing this type of leakage starting from calculating the I_{BTBT} current density [9, 10], more details regarding the BTBT current could be found in [11, 12]. When the biased voltage at

the source and drain is larger than the substrate voltage, an amount of current will flow through the drain/source-substrate junction. The sum of these two junctions flowing current represents the total MOSFET BTBT leakage current is shown in the following formula [16]. The total BTBT leakage current can be described using the rectangular junction approximation having the following equation:

$$I_{BTBT} = \left\{ I_{side} + I_{bottom} = \left[W_{eff} \int_{y_1}^{y_2} J_{b-b}(x_j, y)\, dy|_{side} \right] + \left[W_{eff} \int_{x_1}^{x_2} J_{b-b}(x, y_j)\, dx|_{bottom} \right] \right\} \quad (9)$$

where: (xj, yj) are the side and bottom junction positions, which are in fact perpendicular to each other. Solving these equations, the total BTBT leakage current becomes consisting of the bottom-bottom and side current density side, which defined as shown in [12, 13, 16, 17]. All these functions are solved using Figure 1 with trivial procedure reported in [13]. Where NC and NV are the effective densities for the states of conduction and valence bands, $F_{1/2}^{-1}$ is the inverse of the Fermi-Derek integral which is solved using the approximations proposed in [10, 12, 18].

3. SIMULATIONS AND RESULTS

In the simulation part, the applied voltages are chosen to satisfy the condition at the standby mode of MOSFET transistor, the channel length is chosen to be 22 nm, the oxide thickness is 1.6×10^{-9} m, and the threshold voltage is equal to 0.3692 V. The analytical results are compared to the simulation result for the BSIM4 model with the same simulation environment. The error is calculated using the Absolute Error Method (AEM).

3.1. Subthreshold leakage current Comparisons and simulation results

The simulations in this paper are adjusted to verify the accuracy and simplicity of the proposed models. The SPICE tools are used to simulate the proposed models using PTM MOSFET 22 nm technology. The proposed models are compared with the simulation results of other models using the same device specification. The subthreshold leakage current (I_{sub}) model is compared with the HSPICE model for MOSFET with a channel length equal to 22 nm. The proposed equations for leakage currents are also applied for higher sizes e.g. (32 nm and 45 nm) and lower size (16 nm) to show their higher accuracy for higher scale due to the lower SCE. Also, the threshold voltage for N-MOSFET is 0.3692 V and 0.25399 V for the P-MOSFET type. The applied drain voltage is 0.8 V and the width of the P-MOSFET gate is triple the width of N-MOSFET because the mobility of N-MOSFET is triple than the mobility value of P-MOSFET. The proposed models for the gate current (I_g) are also simulated and compared with the recently proposed models for the same specification, then all of them are compared with the HSPICE [19]. The models of Band-to-Band leakage current (I_{BTBT}) are also simulated in this paper and compared with the reference model using HSPICE.

Figure 2 shows the relation between the junction depth and DIBL variation compared to the simulation results for BSIM4 reported in [13] with different values of depletion layer depth. The increasing depletion layer depth, of course, causes an increasing of DIBL value because of increases in substrate doping concentration which influences barrier height beneath the channel surface at the drain junction side. The maximum value of DIBL when the depletion layer depth equal to 1.55 nm is 7.81 *n*A and it is equal to 27.5 nA in the case of 4.5 nm depletion layer width. Finally, when the proposed model is compared with different published models like in [5, 9, 10] as a function of channel length, the proposed model is faster and closer one to the simulated one reported in [13] with lowest average error as shown in Figure 3. According to this figure and at channel length 22 nm, the BSIM4 model of DIBL current is equal to 8.05 nA while it is 7.81 nA for the proposed model.

According to Figure 4, the DIBL and GIDL component due to the Subthreshold current is low sensitivity, which is unsuitable for SCE in the nanoscale devices. The proposed model in [20] uses an approximation that decreases the effect of higher weak inversion current but with adding a new factor to the delay processing for the transistor. The exponential dependence of the body factor in [20, 21] also adds new values of delay for the proposed model. The comparison between the proposed model and other models shown in the same figure is given using the same SPICE parameters V_{ds}=1 V, T=300 K, L_{eff}=22 nm, W_{eff}=44 nm, $N_s=2\times10^{20}$ cm^{-3} at the same environment.

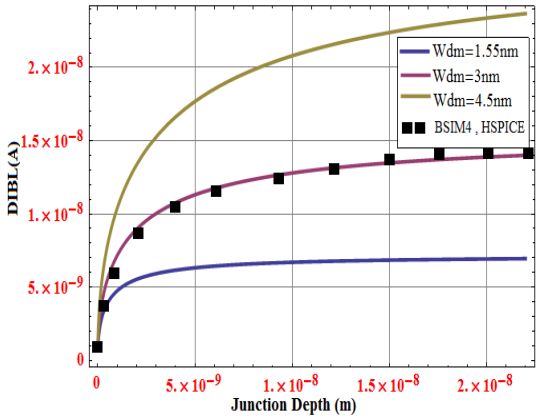

Figure 2. DIBL vs junction depth variation

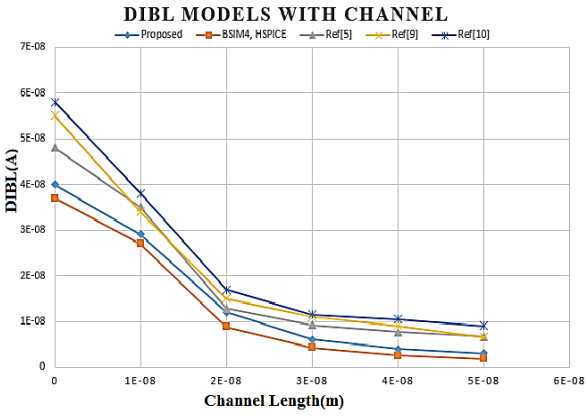

Figure 3. DIBL models with channel length variation

In addition, applying the proposed model using different SPICE parameters is shown in Figure 5. The comparison results show the superiority of the proposed model compared with the same models proposed by BSIM4 using the same SPICE parameters. Simulation results showed that the error percentage was minimized when we applied the new model using higher MOS transistor dimensions due to the lower SCE. In addition, the percentage of error between the new analytical model and the simulated BSIM4 model is increasing to lower MOS dimensions for the increasing of SCE. The percentage error of the proposed model with 32 nm and 45 nm channel lengths is equal to 2.23% and 1.98% respectively using the absolute error method (AEM). On the other hand, the percentage error for the channel length of 16 nm is equal to 4.92% using the HSPICE simulator and the AEM method for error calculation. Hence, the percentage error is also lower than the other models for 16 nm. The proposed subthreshold leakage current model is given for different scales of V_{ds}=0.8 V, T=300 K, W_{eff}=44 nm, N_s=2×10^{20} cm^{-3}.

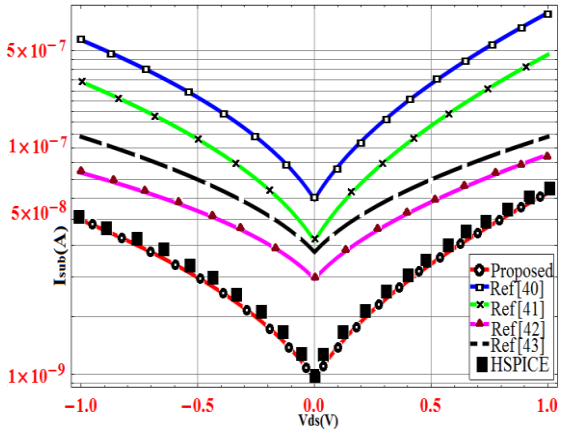

Figure 4. Proposed subthreshold leakage current model vs other models

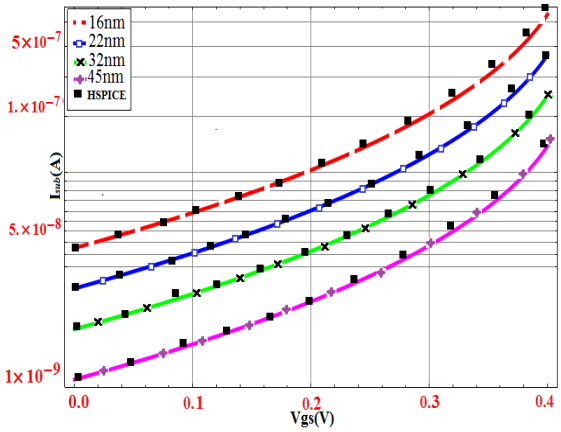

Figure 5. Proposed subthreshold leakage current model for different scales

3.2. Gate leakage current comparison and simulation results

The gate leakage current is simulated also at the drain voltage of 0.8 V, and the gate voltage of 0.2 V. The proposed models are compared with the HSPICE model reported in [19]. In addition, the proposed models are compared with other well-known proposed models with a deep explanation for the reasons of errors in these models and the main factors for the high accuracy and low delay for our proposed models Figure 6 shows the simulation results for the proposed model with HSPICE using the BSIM4 model for the gate to inverted drain leakage vs drain. The same results are given when the gate to inverted source leakage vs the source. The same results are shown in Figure 6. Figure 7 shows the gate to inversion source leakage as a function of drain voltage. The same results are given when the same model applied for the gate to inversion source

leakage as a function of source. From both figures, it seems that the proposed model is so much accurate as of the HSPICE itself. The results of both figures provide a minimum error between the simulation results and the HSPICE to a value equal to 2.84%. The maximum value for the total gate leakage current in reference [19] is equal to 9.68 $\times 10^{-14}$ A. Some of the well-known models are simulated using HSPICE and compared with the proposed model and reference model to show the good agreement for the proposed model compared with the maximum values for these models regarding the value of the gate leakage current for reference [19]. Figure 8 shows the total leakage current for the reference and the proposed models with the models reported in [11-13] references.

3.3. Band-to-Band tunneling leakage current comparisons and simulation

The proposed models for the two types of Band-to-Band leakage current (I_{BTBT}) is simulated also with the same device specification and simulation conditions. The simulation results provide a very good agreement in comparison with the reference model simulation using the HSPICE tool. The maximum value for the BTBT currents that tunnel from the source/drain PN junction with the depletion layer is equal to 5.34×10^{-11} A and 5.38×10^{-11} A. The maximum BTBT current in reference [19] model is equal to 5.65×10^{-11} A. The percentage error for the proposed model and the reference one is equal to 5.6%. Figure 9 shows the proposed model relations for total leakage current with the reference model simulation results using HSPICE. The maximum value of the total leakage current is dominated by the subthreshold leakage and equals to 54.102×10^{-9} A. More details and more references related to the nanoscale transistor could be found in [22-25].

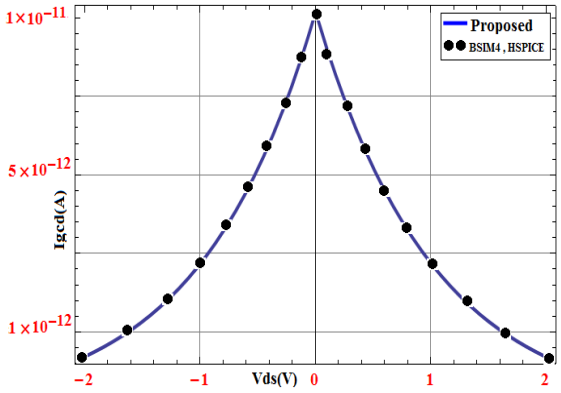

Figure 6. The gate to inverted drain leakage vs. drain voltage

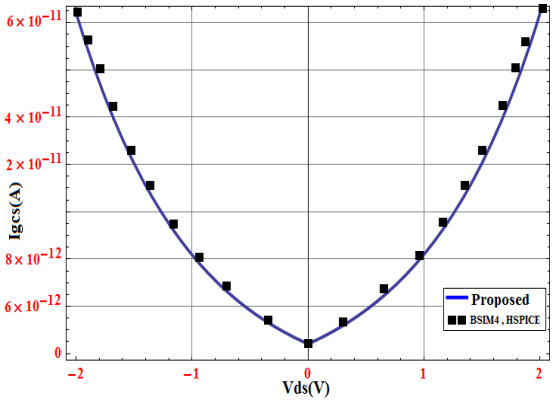

Figure 7. The gate to inversion source leakage as a function of drain voltage

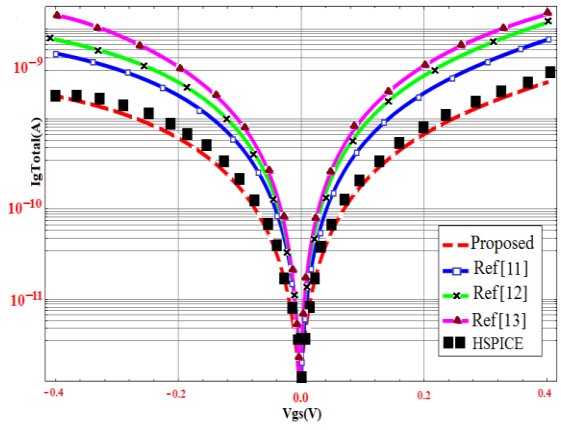

Figure 8. Comparisons with recent models including HSPICE for total gate current

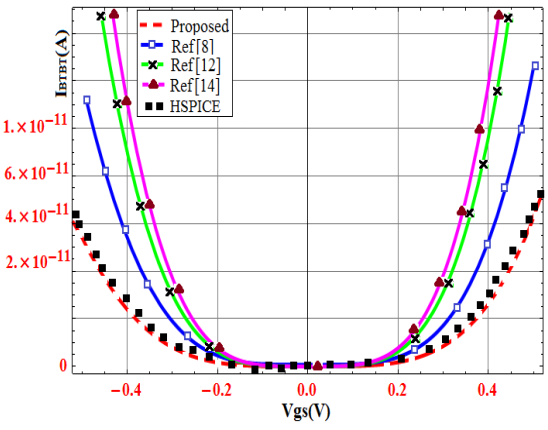

Figure 9. The total BTBT leakage as a function of biasing voltage

4. CONCLUSION

This paper deals with the modeling of leakage current mechanisms of CMOS devices in the sub 100 nm paradigm. The proposed models have been compared with the BSIM4 using HSPICE with very good agreement, the deviation between the simulated model and the BSIM4 is equal to 0.68%. The usage of the insulation layer for the substrate will minimize the leakage current by 47.7%. The Gate leakage (I_G) resources are also modeled too with a great concentration in the method of finding the gate to the inversion channel gate leakage, which is the dominant as we explained in chapter four. We conclude that the gate to substrate leakage current is the smallest type of gate leakage current with a value of 1.5×10^{-12} A. The gate to the substrate will be significant for the future of MOS technology because it depends directly on the tunneling from the oxide insulator through the inversion channel. The gate to inversion channel leakage (I_{GC}) is the only type of gate leakage that depends on the applied gate voltage as shown in chapter three. Using the HiK insulator between the gate and inversion channel in MOS will decrease the gate leakage by 47% of its value in the case of SiO_2 [3]. In addition, using the metal gate in MOS new technology will maximize the efficiency of the transistor by minimizing the value of leakage current due to the gate and BTBT. The error of the proposed model for the total leakage current when compared with the simulation results in HSPICE is equal to 0.37% due to the avoidance of using approximations in derivation for these types of leakage. The Gate leakage will be the significant type of leakage for the future 16 nm MOS transistor.

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