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SPICE model of drain induced barrier lowering in sub-10 nm junctionless cylindrical surrounding gate MOSFET

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ABSTRACT

We propose a SPICE Drain Induced Barrier Lowering (DIBL) model for sub-10 nm Junctionless Cylindrical Surrounding Gate (JLCSG) MOSFETs. The DIBL shows the proportionl relation to the -3 power of the channel length L_g and the 2 power of silicon thickness in MOSFET having a rectangular channel, but this relation cannot be used in cylindrical channel because of the difference in channel structure. The subthreshold currents, including the tunneling current from the WKB (Wentzel-Kramers-Brillouin) approximation as well as the diffusion-drift current, are used in the model. The constant current method is used to define the threshold voltage as the gate voltage at a constant current, $(2\pi R/L_g)\ 10^{-7}$ A for channel length and channel radius *R*. The central potential of the JLCSG MOSFET is determined by the Poisson equation. As a result, it can be seen that the DIBL of the JLCSG MOSFET is proportional to the –2.76 power of the channel length, to the 1.76 power of the channel radius, and linearly to the oxide film thickness. At this time, we observe that the SPICE parameter, the static feedback coefficient, has a value less than 1, and this model can be used to analyze the DIBL of the JLCSG MOSFET.

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1. INTRODUCTION

In order to increase the degree of integration of integrated circuits, efforts are being made not only to develop a design method for a three-dimensional structure but also to fabricate a transistor itself as a three-dimensional structure. Among these efforts, a multi-gate MOSFET is one of the most studied structures [1-3]. A multi-gate MOSFET has the effect of reducing the short channel effects such as the subthreshold swing degradation, threshold voltage roll-off, and drain induce barrier lowering (DIBL) by increasing the number of gates and improving the control ability of the carriers by the gate voltages in the channel. Major manufacturers are using FinFETs as transistors in their three-dimensional integration. FinFETs are structures that increase the controllability of carriers in a channel by fabricating three gates around the channel [4-6]. The graphene nanoribbon has been also studied to use in double gate MOSFET [7].

The miniaturization of the transistor plays an important role in the development of the semiconductor industry, and it is estimated that transistor size will decrease to 5 nm in the future as the development of transistors below 10 nm started in 2017 [8]. The structure that is being developed to reduce the inevitable short channel effects is a cylindrical MOSFET structure [9-11]. A cylindrical MOSFET is a structure that surrounds a channel with the gate and maximizes the controllability of the carriers in a channel by the gate voltage. In particular, many studies have been actively conducted on transistors with a Junctionless Cylindrical Surrounding Gate (JLCSG) structure to prevent a sudden change in the doping

distribution between a source and a channel, and between a drain and a channel [12-15]. The junctionless structure minimizes the source-channel and drain-channel potential barriers by doping the channel with almost the same amount of impurities of an equal type as the doping in the source and drain regions. Such a structure can eliminate the drastic change in the doping distribution that can occur in the process. The junctionless double gate MOSFET having a rectangular channel shows the DIBL is proportional to $L_g^{-3}t_{si}^2t_{ox}$, for channel length L_g, silicon thickness t_{si} and oxide thickness t_{ox} [16]. However this relation cannot be used for the JLCGS MOSFET due to the different channel structure. In this paper, we show the DIBL model using in SPICE for the JLCSG MOSFET by observing the change of the DIBL for channel length, channel radius R, and gate oxide thickness.

The threshold voltage is defined as the gate voltage when the drain current is constant that corresponds to the value of $(2\pi R/L_g)10^{-7}$ A by approximating the channel width as $2\pi R$ in the JLCSG MOSFET. Since the tunneling current is not negligible when the drain current is calculated at sub-10 nm channel length, it is calculated using the Wentzel-Kramers-Brillouin (WKB) approximation. Then the drain current may be obtained by adding the tunneling current and the thermionic emission current consisting of diffusion and drift currents.

Hu et al. analyzed the subthreshold characteristics [17] and Trivedi et al. proposed a current-voltage characteristic model of a junctionless cylindrical structure [18]. However, their analyses were only for channel lengths of 10 nm or more. In this study, we analyze the DIBL phenomenon in the subthreshold region for a JLCSG MOSFET with a sub-10 nm channel length according to the channel size and present an analytical DIBL model that can be used in SPICE. The static feedback coefficient is used as a parameter in the DIBL model of SPICE, and it is less than 1 and mainly uses 0.7 for the DIBL model of CMOSFET. We derive the DIBL model to have the static feedback coefficient η less than 1 for the JLCSG MOSFET.

In Section 2, we will explain the analytical potential distribution, threshold voltage, and DIBL for JLCSG MOSFETs. In Section 3, we will analyze the obtained DIBL according to the channel structure and present the SPICE model. We conclude in Section 4.

2. THE STRUCTURE OF JLCSG MOSFET AND DIBL

Figure 1 shows a JLCSG MOSFET. The JLCSG structure has a cylindrical structure. In this case, the structure between the source/drain and channel region is junctionless, and the doping concentrations of the source and drain region are N_d=10^{20} /cm^3, and the channel is N_d=10^{19} /cm^3. In this paper, the threshold voltage and central potential distribution are compared and analyzed for channel length L_g between 5 nm and 10 nm, channel radius R from 1 nm to 5 nm, and oxide thickness t_{ox} between 0.5 nm and 3 nm. Since there is up-and-down symmetry, the following Poisson equation is used in the region of $0 < r < t_{si}/2$.

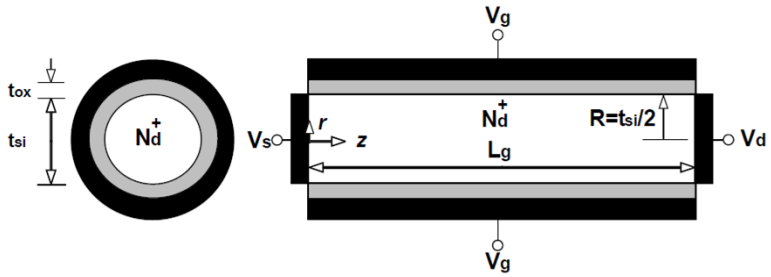

Figure 1. Schematic cross-sectional diagram of a Junctionless Cylindrical Surrounding Gate (JLCSG) MOSFET

$$\frac{\partial^2\phi(r,z)}{\partial r^2}+\frac{1}{r}\frac{\partial\phi(r,z)}{\partial r}+\frac{\partial^2\phi(r,z)}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}} \quad (1)$$

Using the deployment method of Trivedi et al., the central potential is as follows [8].

$$\phi(r=0,z)=Ae^{z/\lambda}+Be^{-z/\lambda}+\eta \quad (2)$$

$$A = \frac{(\phi_{bi} - \eta)(e^{-L_g/\lambda} - 1) - V_d}{e^{-L_g/\lambda} - e^{L_g/\lambda}}$$

$$B = \frac{(\phi_{bi} - \eta)(1 - e^{L_g/\lambda}) - V_d}{e^{-L_g/\lambda} - e^{L_g/\lambda}}$$

$$\lambda = \sqrt{(4\varepsilon_{si} t_{si} + t_{si}^2 C_{ox}) / 16 C_{ox}}$$

$$\eta = V_g - V_{fb} + qN_d t_{si} / 4C_{ox} + qN_d t_{si}^2 / 16\varepsilon_{si}$$

where ϕ_{bi} is the barrier height between source and channel, C_{ox} is the gate oxide capacitance, V_{fb} is the flat-band voltage, and V_g and V_d are the gate and drain voltages, respectively. In the case of the JLCSG MOSFET, most carriers are transported through the center of the channel, so the change in potential energy obtained using the central potential is as shown in Figure 2, depending on the channel length and drain voltage.

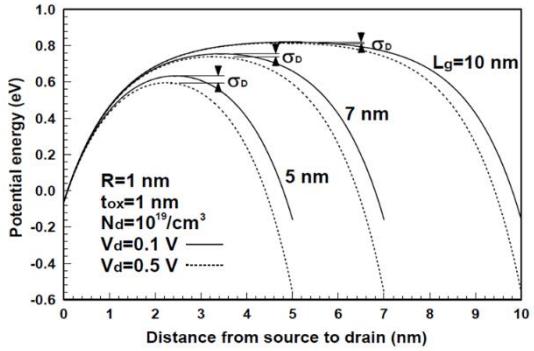

Figure 2. Comparison of potential energy in this model for different channel lengths, under given conditions

As shown in Figure 2, when the channel length decreases, the σ_D, known as the DIBL, increases. In this way, the potential energy varies not only with the channel length but also with the channel radius and the thickness of the oxide film, which will affect the threshold voltage. Though there are various methods to obtain the threshold voltage [19], in this study, the threshold voltage was defined as the gate voltage at the constant drain current. That is to say, the gate voltage at the drain current of (3) is defined as the threshold voltage.

$$I_d = (W / L_g) \times 10^{-7} A = (2\pi R / L_g) \times 10^{-7} A \quad (3)$$

In (3), the drain current I_d consists of the diffusion-drift current $I_{d\text{-}d}$ [20] and the tunneling current I_{tunn} by the WKB approximation and each current model is as follows:

$$I_{d-d} = \frac{2\pi N_d \mu_n kT \left(1 - \exp\left\{\frac{-qV_d}{kT}\right\}\right)}{\int_0^{L_g} \frac{1}{\int_0^R r \exp\left\{\frac{q\phi(r,z)}{kT}\right\} dr} dz} \quad (4)$$

$$I_{tunn} = \left(\frac{qN_d \pi R^2}{6}\right)\left(\frac{2T_t v_{th_t}}{3} + \frac{T_l v_{th_l}}{3}\right) \quad (5)$$

$$T_{t,l} = \exp\left[-2\int_{z_1}^{z_2} \left|\alpha_{t,l}(z)\right| dz\right]$$

$$\alpha_{t,l}(y) = \sqrt{\frac{2m_{t,l}[q\phi(r,z) - E_{fm}]}{\hbar^2}}$$

The variables used here are shown in the previous papers [21, 22]. In the case of conventional MOSFETs with the rectangular channel, σ_D is proportional to the oxide thickness only and is known to be proportional to the -3rd power of the channel length L_g, and the DIBL phenomenon is analyzed using the SPICE parameter η, called the static feedback coefficient [23]. However, in a sub-10 nm JLCSG MOSFET with a cylindrical channel, there is a very small channel length and channel radius. Since the entire channel size affects carrier transport, σ_D can be expressed by the following equation including not only the channel length but also the channel radius.

$$\begin{aligned}\sigma_D &= [V_{th}(V_d = 0.5V) - V_{th}(V_d = 0.1V)] / 0.4 \\ &= A\eta t_{ox} L_g^{-3+x} R^{2-x}\end{aligned} \quad (6)$$

Here, the effect of the channel radius R is also included. In particular, the effect of the channel length and the channel radius is analyzed by the variable x. Because the channel is a cylindrical structure, it will have a different proportional mechanism, compared with a conventional MOSFET with a square structure that the σ_D is proportional to L_g^{-3} . Also, since σ_D has a unit of V / V as shown in (6), there is no displacement dimension, so we set (6) such that the sum of all orders of L_g, t_{si}, and t_{ox} related to displacement is zero. The SPICE DIBL model of the JLCSG MOSFET is presented by obtaining a proper constant A and the x value in (6) when the variation range of the SPICE parameter η is smallest. In the conventional MOSFET, since the value of η is about 0.7, the range of η is derived to be between 0 and 1 for the JLCSG MOSFET.

3. SPICE DIBL MODEL OF THE SUB-10 NM JLCSG MOSFET

Since the diffusion-drift current equation and the validity of the tunneling current proposed in this paper have been confirmed in papers already published [11, 12, 20], the threshold voltage at the drain voltage of 0.1 V and 0.5 V is calculated using (3). And the SPICE model is proposed by observing the DIBL changes in channel length, channel radius, and oxide thickness. Figure 3 shows the variation of DIBL with the channel radius as a parameter in order to observe the change of DIBL with respect to the channel length. In the conventional MOSFET, the DIBL is proportional to L_g^{-3}. But as shown in Figure 3, while the DIBL is proportional to L_g^{-3} at R=1 nm, when R increases to about 5 nm, it is proportional to L_g^{-2}. That is, the change in the channel length in the range of 1 nm ≤ R ≤ 5 nm may be a value between the -2nd and -3rd power. Therefore, it can be shown that the σ_D is proportional to the power of -3 + x ($0 \le x \le 1$) for the channel length as expressed in (6). The channel radius determines the channel width of the JLCSG MOSFET. As the radius of the channel decreases, the entire channel becomes the carrier transport path. Therefore, the channel radius has a significant effect on the current below the threshold voltage.

Figure 4 shows the change in DIBL as a function of channel radius using the oxide thickness as a parameter. At this time, the channel length was 5 nm, and the oxide film thickness was changed from 0.5 nm to 3 nm with an interval of 0.5 nm. As shown in Figure 4, it can be found that the DIBL shows a proportional relationship between the 1st and 2nd power for R depending on the range of R and oxide thickness. Thus, it can be seen that the DIBL is proportional to the power of 2-x ($0 \le x \le 1$) for the channel radius as shown in (6).

Finally, to determine the relationship between the thickness of the gate oxide and the DIBL, the DIBL is shown as a function of oxide thickness in Figure 5 with the channel radius as a parameter at the channel length of 5 nm. In conventional MOSFETs, DIBL is known to be inversely proportional to the gate oxide capacitance. In other words, it is linearly proportional to the oxide thickness. As can be seen in Figure 5, the DIBL changes linearly with oxide thickness when the channel radius changes from 1 nm to 5 nm. Therefore, the expression for σ_D mentioned in (6) is valid.

In the case of a sub-10 nm low doping double-gate MOSFET with a square channel structure, the DIBL is proportional to 2nd power for silicon thickness, -3rd power for the channel length, and 1st power for the oxide thickness [24]. However, in the case of the JLCSG MOSFET, it was observed that the relationship is as shown in (6) due to different channel structure. In conventional MOSFETs, the SPICE parameter η has a value between 0 and 1 (typically 0.7). In this paper, optimal A and x values in (6) are derived so as to have such a range.

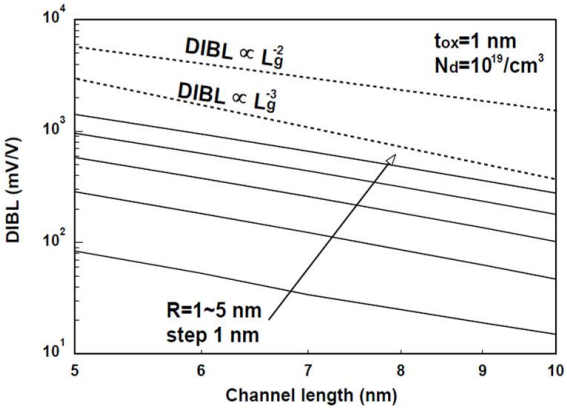

Figure 3. DIBLs for channel length with the channel radius as a parameter for sub-10 nm JLCSG MOSFET. Dotted lines denote the proportional lines for the power of -2 and -3 for the channel length

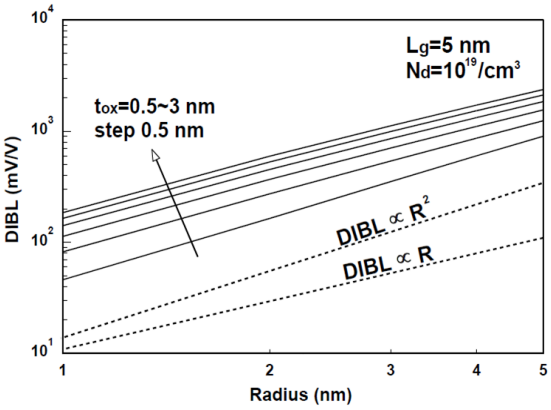

Figure 4. DIBLs for channel radius with the oxide thickness as a parameter for sub-10 nm JLCSG MOSFET. Dotted lines denote proportional lines for the power of 1 and 2 for channel radius

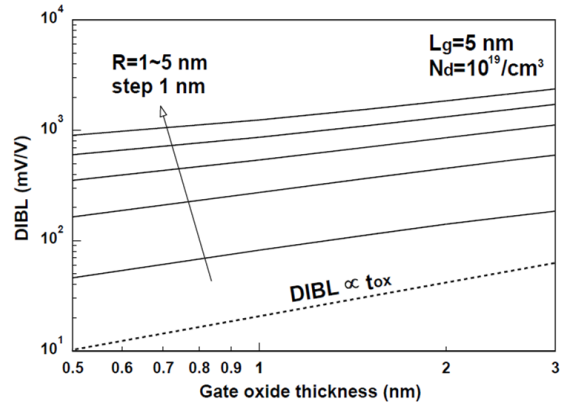

Figure 5. DIBLs for gate oxide thickness with the channel radius as a parameter for sub-10 nm JLCSG MOSFET. The dotted line denotes proportional line for the power of 1 for oxide thickness.

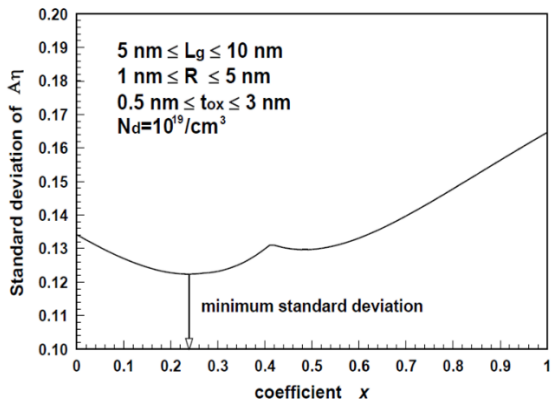

Figure 6. The standard deviation of $A\eta$ to obtain optimum x value in (6) in the range of 5 nm $\leq L_g \leq$ 10 nm, 1 nm $\leq R \leq$ 5 nm, and 0.5 $\leq t_{ox} \leq$ 3 nm.

First, the standard deviations of the value of $A\eta$ in the ranges of 5 nm $\leq L_g \leq$ 10 nm, 1 nm $\leq R \leq$ 5 nm, and 0.5 $\leq t_{ox} \leq$ 3 nm, for x in the range of 0 to 1, are shown in Figure 6. As shown in Figure 6, the value of $A\eta$ shows the minimum value at x = 0.24, so 0.24 is substituted for x in (6) and the maximum value of $A\eta$ was set to A to maintain a value between 0 and 1 for η. The derived value for A was 17.3. As a result, the SPICE DIBL model of the sub-10 nm JLCSG MOSFET obtained in this study is as follows.

$$\sigma_D = 17.3\eta L_g^{-2.76} R^{1.76} t_{ox} \quad (7)$$

In order to investigate the static feedback coefficient η of (7), it is obtained in range of the channel length, channel radius and oxide thickness range used in this paper and shown in Figure 7. As described above, it can be seen that η is limited to a value of between 0 and 1. Since η = 0.7 is generally used in conventional MOSFETs, the SPICE DIBL model of (7) proposed in this paper is reasonable for the JLCSG MOSFET. Figure 7 shows variations of the parameters of channel radius and oxide thickness. Figure 7 (a) shows the case where the channel radiuses are 1 nm and 2 nm, and it can be observed that the range of η does not vary greatly depending on the channel radius. However, as the oxide thickness increases, the value of η decreases and shows nearly constant as shown in Figure 7(b). Therefore, it is found that the DIBL phenomenon can be expressed more accurately using (7) as the oxide thickness increases.

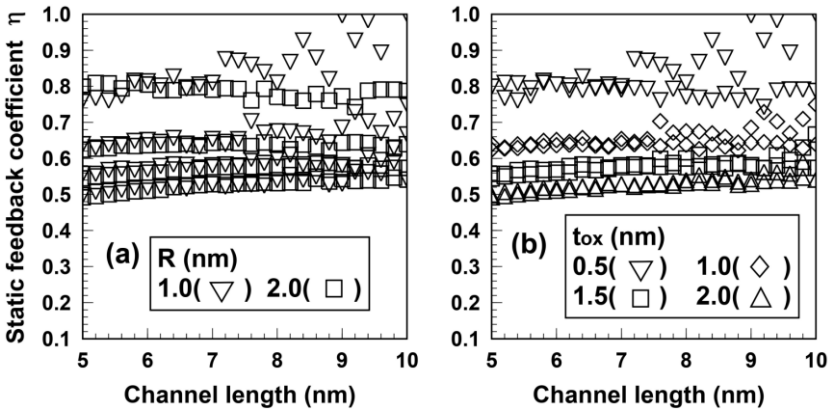

Figure 7. Static feedback coefficients for deviations of the channel radius and gate oxide thickness

In order to verify the validity of (7), we compared the DIBL values of the previous papers [17, 25] with those of this model in Figure 8. Since the static feedback coefficient η is a SPICE parameter having a value of 1 or less, the DIBLs for the minimum value η = 0.1 and the maximum value η = 1.0 are shown in Figure 8 using (7). The solid line denotes the DIBLs at R = 5 nm and t_{ox} = 2 nm and the dotted line at R = 10 nm and t_{ox} = 2 nm. As can be seen in Figure 8, it is confirmed that the DIBLs of Hu et al. were found to be in the range of $0.1 \leqq \eta \leqq 1.0$ of this model at R = 5 nm and t_{ox} = 2 nm, and those of Sharma et al. also fall within the range of $0.1 \leqq \eta \leqq 1.0$. Therefore, it is reasonable to use (7) to calculate the DIBL for JLCSG MOSFET.

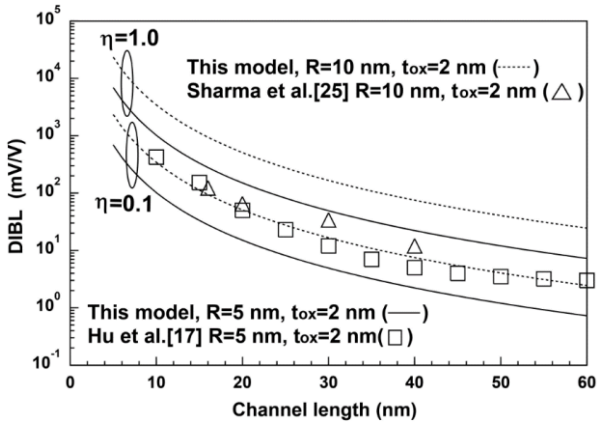

Figure 8. Comparisons of this model with various models for the DIBL of JLCSG MOSFET

4. CONCLUSION

The SPICE DIBL model for the sub-10 nm JLCSG MOSFETs is presented. To this end, the subthreshold current model includes not only the diffusion-drift current but also the tunneling current which cannot be ignored in sub-10 nm channel length. The threshold voltages at drain voltages of 0.1 V and 0.5 V were obtained, and the DIBL was determined according to the channel length, channel radius, and oxide thickness, and then a reasonable range of a static feedback coefficient η available for SPICE was set. Unlike the square structure, the DIBL of the cylindrical structure is not proportional to an integer power for the channel length and the channel radius, so the optimal power for the channel length and the channel radius is obtained for the JLCSG MOSFET. As a result, the change range of the static feedback coefficient is the smallest when the DIBL is the -2.76 power for channel length, the 1.76 power for the channel radius, and the first power for the oxide thickness. Especially, as the oxide film thickness increased, the static feedback coefficient η was almost constant regardless of the change in channel length. For the η value between 0.1 and 1.0 of the SPICE DIBL model proposed in this paper, the DIBLs matches well with other models, so this model can be reasonably used in SPICE for the JLCSG MOSFET.

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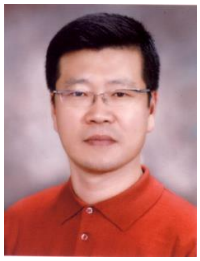

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