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Threshold voltage model for hetero-gate-dielectric tunneling field effect transistors

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ABSTRACT

In this paper, a two dimensional analytical model of the threshold voltage for HGD TFET structure has been proposed. We have also presented the analytical models for the tunneling width and the channel potential. The potential model is used to develop the physics based model of threshold voltage by exploring the transition between linear to exponential dependence of drain current on the gate bias. The proposed model depends on the drain voltage, gate dielectric near the source and drain, silicon film thickness, work function of gate metal and oxide thickness. The accuracy of the proposed model is verified by simulation results of 2-D ATLAS simulator. Due to the reduction of the equivalent oxide thickness, the coupling between the gate and the channel junction enhances which results in lower threshold voltage. Tunneling width becomes narrower at a given gate voltage for the optimum channel concentration of $10^{16}/cm^3$. The higher concentration in the source (N_s) causes a steep bending in the conduction and valence bands compared to the lower concentration which results in smaller tunneling width at the source-channel interface.

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1. INTRODUCTION

As the conventional MOSFETs are scale to the sub-nanometer region, the close proximity between the source and drain reduces the gate control over channel which leads to several problems, such as high subthreshold swing (SS), high leakage current, and short channel effects (SCEs) [1-4]. Tunneling field-effect-transistors (TFETs) are considered one of the attractive devices to replace the conventional MOSFETs in the sub-nanometer region [5, 6] due to its lower SS value (< 60 mV/decade) at room temperature. This advantage translates into low-voltage operation and results in low stand-by power dissipation which makes TFET more energy-efficient compared to the conventional MOSFETs [7-9]. Despite the better SS, there are two main drawbacks with TFETs; one is the low ON- current which degrades the performance and the other is the large ambipolar current [10].

Thus, to increase the ON-current and reduce the ambipolar current, researchers have introduced hetero-gate-dielectric (HGD) TFETs [11-15]. This device gives lower SS without scarifying the chip density. The HGD TFET has different dielectric material at the drain and the source side. The characteristics of HGD TFET device in terms of band bending channel potential, electric field, ON-current and SCEs experimentally and analytically have been studied extensively in the literature [16-19]. The threshold voltage of the TFET device is one of the most important electrical parameter. Researchers have extracted the value of threshold

voltage either using constant current method (at gate voltage for which I_D=10^{-7} A) or transconductance change method [20, 21]. Since, the constant current method uses an arbitrary value; hence, it has no practical meaning. In the transconductance change method, the threshold voltage is defined as the gate voltage corresponding to maxima of the transconductance derivative. The main drawback of this method is that the plot has much numerical derivative noise which makes its impractical. Analytical models are helpful to design, simulate and provide a further insight on the working electrical characteristics of the device. Therefore, to understand the overall performance of a device compact analytical threshold voltage model of HGD TFET structure is needed but no analytical model is available in the literature for HGD TFET in best of our knowledge except few analytical models available for TFET [22-25].

In this paper, compact analytical models for the channel potential, tunneling width and the threshold voltage of the HDG TFET have been derived using parabolic potential approximation method to solve the 2-D Poisson's equation. The accuracy of the proposed models are validated by comparing the model results with the results available in the literature as well as 2-D ATLAS TCAD simulator results with a close agreement. It is observed that as the length of high-k region near the source reduces, the conduction band becomes shallow which makes band-to-band tunneling difficult and increases the threshold voltage. The structure of this paper is given as follows: Section 2 describes the analytical models for the channel potential, tunneling width and threshold voltage. Section 3 describes the simulation results whereas section 4 concludes the paper.

2. PROPOSED ANALYTICAL MODELS

Figure 1 shows the schematic of the proposed n-channel HGD TFET and its coordinate system. The whole channel region is divided into two: High-k region near source to control the tunnelling current (relative permittivity of kr_1 and oxide thickness, tox_1=3 nm), Low-k region near drain (relative permittivity of kr_2 and oxide thickness, tox_2=3 nm) to minimize the ambipolar current. The doping concentration of p+ source region is 10^{20}/cm^3, channel region is 10^{16}/cm^3 and drain region n+ is 10^{18}/cm^3. L_1 is the length of high-k region and (L-L_1) is length of low-k region respectively where L is total gate length. The quantum confinement effect in the analysis is ignored because the film thickness (t_{si}) is greater than 3 nm. Neglecting the fixed carrier oxide change, the 2-D Poisson equation for n-channel HGD TFET in High-k and Low-k (SiO_2) regions are given as [18].

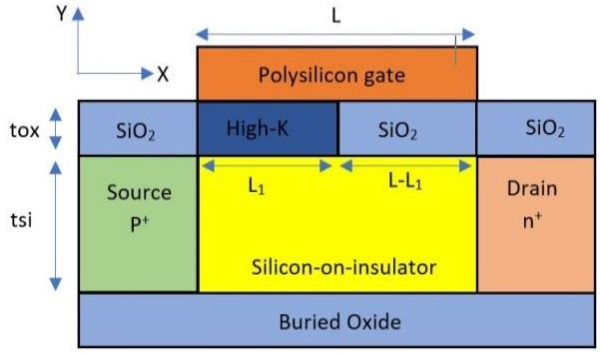


Figure 1. Schematic of the n-channel HGD TFET device

$$\frac{d^2\varphi_{j(x,y)}}{dx^2} + \frac{d^2\varphi_{j(x,y)}}{dy^2} = \frac{-qN_{cj}}{\epsilon_{si}} \quad (1)$$

Where, the subscript j takes value 1 and 2 for High-k and Low-k regions respectively, $\varphi_{j(x,y)}$ is the 2-D electrostatic potential, ϵ_{si} is the dielectric constant of the silicon, $N_{cj} = N_c$ is the channel doping concentration. Assuming, a parabolic potential profile along the film thickness (i.e. along y-direction), the 2-D electrostatic potential in the channel can be expressed as [18]:

$$\varphi_{j(x,y)} = a_0 + a_{j1}y + a_{j2}y^2 \quad (2)$$

Where, a_{0j}, a_{j1}, a_{j2} are constants and function of x-only. These constants can be determined by using the following Boundary Conditions (BCs):

$$\left.\frac{d^2\varphi_{j(x,y)}}{dy^2}\right|_{y=0} = 0,\ \varphi_{j(x,y)}\big|_{y=\frac{t_{si}}{2}} = \phi_{sj(x)},\ \left.\frac{d^2\varphi_{j(x,y)}}{dy^2}\right|_{y=\frac{t_{si}}{2}} = -\frac{C_{ox1}}{\epsilon_{si}}\left[V'_{GSf_j} + \phi_{Sj(x)}\right]$$

Where $\phi_{Sj(x)}$ is surface potential, $V'_{GSf_j} = V_{GS} - V_{fb}$. V_{fb} is the flat-band voltage which is given as

$$V_{fb} = \phi_m - \left[x + \frac{E_g}{2} + \frac{kT}{q}\ln\left(\frac{N_c}{n_i}\right)\right] \quad (3)$$

ϕ_m is the metal work function, x is the silicon electron affinity and E_g is forbidden gap of Si. Using, these Boundary conditions, we get

$$a_{0j} = \phi_{sj(x)} - a_{j2}\frac{t_{si}}{4}^2,\ and\ a_{j2} = -\frac{C_{oxj}}{\epsilon_{si}t_{si}}\left(V'_{GSf} - \phi_{Sj(x)}\right) \quad (4)$$

Substituting (2) into (1), the surface potential $\phi_{Sj(x)}$, in the respective region, must satisfy the following 2-D scaling equation

$$\frac{d^2\phi_{sj(x)}}{dx^2} - \frac{1}{\lambda^2_j}\phi_{Sj(x)} + \frac{\sigma_j}{\lambda^2_j} = 0 \quad (5)$$

Where $\lambda_j = \sqrt{\frac{\epsilon_{si}t_{si}}{2C_{oxj}}}$ is known as characterise length or scaling length, $C_{oxj}=(\varepsilon_{oxj}/t_{oxj})$, σ_j is long channel surface potential and given as

$$\sigma_j = -\frac{qN_c}{\epsilon_{si}}\lambda_j^2 - V'_{GSf}$$

The general solution of the differential equation (5) is expressed as:

$$\phi_{Sj(x)} = A_j e^{\frac{x}{\lambda_j}} + B_j e^{-\frac{x}{\lambda_j}} + \sigma_j \quad (6)$$

Where A_j and $B_j$are constant and determined using the BCs:

$$\phi_{Sj(x=0)}\big|_{source\ end} = V_{bi1}\ ,\phi_{Sj(x=L)}\big|_{drain} = V_{bi2} + V_{ds}$$

$$\left.\frac{d\varphi_{s1}}{d_x}\right|_{x=L1} = \left.\frac{d\varphi_{s2}}{d_x}\right|_{x=L1}\ ,\ \text{and}\ \phi_{S1(x=L1)} = \phi_{S2(x=L1)} \quad (7)$$

Where, $V_{bi2} = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right)$, $V_{bi1} = -\frac{kT}{q}\ln\left(\frac{N_s}{n_i}\right)$.
Using, these four Boundary Conditions, we get;

$$A_2 = \frac{q_{11}-B_2}{\gamma},\ B_2 = \frac{q_{12}}{\gamma e^{-\frac{L}{\lambda 2}} - \delta e^{\frac{L}{\lambda 2}}},\ A_1 = \alpha A_2 + \beta B_2 + R_{11}e^{-\frac{L}{\lambda 1}}\ \text{and}\ B_1 = V_{bi1} - \sigma_1 - A_1$$

Where, $R_{11} = \sqrt{\frac{\sigma_1-\sigma_2}{2}}$, $\alpha = \frac{1}{2}\lambda_1\left[\frac{1}{\lambda_1} - \frac{1}{\lambda_2}\right]e^{L_1\left(\frac{1}{\lambda_2}-\frac{1}{\lambda_1}\right)}$, $\beta = \frac{1}{2}\lambda_1\left[\frac{1}{\lambda_1} + \frac{1}{\lambda_2}\right]e^{-L_1\left(\frac{1}{\lambda_1}+\frac{1}{\lambda_2}\right)}$, $q_{11} = R_{11}e^{-\frac{2L_1}{\lambda_1}} + \sigma_1\left(e^{\frac{L_1}{\lambda_1}} - \frac{1}{2}\right) + \frac{\sigma_2}{2} - Vb_{i1}e^{-\frac{L_1}{\lambda_1}}$, $q_{12} = (Vb_{i2} + Vd_s - \sigma_2)\gamma - q_{11}e^{\frac{L}{\lambda_2}}\gamma = 2\alpha Sinh\left(\frac{L_1}{\lambda_1}\right) - e^{\frac{L_1}{\lambda_1}}$, $\delta = 2\beta Sinh\left(\frac{L_1}{\lambda_1}\right) - e^{-\frac{L_1}{\lambda_1}}$

Therefore, electrostatic potential in the respective region is given as;

$$\varphi_{j(x,y)} = \phi_{sj}\left[1 + \frac{C_{oxj}}{\epsilon_{si}t_{si}}\left(\frac{t_{si}^2}{4} - y^2\right)\right] + \frac{C_{oxj}}{\epsilon_{si}t_{si}}V_{gsf}\left(\frac{t_{si}^2}{4} - y^2\right) \quad (8)$$

At the interface, $y = \frac{t_{si}}{2}$ (8) reduces to $\varphi_j\left(x, \frac{t_{si}}{2}\right) = \phi_{sj}(x)$. The centre potential is obtained for y=0 in (8).

From analysis it is observed that surface potential is smaller than the centre potential particularly at the source and drain ends respectively. Tunnelling barrier width (w_b) is an important parameter to determine the threshold voltage of the TFET. Tunnelling width exhibits a transition from strong dependence to weak dependence on the gate voltage at threshold voltage. w_b is the lateral distance between the source channel

interface ($x = 0$) and the point in the channel when surface potential changes by $\left(\frac{E_g}{q}\right)$. Neglecting source/drain depletion region due to heavy doping, the tunnelling width is obtained after solving eqn. (8) and given as;

$$\frac{w_b}{\lambda_1} = \ln\left[\frac{\delta_1}{2}\left\{1 + \sqrt{1 - \frac{4\delta}{\delta_1^2}}\right\}\right] \tag{9}$$

Where, $\delta = \left(\frac{B_1}{A_1}\right)$ and $\delta_1 = \frac{\left(A_1 + B_1 - \frac{Eq}{q}\right)}{A_1}$

The physical definition of threshold voltage V_{th} for TFETs is the gate voltage which indicates the transition between the strong control and weak control of the tunneling energy barrier width at the source tunnel junction [20]. Tunneling barrier width exhibits a transition from strong dependence to weak dependence on gate voltage at gate threshold voltage. At this inflection point, x = w_b and the surface potential reaches to value of $V_{ds} + \frac{kT}{q}\ln\frac{N_d}{N_c}$ [23]. Substituting $x \cong w_b$ in eqn. (8) and equating it to value of $\frac{kT}{q}\ln\frac{N_d}{N_c}$, the analytical expression for the threshold voltage is;

$$V_{th} = \frac{h_{11} - \sqrt{h_{11}^2 - L * h_{12}}}{2} \tag{10}$$

Where, $h_{11} = \frac{\left(\frac{Eq}{q}\right) + \delta_{11}\delta_{14} + \delta_{12}\delta_{13} - (\alpha_{11}\delta_{12} + \delta_{11} + \delta_{11}\delta_{14} - \delta_{13})}{\delta_{12} + \delta_{14} - \delta_{12}\delta_{14}}$, $h_{12} = \frac{\alpha_{11}\delta_{11} + \alpha_{11}\delta_{13} - \alpha_{11}\left(\frac{Eq}{q}\right) - \delta_{11}\delta_{13}}{\delta_{12} + \delta_{14} - \delta_{12}\delta_{14}}$

$\alpha_{11} = V_{ds} + \frac{kT}{q}\ln\frac{N_d}{N_c} - \frac{qN_c}{\epsilon_{si}}\lambda_1^2 - V_{fb}$, $\delta_{11} = \alpha\xi_{13} + \beta\xi_{11} + R_{11}e^{-\frac{L_1}{\lambda_1}}$, $\delta_{12} = \beta\xi_{12} - \alpha\xi_{14}$, $\delta_{13} = V_{bi1} - \frac{qN_c}{\epsilon_{si}}\lambda_1^2 - V_{fb} - \delta_{11}$, $\delta_{14} = (1 - \delta_{12})$, $\xi_{11} = \left(\frac{\eta_{12}}{\eta_{14}}\right)$, $\xi_{12} = \left(\frac{\eta_{13}}{\eta_{14}}\right)$, $\xi_{11} = \frac{\eta_{11} - \xi_{11}\delta}{\gamma}$, $\xi_{11} = \left(\frac{e^{-\frac{L_1}{\lambda_1}} + \xi_{12}\delta}{\gamma}\right)$, $\eta_{11} = \left(R_{11}e^{-\frac{2L_1}{\lambda_1}} - V_{bi1}e^{-\frac{L_1}{\lambda_1}}\right) + \left(\frac{qN_c}{\epsilon_{si}}\lambda_1^2 - V_{fb}\right)\left(e^{-\frac{L_1}{\lambda_1}} - \frac{1}{2}\right) + \frac{1}{2}\left(\frac{qN_c}{\epsilon_{si}}\lambda_1^2 + V_{fb}\right)$, $\eta_{12} = (V_{bi2} + V_{ds})\gamma - \left(\frac{qN_c}{\epsilon_{si}}\lambda_2^2 + V_{fb}\right)\gamma - \eta_{11}$, $\eta_{13} = \gamma - e^{-\frac{L_1}{\lambda_1}}$, $\eta_{14} = \gamma e^{-\frac{L}{\lambda_2}} - \delta e^{\frac{L}{\lambda_2}}$

3. RESULTS AND ANALYSIS

The proposed analytical models are simulated for the following values; L=50 nm, t_{ox1}=t_{ox2}=3 nm, t_{si}=10 nm, V_{ds}=0.7 V, N_s=10^{20} /cm^3, N_d=10^{18} /cm^3, N_c=10^{16} /cm^3 unless and until specified. As seen from Figure 2, a sharp band bending occurs for t_{ox1}=3 nm and t_{ox2}=5 nm due to reduction of equivalent oxide thickness which enhances the coupling between the gate and the channel junction.

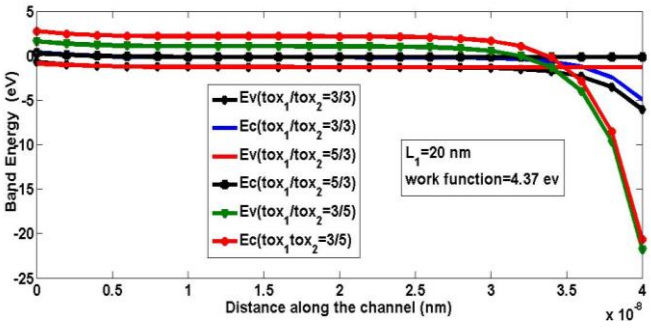
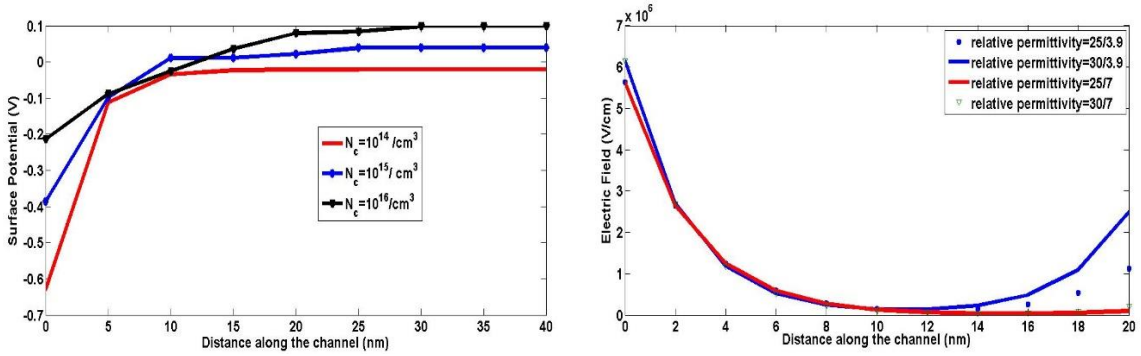


Figure 2. Band diagram for different combination of oxide thickness in two regions

The surface potential mainly varies within 10 nm from source-channel interface that is entirely in high-k region whereas away from tunneling space (mainly in low-k region) it remains almost constant which reflects that tunneling is only controlled by high-k dielectric. This finding suggests that the optimum tunneling length is set to be at 10 nm for higher ON current. Figure 3(a) predicts that the surface potential takes larger value when the channel concentration is 10^{16}/ cm^3. The effect of Nc on surface potential mainly occurs in high-

k region for x≤10 nm. This result gives the optimum value of the channel doping in the HGD TFET device. From Figure 3(b) it is observed that electric field takes larger value when high-k region is occupied by higher dielectric material and the lateral electric field reduces along the channel and takes minimum value in the middle of the channel. The stronger electric field near the source-channel interface enhances tunneling probability whereas lower electric field near drain lowers the ambipolar current. The comparison results of the tunneling width of our proposed model with the 2-D Silvaco simulator and ref [16] results are shown in Figure 4. A slight difference between proposed and ref [16] results is due to structural difference whereas a good agreement with the Silavco 2-D simulation results is observed. For the fair comparison, the simulation is performed for the same value of the parameters as reported in the ref. [16]. The surface potential close to the source end becomes more abrupt due to increased doping concentration ratio between the source and drain regions, which results in improved electrical characteristics and narrow tunneling width which results in lower threshold voltage irrespective of the channel length Figure 5(a). As the length of high-κ region reduces, conduction band becomes shallow which makes band-to-band tunneling difficult and increases the threshold voltage Figure 5(b). Table 1 gives the comparison results of the proposed threshold voltage model with ref [13] results. The two results show close proximity with slight difference due to dual material gate in ref. [13]. For fair comparison we have taken L=50 nm, L_1=8 nm, kr_2=21, kr_1=3.9, metal work function 4.0 eV and 4.4 eV as suggested in ref. [13]. Increased relative dielectric constant in high-κ region results in stronger control of gate over the channel which gives larger carrier tunnel from source to channel and hence lowers the threshold voltage irrespective of the metal type Figure 5(c). This reduction is more for lower work function gate metal due to larger band overlap which reduces the tunneling width and increases the tunneling probability at the source side. Figure 5(d) shows the comparison between proposed model results and 2-D ATLAS simulator results with an excellent matching for the higher dielectric gate material due to controlled leakage current. Figure 5(e), shows an excellent matching between two results for V_{ds}=0 V due to absence of DIBL effect whereas appreciable difference is observed for L≤20 nm and V_{ds}=0.7 V due to the negligence of SCEs in proposed model.



(a) (b)

Figure 3. (a) Surface potential along channel for different channel concentration,
(b) Variation of electric field along channel for different relative permittivity combination

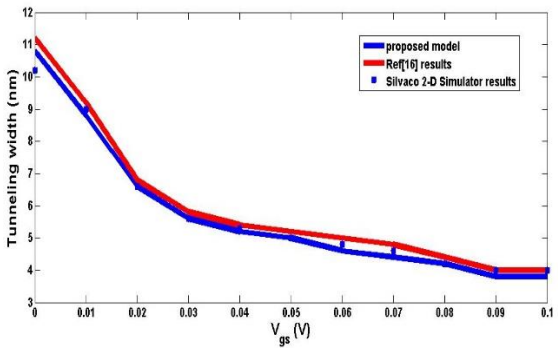


Figure 4. Comparison of tunneling width for proposed model, Silvaco 2-D simulator and ref. [16] results

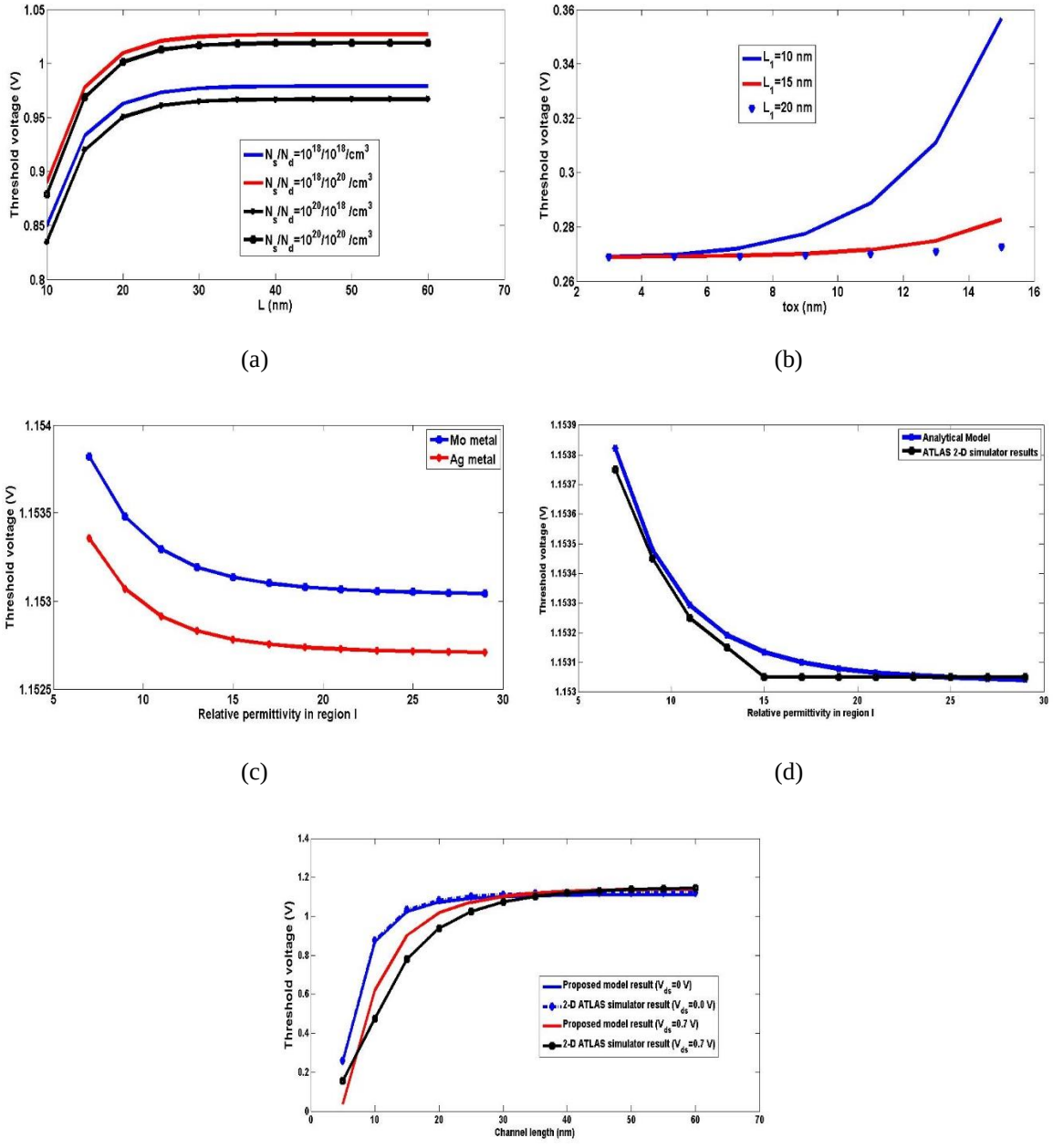


Figure 5. (a) Threshold voltage of HGD TFET device versus channel length for different concentrations combination in the source and drain regions, (b) Threshold voltage variation with t_{ox} for different tunneling length (L_1), (c) Threshold voltage variation with relative permittivity in region I for two gate metals, (d) Comparison of threshold voltage with proposed model and 2-D ATLAS simulator results, (e) Comparison of threshold voltage with proposed and 2-D ATLAS simulator

Table 1. Threshold Voltage comparison with ref. [13] results

Φ_{m1} (eV)	Φ_{m2} (eV)	Threshold voltage (V)	
		Proposed	Ref [13
4.0	4.0	0.349	0.34
4.4	4.4	1.10	0.74

4. CONCLUSION

A two dimensional analytical model of threshold voltage has been proposed using parabolic approximation. The proposed model shows a good agreement with the 2-D ATLAS simulator results. As the gate voltage increases, the tunneling width reduces which lowers the threshold voltage. Threshold voltage of the device also reduces as the dielectric constant of the tunnel space region increases and the length of high-k region increases.

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