

Log-domain electronically-tuneable fully differential high order multi-function filter

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Article Info

Article history:

Received Mar 27, 2019

Revised Oct 9, 2019

Accepted Oct 17, 2019

Keywords:

Active filters
Analog signal processing
Current mode
Log domain

ABSTRACT

This paper presents the synthesis of fully differential circuit that is capable of performing simultaneous high-pass, low-pass, and band-pass filtering in the log domain. The circuit utilizes modified Seevinck's integrators in the current mode. The transfer function describing the filter is first presented in the form of a canonical signal flow graph through applying Mason's gain formula. The resulting signal flow graph consists of summing points and pick-off points associated with current mode integrators within unity-gain negative feedback loops. The summing points and the pick-off points are then synthesized as simple nodes and current mirrors, respectively. A new fully differential current-mode integrator circuit is proposed to realize the integration operation. The proposed integrator uses grounded capacitors with no resistors and can be adjusted to work as either lossless or lossy integrator via tuneable current sources. The gain and the cutoff frequency of the integrator are adjustable via biasing currents. Detailed design and simulation results of an example of a 5th order filter circuit is presented. The proposed circuit can perform simultaneously 5th order low-pass filtering, 5th order high-pass filtering, and 4th order band-pass filtering. The simulation is performed using Pspice with practical Infineon BFP649 BJT model. Simulation results show good matching with the target.

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1. INTRODUCTION

Filters in the analog domain are considered to be essential blocks in nearly any electronic system including communications, biomedical, instrumentation, and measurement applications. Both current mode and voltage mode design techniques have been widely used to realize and implement such filter circuits [1-8]. The very attractive features current-mode (CM) continuous-time circuits have, ensured increasing demand on current mode filters. Among these features are; high linearity, wide dynamic range, low distortion, low operating voltages, low power consumption, and high frequency performance [9-11]. The relative ease of electronically tune CM circuits is another important feature that results in simpler systems architecture.

Device-based CM circuits are being continuously used to synthesis different analog signal processing functions. Current conveyors of 1st, 2nd, and 3rd generations (CCI, CCII, CCIII), 2nd generation current controlled current conveyors (CCCII), transconductance amplifiers (OTA), and the four terminal floating nullor (FTFN) are examples of popular analog blocks that are being widely used in implementing CM filters [4, 5, 8, 12, 13]. However, high order analog filters based on such active elements usually suffers from relatively lower frequency range, limited ability to be tuned and limited performance. This is in addition

to the need of including resistors within the design which will limit the minimization of the area of the integrated system [14].

On the other hand, log-domain circuits and since they were invented received considerable attention as a powerful technique of realizing analog signal processing functions using bipolar junction transistors (BJT's) [15]. This is mainly due to the additional merits log-domain circuits considered to have including lower sensitivity to temperature variations, larger bandwidth, higher density and ease of tuning [16]. Log-domain circuits are based on the dynamic translinear loop principle (dynamic TLP) presented by Adams [17] as a modified technique of the original TLP method presented by Gilbert [18]. In the dynamic TLP method, capacitors are connected within intersections of the translinear loops which utilize the exponential-logarithmic characteristics of a BJT. Many examples of log-domain high-order filters have been presented in the literature. In [19], for instance, the design of a log-domain current-mode 3rd order elliptic filter was introduced. This filter design was based on Seevinck type dummy inputs and used the state space representation as synthesis method. The proposed filter uses 42 npn transistors with 36 current sources and 6 capacitors. The reported simulation results of that filter show good agreement with expected response for 100 KHz corner frequency. Another current-mode CMOS-based 3rd order LPF was reported in [20], where two ladder filter designs were proposed using the all-pole and Elliptic approximations. The all-pole filter was consisting of 31 transistors and 3 grounded capacitors. The elliptic filter, on the other hand, was consisting of 53 transistors with 3 capacitors also. In both reported designs, one current source was used for biasing and tuning. To provide necessary copies of the current source PMOS current mirrors were used. Both reported designs uses no resistors and were operated at a voltage level of 1.5 V. The input and output signals in that design were non-differential. Another high-order low pass filter (LPF) was presented in [14]. The reported design used the RLC ladder network prototype together with the signal flow graph (SFG) method to achieve the filter design. The resulted design uses lossy and lossless integrators with no resistors. In that paper, researchers presented designs for a 5th order LPF in addition to a 6th band-pass filter (BPF). The designed LPF used 37 npn-BJT's with 5 capacitors and 22 copies of biasing current source with different weights. Though, the input and output signals of that reported filter were non-differential. Another interesting generic design for implementing high order filters is the one presented in [21]. The reported design utilizes log-domain CM circuits and is capable of providing four different topologies that can offer simultaneous high-pass, band-pass and low-pass filter functions. The integrator element used in that design is the exponential cell reported by Frey [22].

In this paper, the design of new fully-differential log-domain CM multi-function high order multi-filtering function is presented. The resulting circuit can simultaneously realize high-pass filter (HPF), low-pass filter (LPF), and band-pass filter (BPF) functions. The main added value of the proposed design is the differential nature of the input and output signals which makes the design most suitable for high-frequency analog signal processing. For the input and output signals to be differential is of critical importance mainly to minimize the harmonic distortion and to have higher rejection of common-mode noises [23]. This is in addition to the ease of synthesis and tune generalized higher order filters using the presented design methodology. The following section discusses the design methodology of the high order LPFs. The integrator circuit is presented in section three. Simulation results of the realization of 5th order Chebyshev and Butterworth LPFs are presented and discussed in the fourth section of this paper. Finally, conclusions are summarized in the last section.

2. DESIGN METHODOLOGY

The transfer function of a n^{th} order LPF may be represented mathematically as

$$T(s) = \frac{K}{B(s)} = \frac{K}{s^n + a_{n-1}s^{n-1} + \dots + a_0} \quad (1)$$

where K , a_0 , a_1 , ..., a_{n-1} are constants. The denominator $B(s)$ is usually presented for the specific filter type in tabulated results factored into first and second order polynomials [24]. These filter functions can be easily represented in canonical SFG with n cascaded integrators together with pickoff and summing nodes forming feedback loops. First, the general transfer function presented by (1) is presented in as

$$T(s) = \frac{Ks^{-n}}{1 + a_{n-1}s^{-1} + \dots + a_0s^{-n}} \quad (2)$$

In the case of a 5th order LPF, the transfer function can be then written as

$$T(s) = \frac{Ks^{-5}}{1 + a_4s^{-1} + a_3s^{-2} + a_2s^{-3} + a_1s^{-4} + a_0s^{-5}} \quad (3)$$

Applying Mason’s gain formula [25], the transfer function in (3) can then be easily represented in the form of a SFG as shown in Figure 1, with b_1 to b_5 are all constants representing gains of the feed-forward integrators. Out of this SFG a set of transfer functions representing different filtering functions can be directly obtained depending on the node from which the output signal is taken as given in Table 1. The constants b_1 to b_5 can then be directly mapped to the constants a_0 to a_4 through direct comparison with (3).

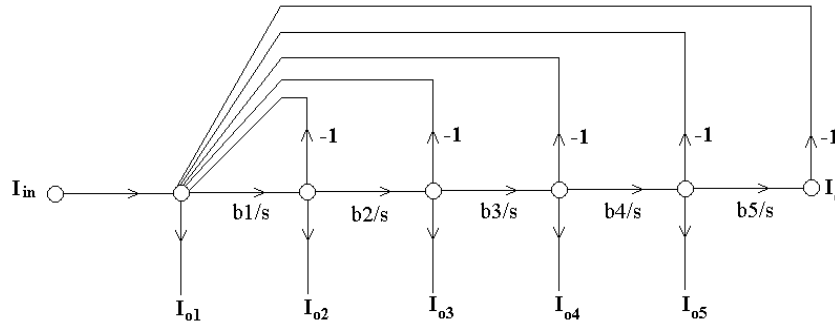


Figure 1. Signal flow graph representing a 5th order LPF

Table 1. Filter functions obtained from SFG presented in Figure 1

Output node	Transfer function	Filtering function
I_o	$\frac{b_1 b_2 b_3 b_4 b_5}{s^5 + b_1 s^4 + b_1 b_2 s^3 + b_1 b_2 b_3 s^2 + b_1 b_2 b_3 b_4 s^1 + b_1 b_2 b_3 b_4 b_5}$	5 th order LPF
I_{o1}	$\frac{b_1 b_2 b_3 b_4 b_5}{s^5}$	5 th order HPF
I_{o2}	$\frac{b_1 b_2 b_3 b_4 b_5}{b_1 s^4}$	Non-symmetrical BPFs
I_{o3}	$\frac{b_1 b_2 b_3 b_4 b_5}{b_1 b_2 s^3}$	
I_{o4}	$\frac{b_1 b_2 b_3 b_4 b_5}{b_1 b_2 b_3 s^2}$	Non-symmetrical BPFs
I_{o5}	$\frac{b_1 b_2 b_3 b_4 b_5}{b_1 b_2 b_3 b_4 s}$	
I_{in}	$\frac{b_1 b_2 b_3 b_4 b_5}{s^5 + b_1 s^4 + b_1 b_2 s^3 + b_1 b_2 b_3 s^2 + b_1 b_2 b_3 b_4 s^1 + b_1 b_2 b_3 b_4 b_5}$	

Realizing this SFG in current-mode becomes straight forward; any summing node can be realized using a single circuit node, whereas any pickoff point can be realized with a current mirror. The integrators are realized using lossy/lossless current-mode integrators (CIs). To serve this purpose, a new fully differential CM integrator is presented. The integrator uses grounded capacitors with no resistors and can be configured either as a lossless or a lossy integrator with adjustable cutoff frequency via biasing currents. This ease of realization together with the many attracting features current-mode circuits have, made them suitable choice for implementing high performance filters. Following the same analogy, any set of nth order filter functions can then be directly realized using current-mode integrators and current mirrors.

3. PROPOSED INTEGRATOR CIRCUIT

Number of designs for continuous-time CM integrator circuits can be found in the literature. Examples of these designs can be found in references [26-35]. One very attractive design for high frequency applications is the current-mode integrator circuit proposed by Seevinck [26]. The Seevinck’s integrator is a class AB differential integrator that consists mainly of two translinear loops and two grounded capacitors. The unity-gain bandwidth f_{ug} of the integrator is limited only by the used transistor’s cutoff frequency f_T and is tunable via DC bias current I_{DC} according to the following relation

$$f_{ug} = \frac{I_{DC}}{2\pi C V_T} \tag{4}$$

where V_T is the thermal voltage and C is a grounded capacitor. However, Seevinck's integrator as presented by Seevinck [26] works only for very high frequency range as lossless integrator and hence cannot be directly used to give the lossy integration.

Figure 2 represents the proposed fully differential modified Seevinck's integrator circuit. This integrator consists basically of two translinear loops; the first loop is formed from transistors Q_{1c} , Q_{2c} , Q_{3c} , and Q_{4c} or Q_{15c} , and the second is formed from Q_{11c} , Q_{12c} , Q_{13c} , and Q_{4c} or Q_{5c} . Depending on these two loops, and with all base currents being neglected, we can write

$$I_{cq4m} \cdot I_{A3} = I_{o1} \cdot [I_{o2} + i_{c2} + I_{X3}] \tag{5}$$

and

$$I_{cq5m} \cdot I_{A3} = I_{o2} \cdot [I_{o1} + i_{c1} + I_{X3}] \tag{6}$$

where I_{cq4m} and I_{cq5m} are the currents flowing through the collector of transistors Q_{4c} and Q_{5c} respectively. These two currents are forming the input currents I_{in1} and I_{in2} to the integrator and, in turn, could be considered as the output currents of a previous integrator stage. The currents I_{A3} and I_{X3} are dc tuning currents, and i_{c1} and i_{c2} are the currents flowing through the capacitors C_1 and C_2 respectively.

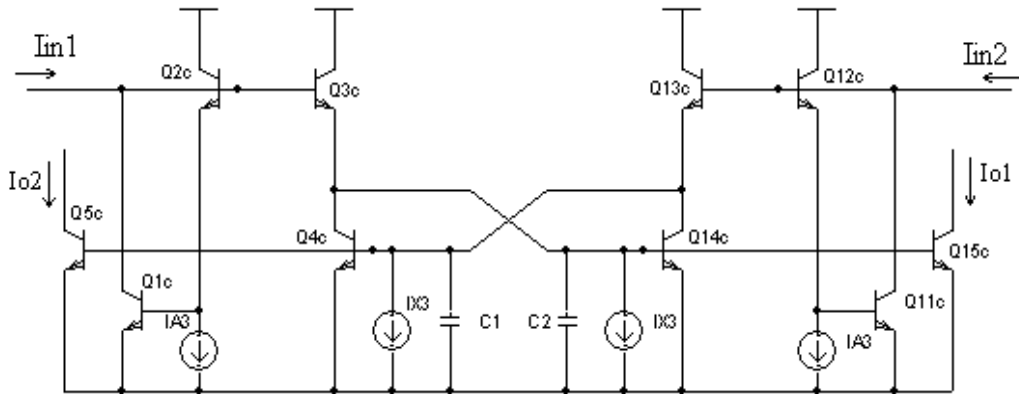


Figure 2. Proposed fully differential Integrator circuit

Utilizing the logarithmic relationship of BJT, we can express the current i_{c1} in terms of the output current I_{o1} as

$$i_{c1} = C_1 \frac{d}{dt} \left(V_T \ln \frac{I_{o2}}{I_s} \right) = C_1 V_T \frac{1}{I_{o2}} \frac{dI_{o2}}{dt} \tag{7}$$

Substituting (7) in (5), we get

$$I_{cq4m} I_{A3} = I_{o1} I_{o2} + C_1 V_T \frac{dI_{o1}}{dt} + I_{o1} I_{X3} \tag{8}$$

Similarly, for the second translinear network, we have

$$I_{cq5m} I_{A3} = I_{o1} I_{o2} + C_2 V_T \frac{dI_{o2}}{dt} + I_{o2} I_{X3} \tag{9}$$

Assuming the two capacitors to be equal and subtracting (9) from (8) results in

$$I_{A3} [I_{cq4m} - I_{cq5m}] = C V_T \frac{d[I_{o1} - I_{o2}]}{dt} + I_{X3} [I_{o1} - I_{o2}] \tag{10}$$

Defining I_{di3} and I_{do} as the differential input and differential output currents of the integrator, the (10) can then be rewritten in the s-domain as

$$\frac{I_{do}}{I_{di3}} = \frac{I_{A3}/(CV_T)}{s+I_{X3}/(CV_T)} = \frac{a_3}{s+b_3} \quad (11)$$

where a_3 and b_3 are independent tunable constants via current sources I_{A3} and I_{X3} . The (11) is applicable also to all other integrators being used but with replacing the currents I_{di3} , I_{A3} and I_{X3} with their designated ones. Since the current source I_{X3} is not a biasing current, it can be set to tune the cutoff frequency f_c of the integrator to wide range of frequencies. However, the accuracy of this tuning will in fact be affected mainly by the base currents of transistors Q_{4c} and Q_{5c} (or Q_{14c} and Q_{15c}). To make the tuning of f_c more accurate, I_{X3} can be replaced with its effective value expressed as

$$I_{Xeff3} \approx I_{X3} - I_{Base4c} - I_{Base5c} \approx I_{X3} - I_{Base14c} - I_{Base15c} \approx I_{X3} - 2I_{Base} \quad (12)$$

Since the proposed circuit is based on the translinear principle with all base currents neglected, the general performance of the circuit is affected by the actual values of these currents. Thus, to enhance the performance, BJTs with high common emitter current gains h_{fe} should be used. Yet, this may impose conditions on the cutoff frequency of the BJTs and thus limiting the high frequency range of the overall system. Another simpler and more effective way to enhance the performance of the integrators is by readjusting the values of the tuning current sources (I_A and I_X) to partially compensate for the base currents.

4. RESULTS AND DISCUSSIONS

Figure 3 represents the circuit realization of three stages of the filter function circuit represented by the SFG of Figure 1. To keep it clear, only three stages are shown. The extension of this circuit to the 5th order or to any higher order can be simply achieved by cascading the required integrators with the previous ones via necessary current mirrors. The tuning currents are adjusted using frequency scaling to implement a 5th order Butterworth filter with cutoff frequencies set to 460 KHz, 4.6 MHz, and 46 MHz. To achieve these cutoff frequencies, the biasing currents and the tuning currents of the five integrators are adjusted to the values stated in Table 2. In this table the I_X currents are mainly used to cancel the effect of the base currents of the transistors forming the translinear loops. Thus, enhancing the overall performance of the circuit especially in the stop band regions where signal currents are expected to be very small. The capacitors values are taken to be the same and equal to 20 pF. The simulations are carried out assuming room temperature (298 K) and results compare well to the calculated target. These simulations were carried out using the BFP640 from Infineon[®] BJT model parameters as given follows.

BFP640 transistor parameters

IS=.22P TR=.2N VJE=.8 VAF=1000 VTF=1.5 ISC=400F IRB=1.522M CJS=93.4F NE=2 FC=.8 VAR=2 VJS=.6 NC=1.8 RBM=2.707 CJE=227.6F CJC=67.43F XCJC=1 TF=1.8P ITF=0.4 VJC=0.6 MJS=.27 XTI=3 AF=2 BF=450 IKF=.15 BR=55 IKR=3.8M RB=3.129 RE=.6 XTF=10 MJC=.5 EG=1.078 NK=-1.42 KF=72.91P NF=1.025 ISE=21F NR=1 RC=3.061 MJE=0.3

Simulation results of the gain-frequency responses of the HPF and LPF of the presented circuit are illustrated in Figure 4. The simulation results compare well to the calculated target. However, when going deep in the cutoff region, the simulated output reaches a constant minimum level. This is mainly due to the very small current levels resulting in the deep cutoff and is of minor importance. Figure 5 shows the phase responses of the designed filter for both the HPF and LPF functions. The phase performance of the proposed filters show relatively good agreement with the expected phase especially around the cutoff frequencies. This agreement becomes poorer as the frequency of the applied signal enters the cutoff region.

The group delay of both the LPF and HPF functions are shown in Figure 6. In the case of the LPF, the group delay is flat for frequencies up to around the cutoff frequency with a value of about 1.0×10^{-6} sec for 4.6 MHz cutoff frequency. However, for the HPF, the group delay keeps increasing within the stop-band until reaching a maximum around the cutoff frequency and then decreasing within the pass-band. For a cutoff frequency of 4.6 MHz, the group delay is reaching a maximum value of around 5.0×10^{-5} sec.

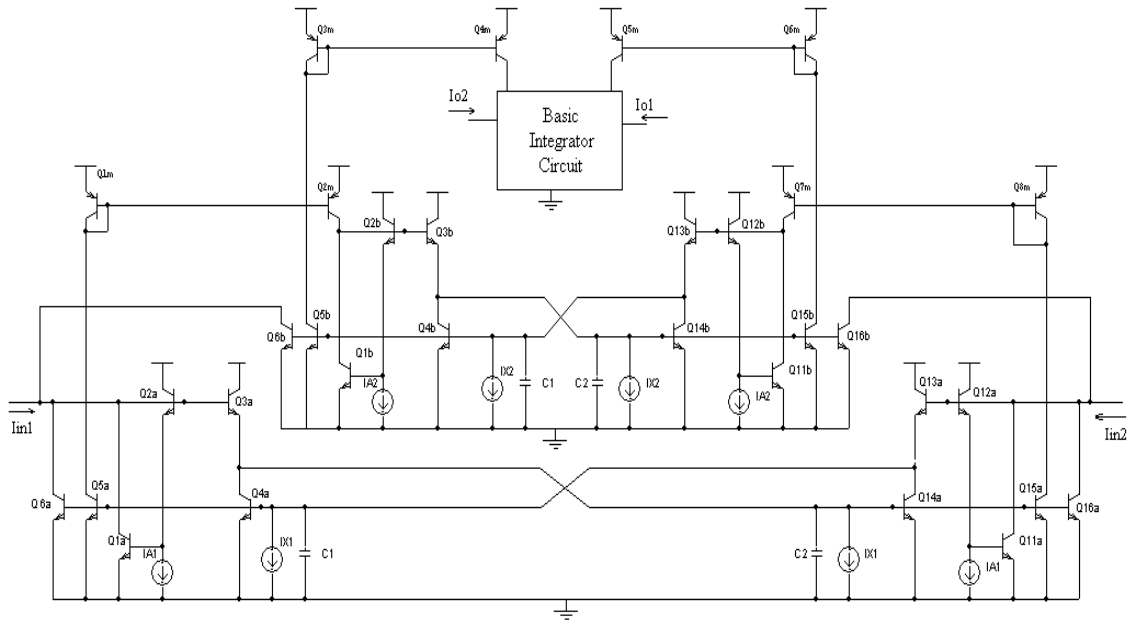


Figure 3. Proposed circuit of realizing three stages of the signal flow graph shown in Figure 1

Table 2. Biasing currents of the integrator stages when cutoff frequency is set to 460 KHz, 4.6 MHz, and 46 MHz

f_c	Tuning current	Integrator 1	Integrator 2	Integrator 3	Integrator 4	Integrator 5
460 KHz	I_A (μA)	4.6764	2.3383	1.4451	0.89313	0.44658
	I_X (μA)	-0.047	-0.021	-0.014	-0.0091	-0.0041
4.6 MHz	I_A (μA)	46.764	23.383	14.451	8.9313	4.4658
	I_X (μA)	-0.47	-0.21	-0.14	-0.091	-0.041
46 MHz	I_A (μA)	467.64	233.83	144.51	89.313	44.658
	I_X (μA)	-4.7	-2.1	-1.4	-0.91	-0.41

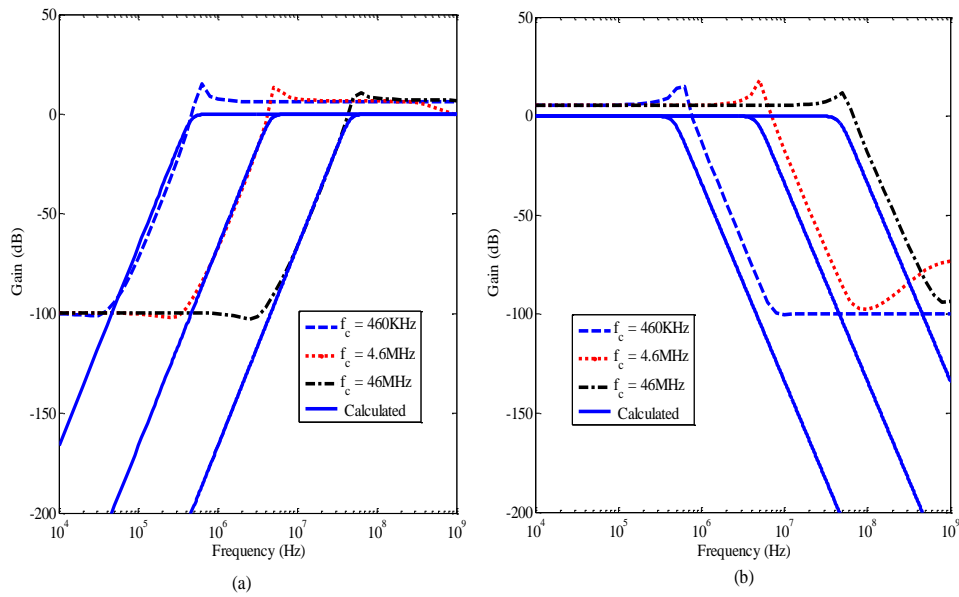


Figure 4. Gain response of the proposed 5th order for different cutoff frequencies, (a) HPF response and (b) LPF response

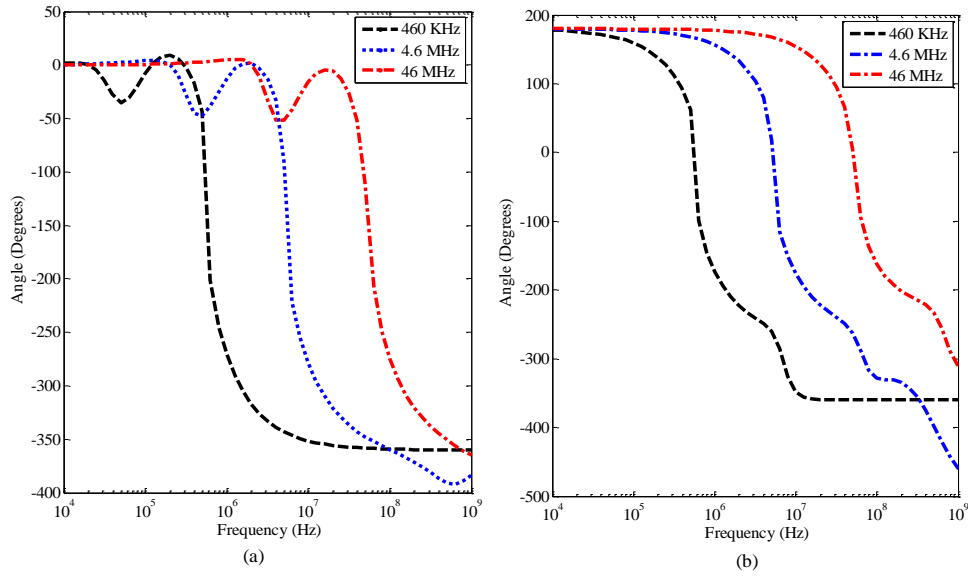


Figure 5. Phase response of the proposed 5th order for different cutoff frequencies, (a) HPF response and (b) LPF response

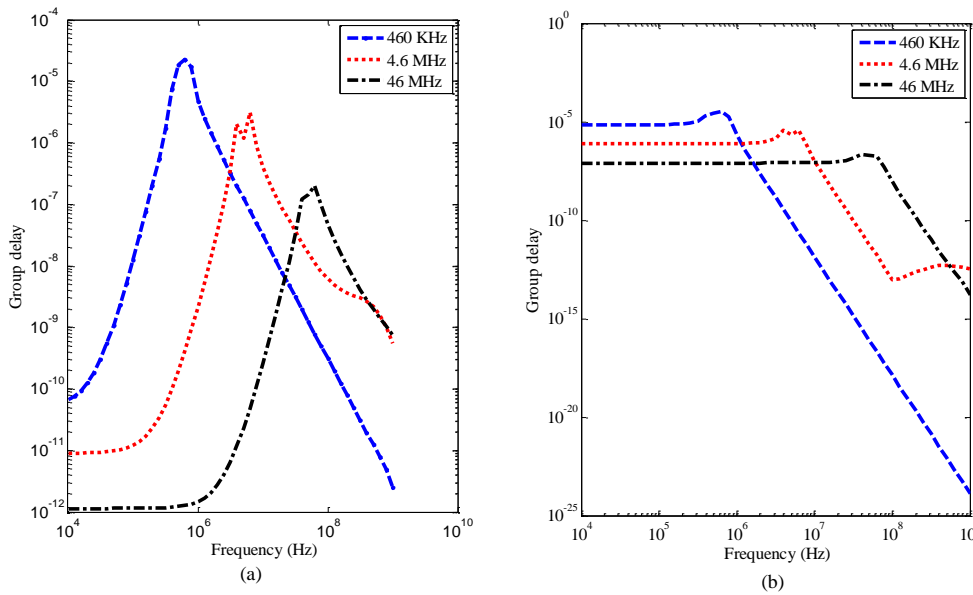


Figure 6. Group delay of the proposed 5th order for different cutoff frequencies, (a) HPF response and (b) LPF response

Simulation results for the non-symmetrical BPFs by taking the outputs from the intermediate nodes, as illustrated in Table 1, are shown in Figure 7. From this figure we can see that all these BPFs are having the same center frequencies, but with different roll-off factors depending on the order of the numerator of their transfer function. To test the simultaneous filtering capabilities of the presented circuit, signal consisting of three different sinusoidal signals with similar amplitudes and different frequencies (100 KHz, 1 MHz, and 10 MHz) is applied to the input of the filter. Figure 8 represents the time response of the HPF and LPF functions. Whereas, Figure 9 represents the frequency spectrum of the input and output signals. From these figures it is clear that simultaneous LPF and HPF functions are being achieved effectively.

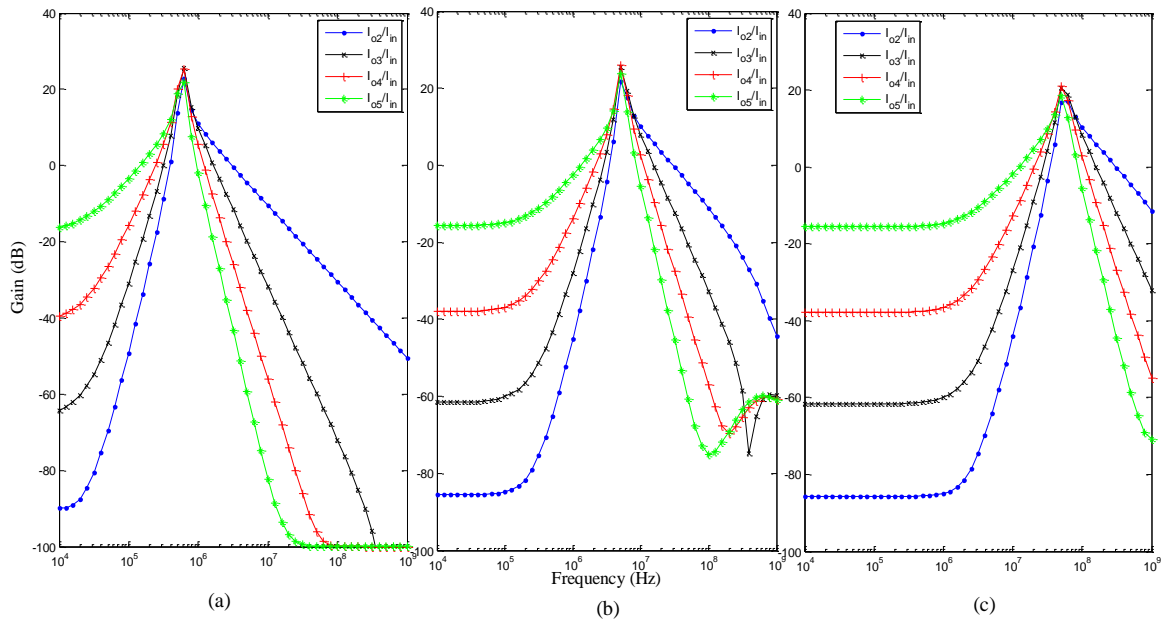


Figure 7. Gain-frequency response of the non-symmetrical BPFs with center frequency set to (a) 460 KHz, (b) 4.6 MHz, and (c) 46 MHz

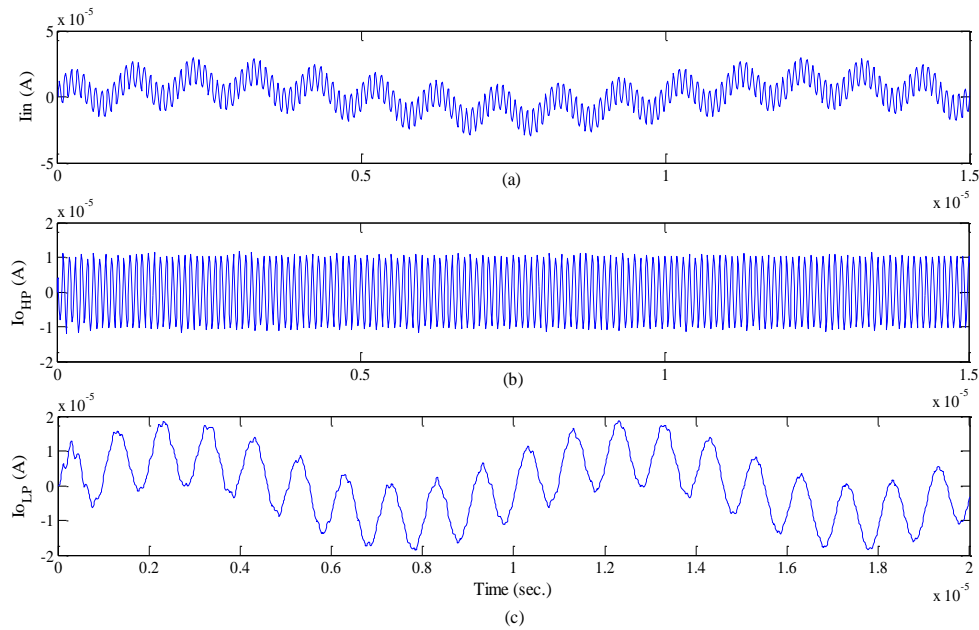


Figure 8. (a) Input signal, (b) output signal of the HPF, and (c) output signal of the LPF

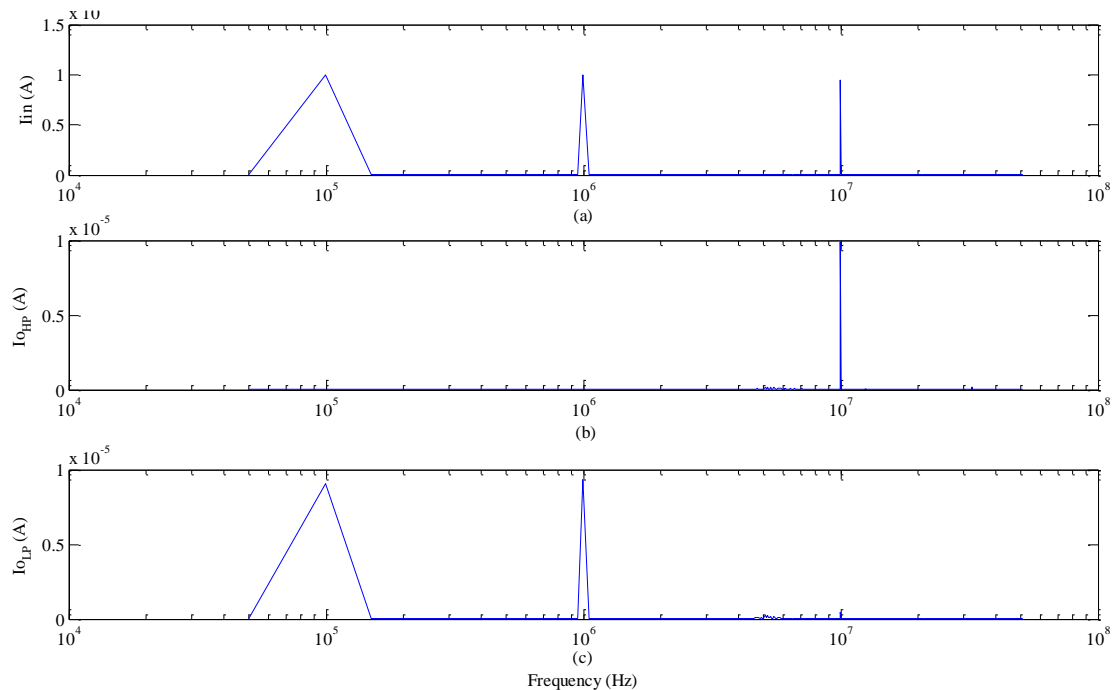


Figure 9. Frequency spectrum of (a) Input signal, (b) output signal of the HPF, and (c) output signal of the LPF

5. CONCLUSION

This paper presents a synthesis method that could be extended to implement high order simultaneous filter functions including HPF, LPF and BPF functions. The method depends on starting with a transfer function representation of the required filter. Utilizing Mason's gain formula, the transfer function is then represented in the form of signal flow graph which, in turn, is directly realized using feed-forward integrators associated with negative feedback loops. The integrators are implemented using fully-differential modified CM translinear loops. These integrators can be configured as either lossy or lossless integrators with all multiplication cofactors tuned independently via current sources. When configured as lossy, the biasing currents are used to cancel the effect of the base currents of the transistors forming the translinear loops. The resulted design uses no resistors with all capacitors being grounded. As an example of the capabilities of the proposed circuit, the realization of 5th order multi-function filters was introduced. The circuit provides simultaneous 5th order LPF, 5th order HPF, and four different non-symmetrical BPF. The cutoff frequency of the proposed filters is limited only to the cutoff frequency of the BJT transistor being used. Pspice simulation results of the presented circuits show good characteristic behaviors in comparison with calculated target. These simulations have been performed using the Pspice parameters of the BFP640 BJT Infineon® transistor.

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