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DC and RF characteristics of 20 nm gate length InAlAs/InGaAs/InP HEMTs for high frequency application

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ABSTRACT

lnAlAs/lnGaAs/InP high electron mobility transistor (HEMT) offers excellent high frequency operation.In this work, the DC and RF performance of a 20 nm gate length enhancement mode InAlAs/InGaAs/InP high electron mobility transistor (HEMT) on InP substrate are presented. The SILVACO-TCAD simulations performed at room temperature using the appropriate model sshowed that the studied device exhibit excellent pinch-off characteristics, with a maximum transconductance of 1100ms/mm, a threshold voltage of 0,62V, and an Ion/Ioff ratio of 2.106. The cut-off frequency and maximum frequency of oscillation are 980 GHz and 1.3THz respectively. These promising results allow us to affirm that this device is intended to be used in high frequency applications.

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1. INTRODUCTION

High electron mobility transistors (HEMTs) technology is usually used for high frequency, high speed and low power applications [1] due to the enhanced electron mobility and velocity at high electron density in the channel. This provides an important drive current I_D, an improved transconductance gm, an important cutoff frequency f_T, and an important output gain, and also provided a low value of noise, low noise and high gain performances. Accordingly, HEMT devices became a significantly competitive candidate for various high-speed circuits [2, 3] millimeter wave systems [4, 5] and even terahertz applications [6-8]. In another hand High electron mobility devices based in the InAlAs/InGaAs material system showed the best high frequency response obtained until now and have exhibited excellent performances in terms of noise parameters compared to MOSFET devices at RF and microwave fields [9]. Also, diverse research groups work hard to increase the maximum frequency fmax of InP and succeeded in bringing up its fmax up to 1 THz. Actually, several technologies are based todayon InGaAs/InAlAs quantum well HEMT devices [10]. InAlAs/InGaAs HEMTs play a leading role in the communication domain ranging from cell phones to electronic warfare systems such as radar and radio astronomy and amplificator application like LNA using an inductive drain feedback technique for wireless application at 5.8GHz and was used in LNA that designed using T-network as a matching technique was used at the input and output terminal, inductive generation to the source and an inductive drain feedback [11, 12]. The particular carrier transport properties of III–V materials are very attractive for THz applications, where outstanding high frequency characteristics have been reported [13-15]. InP-based electron mobility HEMTs are progressively becoming important for the fabrication of millimeter wave-MMICs (monolithic microwave integrated circuits) with high frequency and low noise applications and used for

extraction that was described and tested using the pHEMT measured dataset of I-V characteristics and related multi-bias s-parameters over 20GHz frequency range [16].

The [17-19] this potential is based on the high electron mobility, high electron saturation velocities, and high sheet electron densities provided by these materials. In fact, Compared to silicon compound semiconductors, III–V compound semiconductors have significantly higher electron mobility and can potentially play a major role in future high-speed, low power computing, higher mobility leading to a higher speed at low bias condition. III-V high-electron-mobility transistors (HEMTs) based on InGaAs/InAIAs has emerged as particularly promising for high-frequency applications.

InP-based InAlAs/InGaAs HEMTs on InP substrate showed high operating frequency, low microwave and millimeter-wave noise, as well as high-gain performance. These excellent performances are very attractive for millimeter and also for sub-millimeter wave applications and this are mainly due to the high low-field electron mobility, the high sheet carrier density and the high peak drift velocity. Actually, different works have been achieved in order to enhancethe high-frequency characteristics of InAlAs/InGaAs HEMTs [20-21].

The epitaxial layers of thestudied InGaAs/InAlAs/InP structure consists from the bottom to the top of our structure of:300nm undoped InAlAs buffer layer grown on a 500nm semi-insulating InP substrate layer followed by a 10nm undoped channel layer, a 3nm undoped InAlAs spacer layer a 4-nm undoped InAlAs schottky barrier layera doped InGaAs cap layer. The Silicon doped plane isintroduced between the Schottky barrier and the spacer layers in order to provide electrons carriers for current conduction. The thick barrier layer allowed decreasing leakage current of the gate device, improving current density of the off-state drain-gate breakdown voltage. The effect of low breakdown voltage, due to the tunnelling, can be lowered by the enhancement of the effective gate schottky barrier height. This can be obtained byusing an undoped InAlAs layer (schottky layer) directly beneath the gate [22] or by increasing the aluminum mole fraction in the insulator [23-24] or by moving a portion of the dopants from the top InAlAs layer to the buffer layer [25]. Introduction of schottky layer also enhances the device performance by increasing 2-DEG electron density, improving threshold voltage control [26, 27]. The phenomena dominate the formation of two-dimensional electron gas (2DEG) confined in the quantum well which take the role of the channel in the high electron density transistors (HEMT) based on AlGaN / GaN and InAlAs/InGaAs/InP heterojunction [28]. In this paper, we report the main characteristics of 20nm gate-length InAlAs/InGaAs on InP substrate HEMT.

2. THE HEMT STUDIED DEVICE DESCRIPTION

In this work, the DC and RF performance of 20 nm gate length HEMT on InP substrate have been achieved. A cross-sectional view of the studied InP based HEMT is presented in Figure 1, where parameters and layers details are given. InGaAs contact layer enhance the contact performance below electrodes. The cap layer minimizes the source-drain resistance by forming ohmic contacts with the channel. Schottky layer forms the Schottky contact with the metal gate to guarantee the current flow in one direction and hence, prevent the gate leakage current. Spacer layer physically separates the free carriers from the immobile dopants to minimize the impurity scattering. Figure 2 shows the 3D view of the InAlAs/InGaAs/InP HEMT studied.

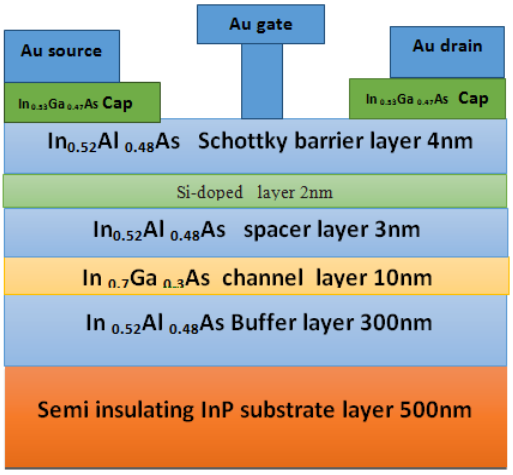

Figure 1. Schematic cross section of the studied InAlAs/InGaAs HEMT on InP substrate

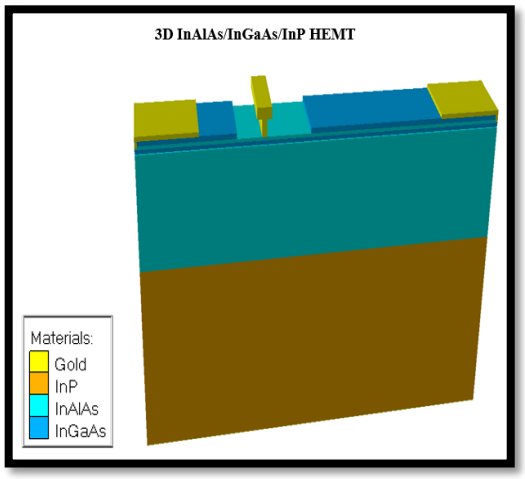

Figure 2. 3D view of the InAlAs/InGaAs/InP HEMT studied

Channel layer is a low band gap material and it is active region in the device. In HEMT devices, the most important point about the channel layer is the 2DEG that results from the band-gap difference between InGaAs and InAlAs. A potential barrier then confines the electrons to a thin sheet of charge known as the 2DEG. This device has considerably less Coulomb scattering compared to MESFET devices, leading to a very high mobility device structure. Athick 300nm undoped InAlAs buffer layer are used to improve carrier confinement in the channel and to create a low leakage isolation floor. It also allows preventing the dislocations from substrate with InP material to the active channel layer.

Creating a high-quality mesh is one of the most critical factors that must be considered since it plays a significant role in the accuracy and stability of the numerical computation that is why a refined meshing has been used in our device channel region as shown in Figure 3. A less refined meshing is used in the other regions, to optimize the time of simulation. Figure 4 shows the doping profile of our device. The cap layer and donor layer are heavily dopedallowing obtaining a good ohmic contact, and providing free electrons to the channel region, which is unintentionally doped.

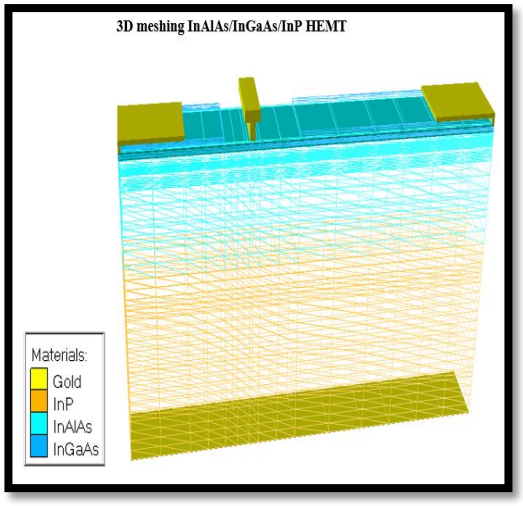

Figure 3. InAlAs/InGaAs/InP HEMT meshing

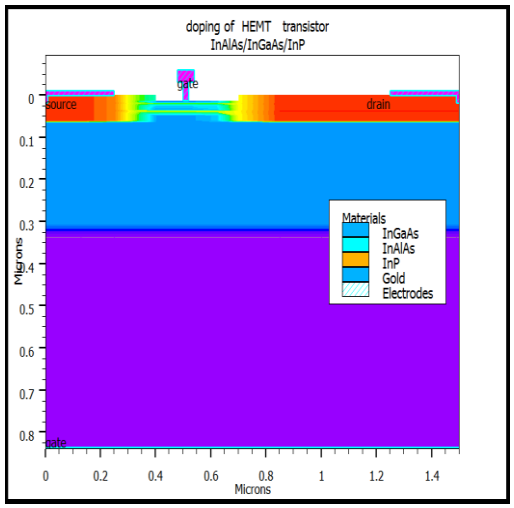

Figure 4. Thedoping of 2D InAlAs/InGaAs/InP HEMT devices

3. RESULTS AND DISCUSSION

To determine the physical phenomenon and the electrical parameter we used the simulation tools is given a great help to determine our characteristics of semiconductors and devices. We used in our simulation blaze module under Atlas and DevEdit for the devices InAlAs/InGaAs /InP HEMT and in our simulation we work with SRH (Shockley-Read-Hall) and fldmob (Parallel Field Dependence: Required to model any type of velocity saturation effect) and lattice temperature models, the method using in our simulation are Newton and gummel.

3.1. DC characteristics

Our device DC properties are simulated at room temperature. Figure 5 shows the simulated transfer characteristic where V_{GS} is in the range from -1V to 0.2V at V_{DS}=1.0V. Figure 6 shows the simulated output characteristics of our studied 20nm gate length InAlAs/InGaAs/InP HEMT where V_{DS} is in the range from 0 to 5V and V_{GS} is in the range from -1.2V to 0V. The threshold voltage (Vth) that is defined by a linear extrapolation of the square root of drain current versus gate voltage to zero current was -0.4V. Our studied HEMT device exhibit good pinch-off characteristics. The drain saturation current obtained at Vgs=0 volt and V_{ds} = 2 Volts is 620mA. A good Ion/Ioff ratio of 510^4 was demonstrated.the same Vgs. Consequently, there is a $0.5.10^4$ fold increase in the I_{ON}/I_{OFF} ratio or figure of merit in the studied HEMT. The subthreshold slope is plotted in Figure 7. We can observe that our studied device provides a subthreshold voltage "SS" slope of 52mv/dec. Figure 8 shows the transconductance (gm) as a function of gate voltage. The maximum transconductance gm obtained is 1100 mS/mm at V_{gs} =-0.3 V and V_{ds} = 1.0 V. Our result is hopeful knowing that an important slope of gm means that we have a good control of the gate on the device channel

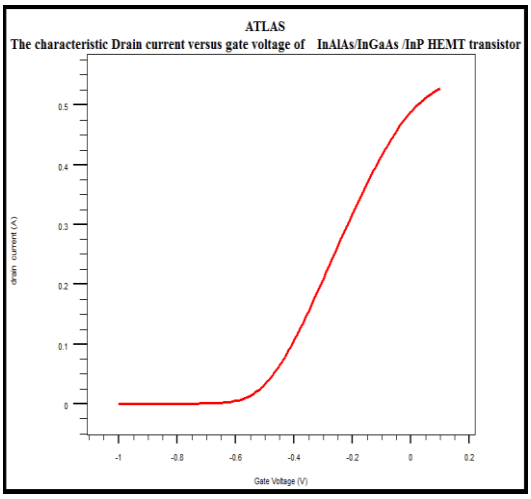

Figure 5. Drain current as a function of gate to source voltage V_{GS} for the 20nm gate length InAlAs/InGaAs/InP HEMT studied

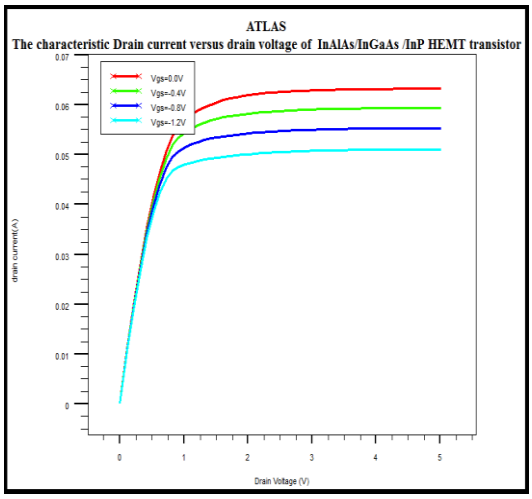

Figure 6. Drain current as a function of source to drain voltage VDS for the 20nm gate length InAlAs/InGaAs/InP HEMT studied

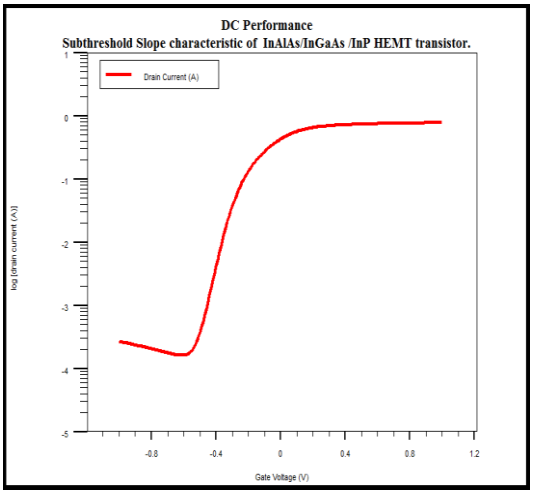

Figure 7. Subthreshold slope characteristicof our 20nm gate lengthInAlAs/InGaAs/InP HEMT on InP

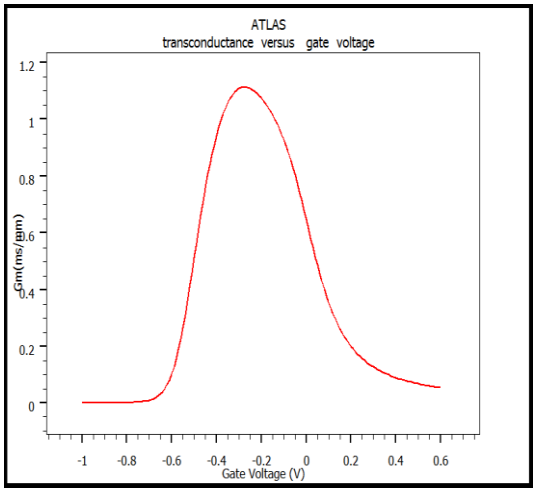

Figure 8. Transconductance gmas a function of source to gate voltage VGS for the 20nm gate length InAlAs/InGaAs/InP HEMT studied

The following study will help to highlight the dependence of the transconductance on V_{DS} and V_{GS}. The extrinsic transconductance gm as a function of source to gate voltage V_{GS} for the 20nm gate length InAlAs/InGaAs /InP HEMT studied with different drain voltage Vds=1.0V,1.5V,2.0V,2.5V and 3.0V respectively is given in Figure 9. A maximum peaktransconductance equal to 1960mS/mm is obtained for Vds = 3.0 V at room temperature. This peak appearsin the curve of the transconductance as a dependence on the gate bias Vgs. This reflects the DC behavior of the simulated HEMT, which corresponds to the 2DEG channels modulated by differentgate voltages. Drain induced barrier lowering DIBL is caused by gate shrinking and reduction in the transistor threshold voltage at higher drain voltages. In Figure 10, we presentthe Drain-induced barrier lowering (DIBL) of 2D InAlAs/InGaAs/InP HEMT transistor, a lower DIBL value of 120mV/V is obtained

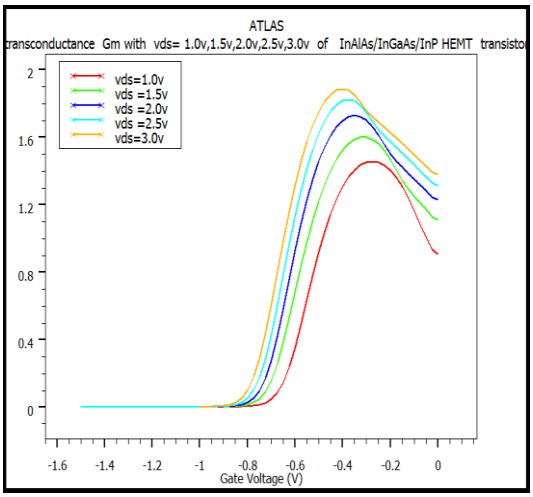

Figure 9. Transconductance gmas a function of source to gate voltage V_{GS} for the 20nm gate length InAlAs/InGaAs/InP HEMT studied with different drain voltage

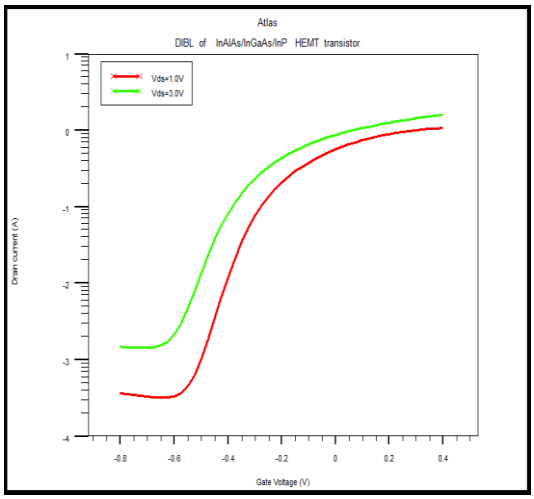

Figure 10. Drain-induced barrier lowering (DIBL) of the InAlAs/InGaAs/InP HEMT studied

3.2. RFcharacteristics

HEMTs are usually characterized in dynamics by two important parameters that are the cut-off frequency F_T and the maximum oscillation frequency Fmax. MTG, GMS, GMA and h_{21} are also very important parameters that can be taken into account in RF study. Figure 11 shows the simulated current gain (h_{21}), the maximum transducer power gain (MTG), maximum stable gain (GMS), available maximum power gain (GMA) and unilateral power gain as a function of frequency, of the 20nm gate length devicefor V_{ds}=5 V and Vgs= 0.0 V. Our results have been obtained over 1 kHz–1 THz frequencyrange. These results allow observing that a maximum gain shown for the current is 60dB, the maximum transducer power gain is 31 dB and the maximum stable power gain is 30 dB at 1 GHz. The electronic transfer in the channel is optimized due to the effect of C_{GS}capacitance. This high value capacitance results from the extended effective gate length [29], the drops suddenly at low frequency in Unilateral power gains because capacity C_{GS} can be ignored in this frequency band. The obtained cutoff frequency and maximum frequency fmax for the HEMTdevice studied were 980 GHZ and 1.3THz, respectively.

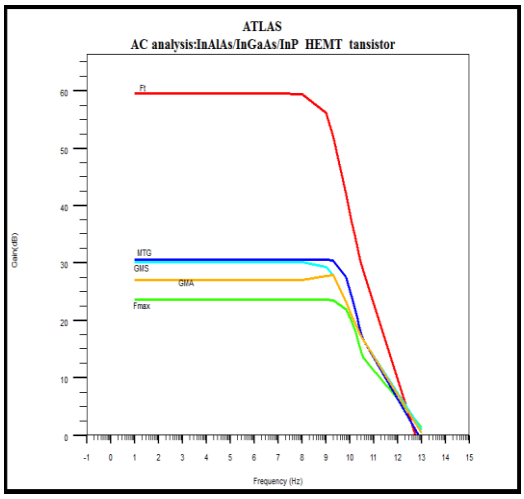

Figure 11. Current gain, h21, and unilateral power gain as a function of frequency for our InAlAs/InGaAs/InP HEMT

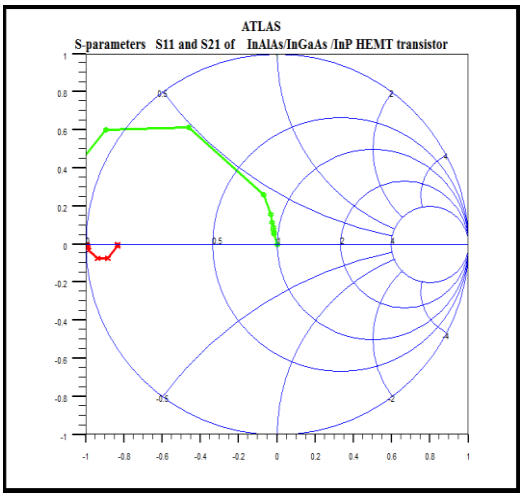

Figure 12. S-parameters S11 and S21 of 2D InAlAs/InGaAs/InP HEMT transistor

The RF characterization was performed on our device from 50MHz to 50 GHz under a bias voltages of Vds=5V and Vgs=-0.45V. The reflection coefficient (S11, S22) are shown in Figure 12. RF gain has a maximum value of S_{21}=-0.9 at f=5THz, reflection coefficients (S11, S22) are less than 20dB at all frequencies of the simulation range.

4. CONCLUSION

In this work, DC and RF performances of HEMT transistor with InAlAs/InGaAs and InP substrate with 20 nm gate length were simulated using Atlas-SILVACO based on drift-diffusion carrier transport model. The results obtained show optimistic gm, DIBL, Ion/Ioff, fTand a cutoff frequency of 980GHZ with a high value of maximum frequency of 1.3THZ that it's important in high frequency application. We can conclude that we can continue scaling with a reduced gate length and dimensions of this device, consuming less power energy. Our DC and RF results has been study and simulated, allow this device is expected to be a promising candidate that we can used in high speed, hight frequency and microwave applications.

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