International Journal of Electrical and Computer Engineering (IJECE)
Vol.9, No.6, December 2019, pp. 4826~4835
ISSN: 2088-8708, DOI: 10.11591/ijece.v9i6.pp4826-4835

Modeling and simulation of graphene field effect transistor (GFET)

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Article Info

Article history:

Received Feb1, 2019
Revised Jun 26, 2019
Accepted Jul5, 2019

Keywords:

Fabrication
GFET
MOSFET

ABSTRACT

Graphene based top-gated Field effect transistor (GFET) is designed and simulated using the device simulator packages. The paper describes fabrication process and the device simulation aspects of the GFET device. Two devices with different gate lengths of 200nm and 350nm are simulated. Device simulations are carried out in open source TCAD software package. The results indicate a depletion FET type operation in which ON/OFF current ratio of 2.25 is obtained.

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1. INTRODUCTION

Graphene is a planar two-dimensional layered crystalline allotrope of Carbon consisting of sp2-hybridized carbon atoms connected in the form of extended benzene rings. Graphene is known to exhibit outstanding electronic properties [1] with exceptionally high electron mobility. Graphene also exhibits exceptional mechanical [2] and optical properties [3]. The another advantage of Graphene is that it requires only planar processing similar to once available/ existing in the CMOS industry.

Pure graphene has a planar honeycomb structure with zero bandgap. The band structure for graphene consists of the conduction and valence bands forming conic shapes and intersecting at Dirac points. The electrons in the Dirac points behave as zero mass particles and can tunnel through potential barriers. As such the electrons in graphene do not display localization effects and hence are able to move long distances without undergoing scattering resulting in high values of mobility [4].

Graphene is fabricated by several methods [5] like the mechanical exfoliation, epitaxy, chemical vapor deposition (CVD) and chemical derivation. Other methods for large scale graphene synthesis are chemical systemization [6,7], ion implantation [6], unzipping carbon nanotubes to form graphene sheets [6] and crystal sonification [7].Graphene FET was invented due to the discovery of the ambipolar characteristics [8, 9]. The doping is induced due to the electric field which causes a change in the Fermi energy. Graphene does not normally need any doping due to its self-doping characteristics.Three topologies of graphene FETs are normally used (a) top gate [10, 11] (b) dual gate [12] and (c) back gate [12]. Figure 1 shows a top gate GFET device. The top gate device can be fabricated by growing epitaxial graphene on SiO2 layers. On top of the graphene layer a dielectric layer is deposited followed by gate contacts.

Graphene FET structure is shown in detail in the Figure 2. The absence of Graphene as a standard library material in the device simulator packages forces the authors to employ an indirect method of redefining the material properties of an existing semiconducting material from the standard device simulator. In the present wok, the authors use polysilicon as the semiconducting material. The properties of the polysilicon material are redefined to simulate the Graphene material.

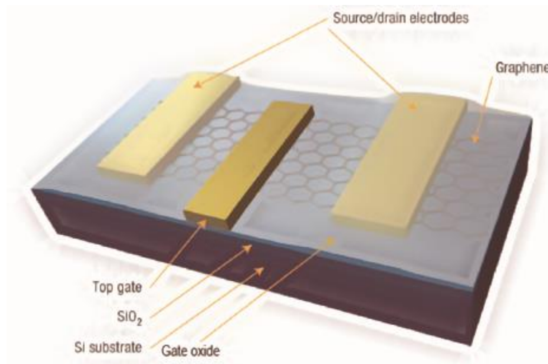

Figure 1. GFET model

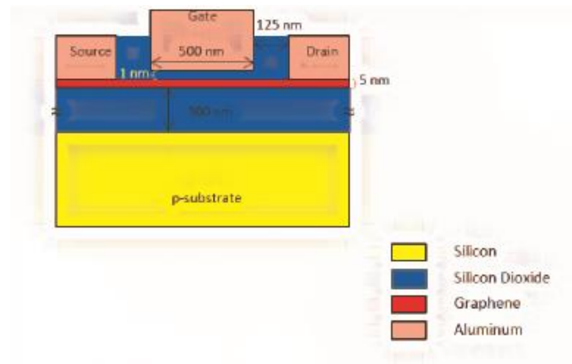

Figure 1. Fabricated GFET structure

The fabrication of GFET starts with a p type <100> silicon wafer substrate with a doping concentration of $N_A=10^{15}cm^{-3}$. The silicon substrate then undergoes a thermal oxidation process to deposit SiO_2 of 300nm. The active layer that will be used for the device operation and carrier transport is deposited. This layer is made up of Graphene. In simulation, however due to the non-availability of graphene as a standard library material, polysilicon is used for this layer. Doped polysilicon layer of 5nm thick is deposited, the doping concentration being n type $NA=10^{17}cm^{-3}$. A thin layer of SiO_2 is then deposited to provide the gate oxide. The oxide layer is patterned to make windows for gate, drain and source electrode. Aluminum is then deposited and patterned to obtain the three electrodes.

2. SIMULATION AND RESULT

The device structure simulated as per the process details described in Table 1 and Table 2 is shown in Figure 2. The active channel region and source drain junctions are highlighted in Figure 3. Meshing is an important step in the device simulation. The mesh density controls the number of simulation nodes and hence the fidelity of solution. At the same time number of simulation nodes directly impacts the simulation time and computational load. Fine meshing is used in the areas near the junctions while coarse meshing is used in other regions. This helps to reduce the computational load but still maintaining the required details at critical areas. The meshed structure is shown in Figure 4.

The non-availability of graphene as a standard library material in device simulation packages calls for some modification in the material properties to be forced in the device simulation package. Polysilicon layer of 5nm deposited to form the active layer, is later redefined as Graphene by altering the material properties as given in Table 3. The command used for redefining the graphene material is as follows:

#material graphene definition

Material material=polysilicon eg300=0 mun=10000 mup=10000 permittivity=25

Table 1. GFET fabrication process steps

Step	Description
0	Starting material initial p-type substrate, <100> orientation
1	Deposit thin oxide layer
2	Deposit polysilicon layer
3	Deposit gate oxide layer
4	Pattern gate oxide for contact windows.
5	Deposit metal electrodes for source drain and gate region

Table 2. Process parameters

Step	Process parameters
Substrate	Boron doped 1x10^{15}cm^{-3}<100> orientation
1	Deposit Partial SiO_2using dry oxidation, time = 530s, temp = 1000degC
2	Deposit polysilicon layer 5nm thick arsenic doped 1x10^{20}cm^{-3}
3	Deposit Gate oxide 5nm thickdry oxidation time = 30s, temp = 800degC
4	Pattern Gate oxide to open windows for electrode deposition
5	Deposit Aluminum
6	Pattern Aluminum and deposit oxide 0.1um thick

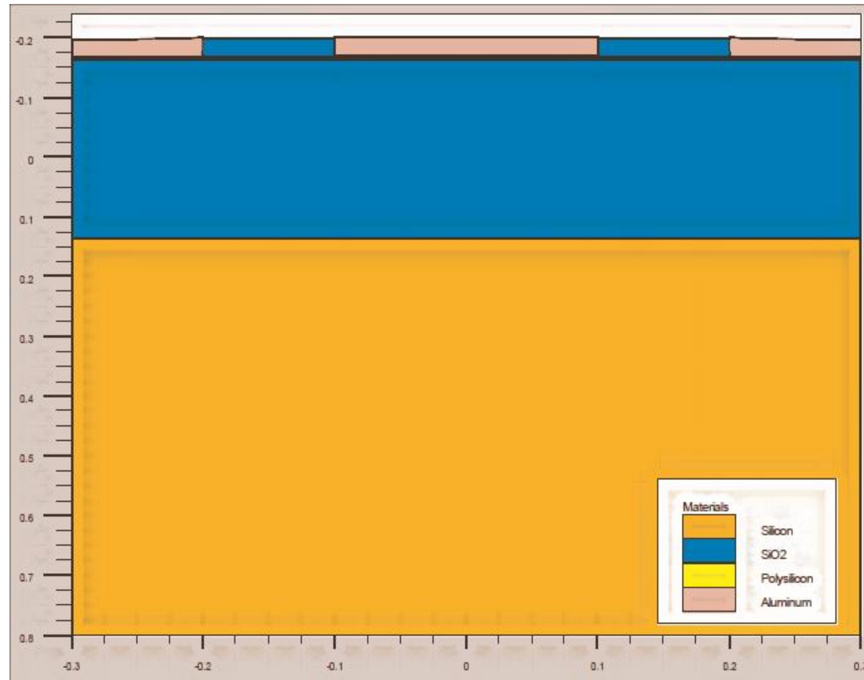

Figure 3. GFET device structure from process simulation

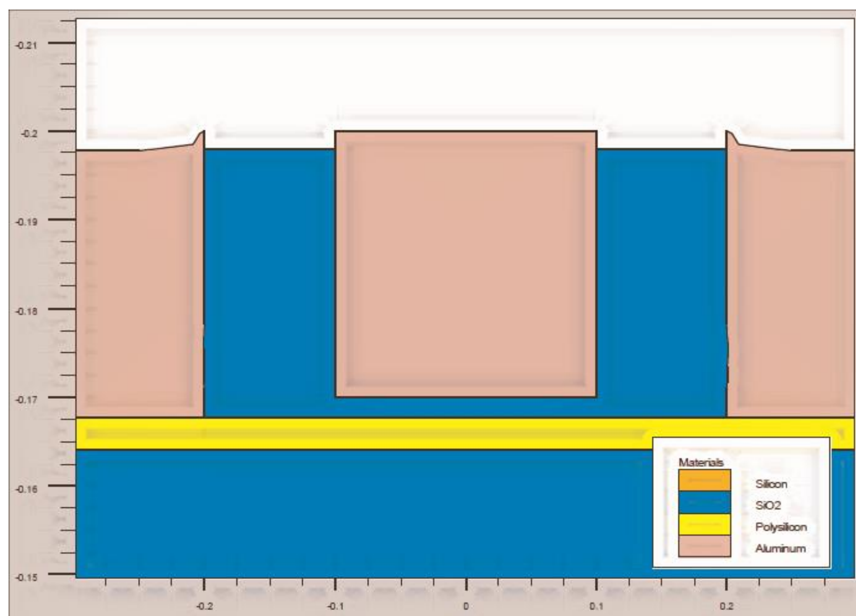

Figure 4. GFET device structure (channel region)

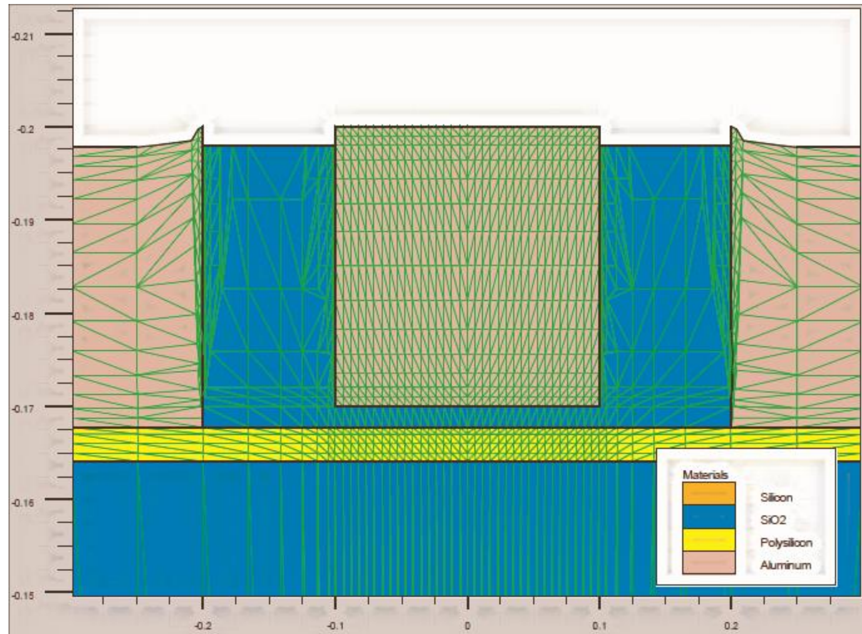

Figure 5. GFET device meshed model

Table 3. Graphene material properties

Process	Model
Eg at 300K	0
Mobility (n carrier)	10000 cm^2/ V-s
Mobility (p carrier)	10000 cm^2/ V-s
Permittivity	25

The device simulation was carried out for different channel lengths. The simulation results are presented in the following paragraphs. The first simulation carried out for the device structure is to obtain the input characteristics. The Id-Vgs curve for the devices are shown in Figure 6 and Figure 7 for a channel length of 200nm and 350nm.

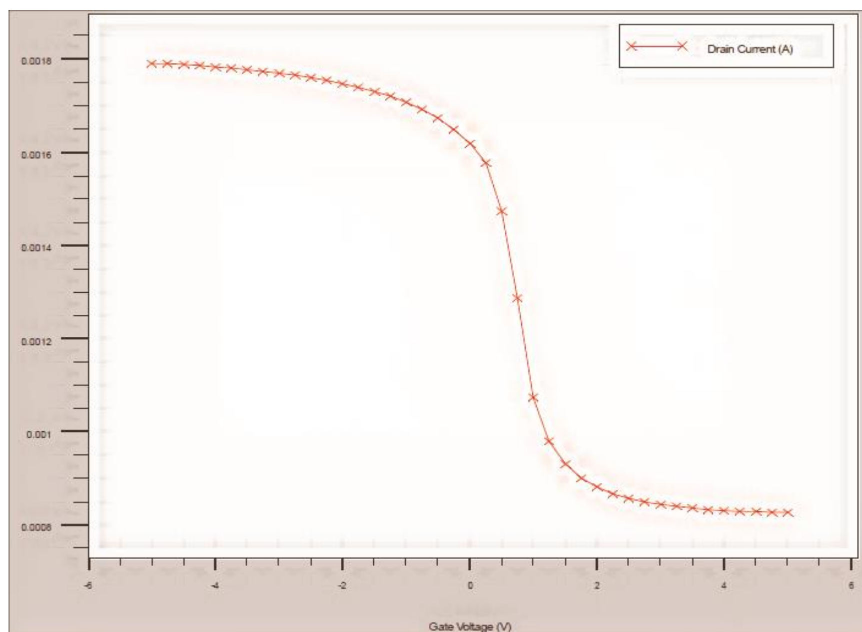

Figure 6. I_d-V_{gs} plot at Vd=1V (L: 200nm)

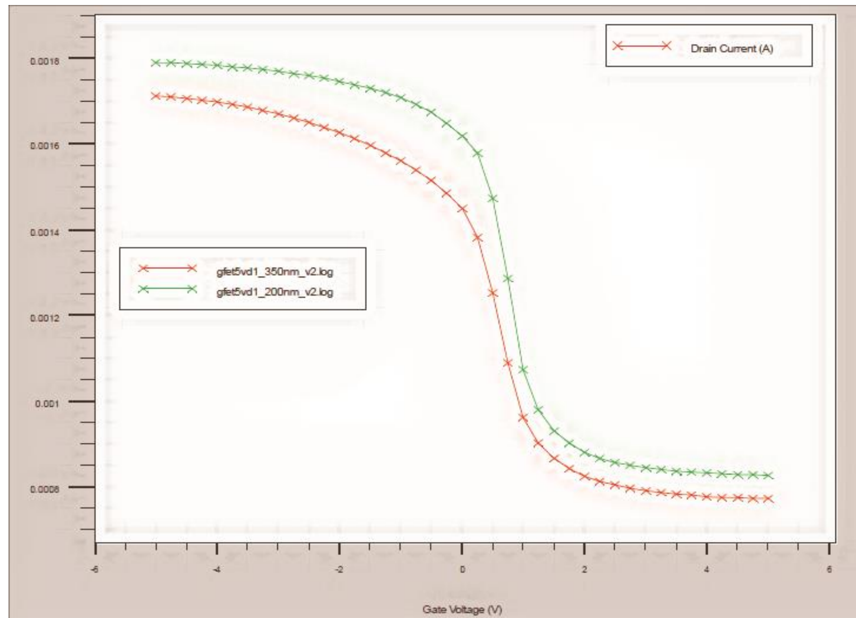

Figure 7. I_d-V_{gs} curve at Vd=1V for L=200nm (Green) and 350nm (Red)

The I_d-V_{gs} plots for the two devices show a depletion MOSFET like performance. This is expected with the source of electrons, the graphene channel being already present underneath the gate. The ON/OFF current ratio is nearly 2.25 for both devices however, the drain current is slightly more for L=200nm device as shown in Figure 7. The threshold voltage for both devices is around 2V as can be deduced from the plots. The I_d-V_{ds} characteristics of the device are shown in Figure 8. The characteristics are obtained for different values of Gate voltages from V_{gs}=0 to -10V. The drain current shows saturation characteristics beyond V_{ds}=2V. Similar characteristics for device with 350nm gate length is shown in Figure 9.

Current densities in the graphene layer are simulated as shown in Figure 10 for 200nm and Figure 11 for 350nm device at V_{ds}=1V and V_{gs}=5V. The same plots for V_{gs}=-5V is shown in and Figure 12 and Figure 13. The plots demonstrate a weaker current flow at V_{gs}=5V as against V_{gs}=-5V as is also depicted from the I_d-V_{gs} plots.

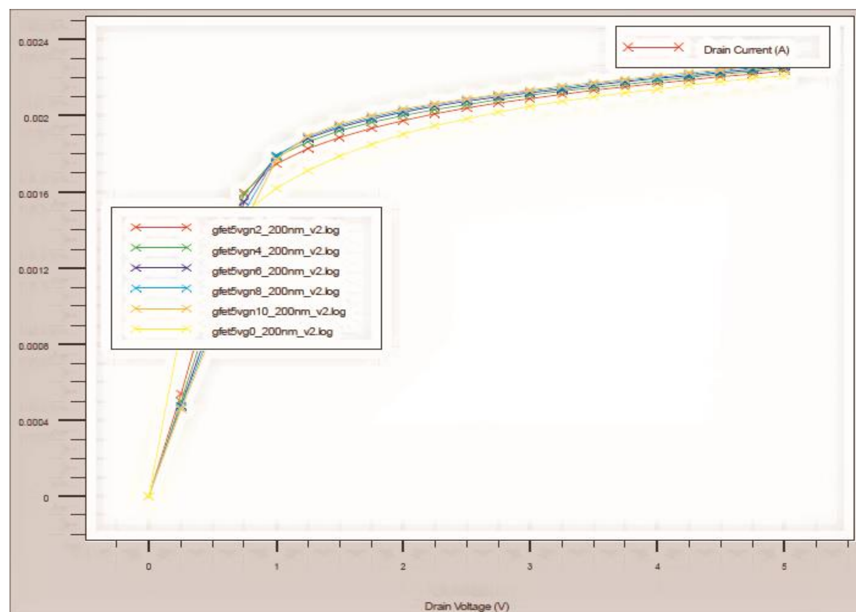

Figure 8. Parametric Id-Vd curve for different V_{gs} (L=200nm)

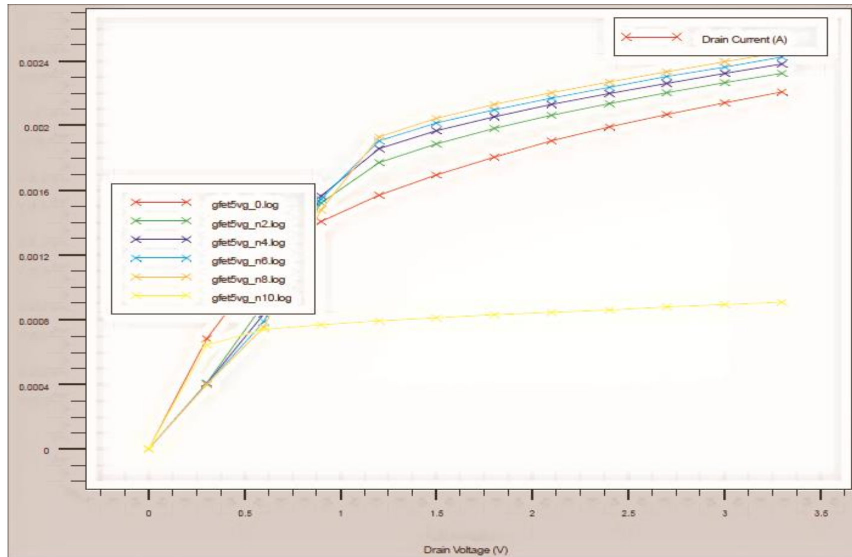

Figure 9. Parametric Id-Vd curve for different V_{gs} (L=350nm)

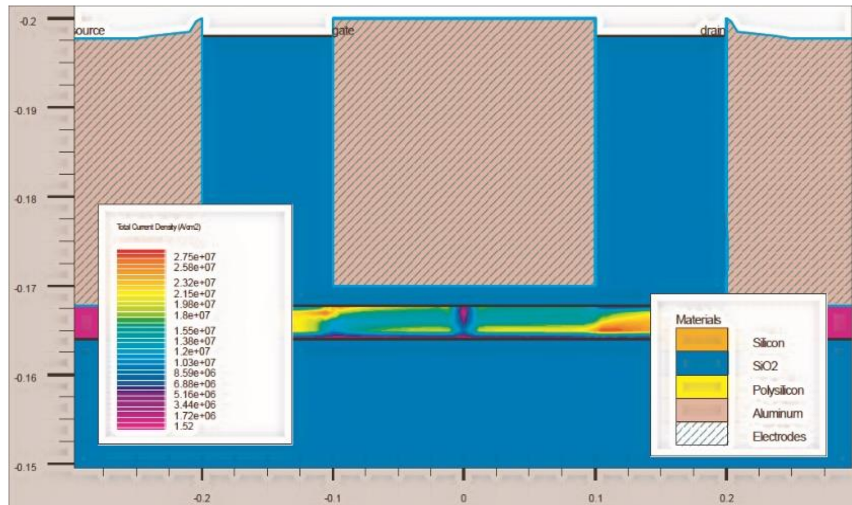

Figure 10. Current density in graphene layer (L: 200nm, Vd: 1V, Vg: 5V)

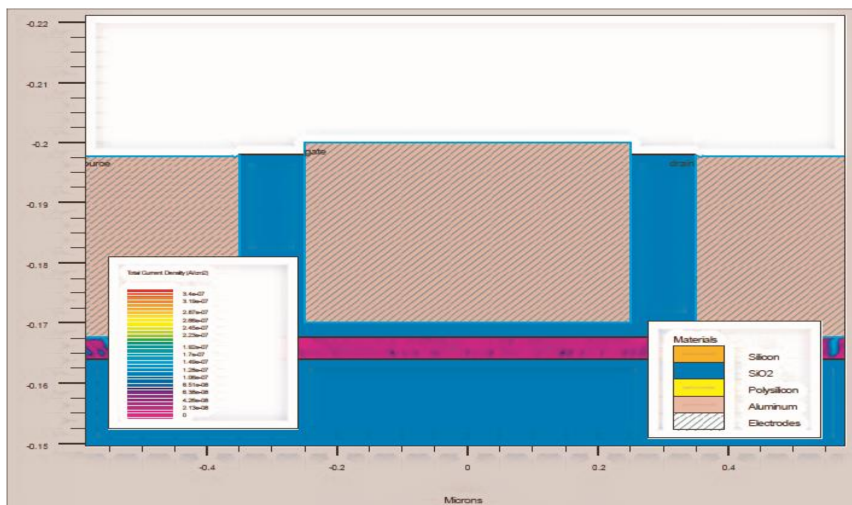

Figure 11. Current density in graphene layer (L: 350nm, Vd: 1V, Vg: 5V)

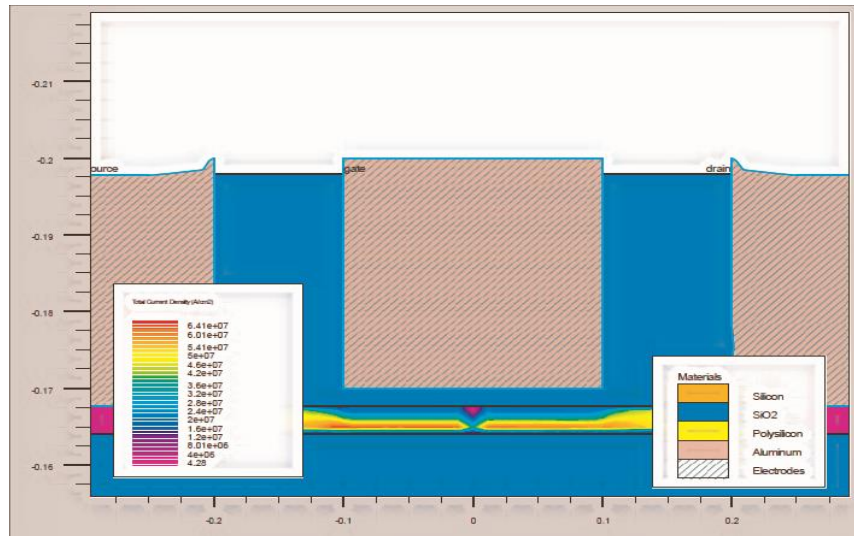

Figure 12. Current density in graphene layer (L: 200nm, Vd: 1V, Vg: -5V)

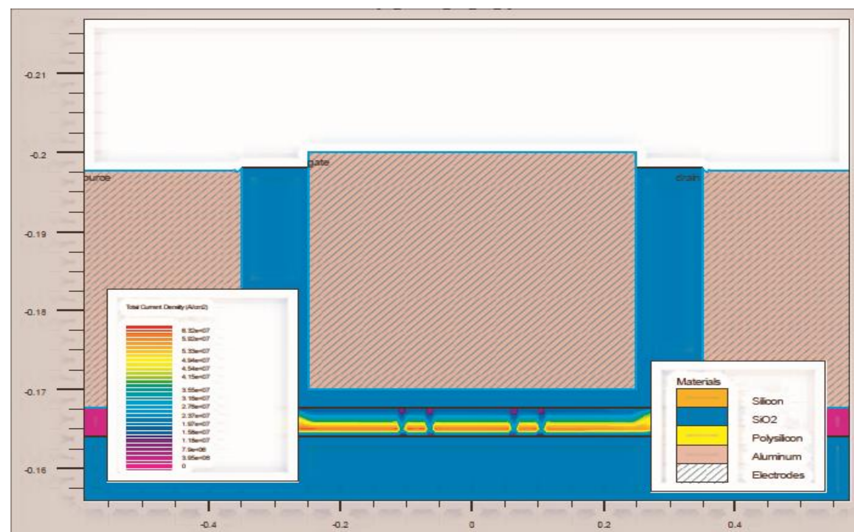

Figure 13. Current density in graphene layer (L: 350nm, Vd: 1V, Vg: -5V)

Figure 14 and Figure 15 shows the Electric Field distribution in the graphene channel for 200nm and 350nm channel length device. The drain source terminals were open and Gate Voltage was -5V. The electric field is concentrated in the channel region below the gate. Figure 16 and Figure 17 depict the electron concentration in the two devices at the mentioned bias voltages. These figures depict a continuous carrier concentration below the channel region from drain to source and hence the drain current.

Figure 18 and Figure 19 shows the low frequency Gate-Source capacitance plot for different gate voltages for two devices of different channel length. The capacitance measurements were done at 1 kHz frequency. The capacitance curve is similar to those obtained for a MOSFET, hence demonstrating gate control on the device operation.

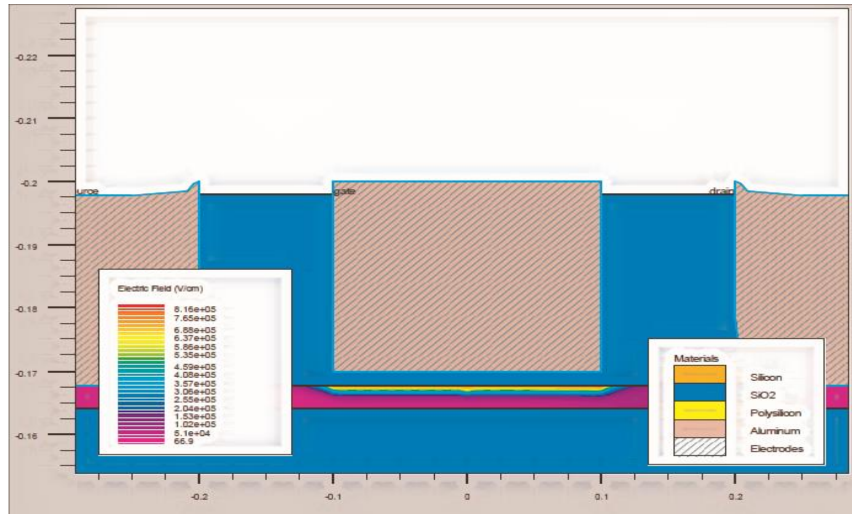

Figure 14. Electric field in graphene layer, (L: 200nm, Vd: open, Vg: -5V)

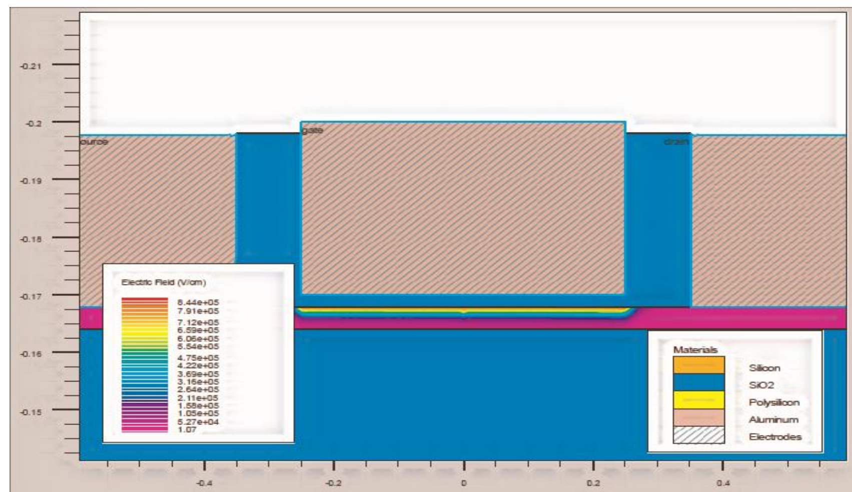

Figure 15. Electric field in graphene layer, Emax = 8.44e+05 V/cm (L: 350nm, Vd: open, Vg: -5V)

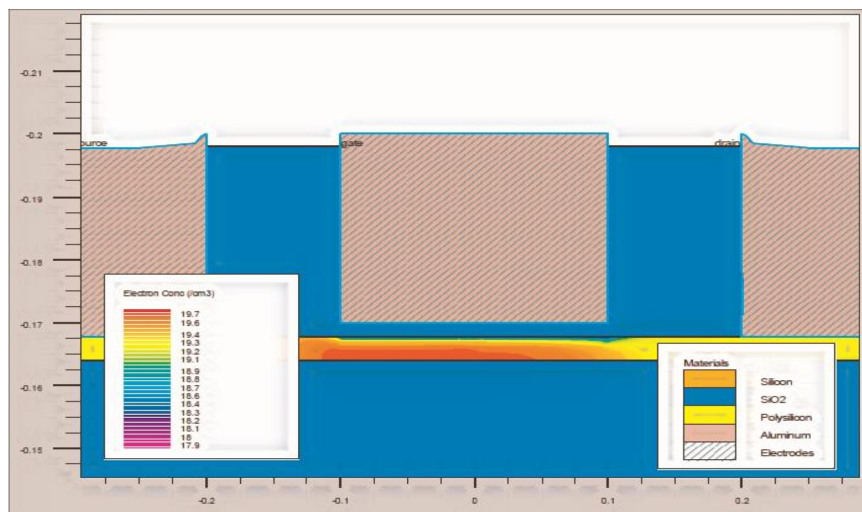

Figure 16. Electron Concentration in graphene channel (L: 200nm, Vd: 1V, Vg: -5V)

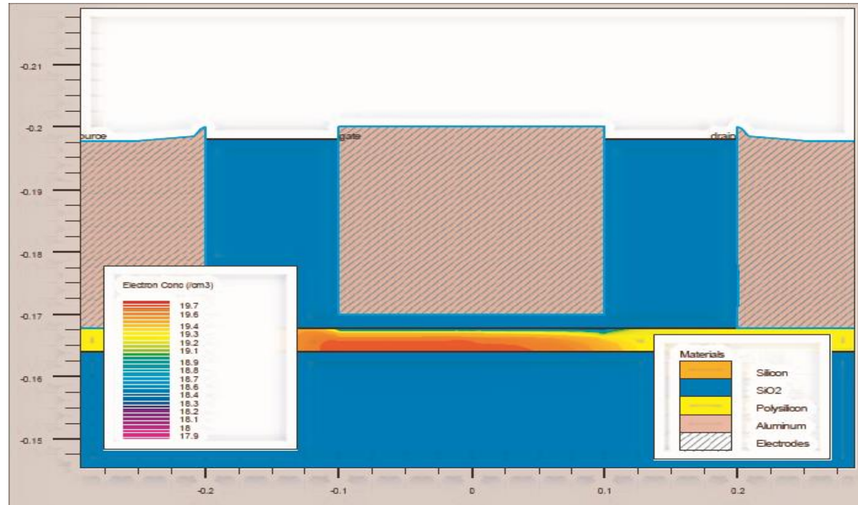

Figure 17. Electron Concentration in graphene channel (L: 200nm, Vd: 1V, Vg: -5V)

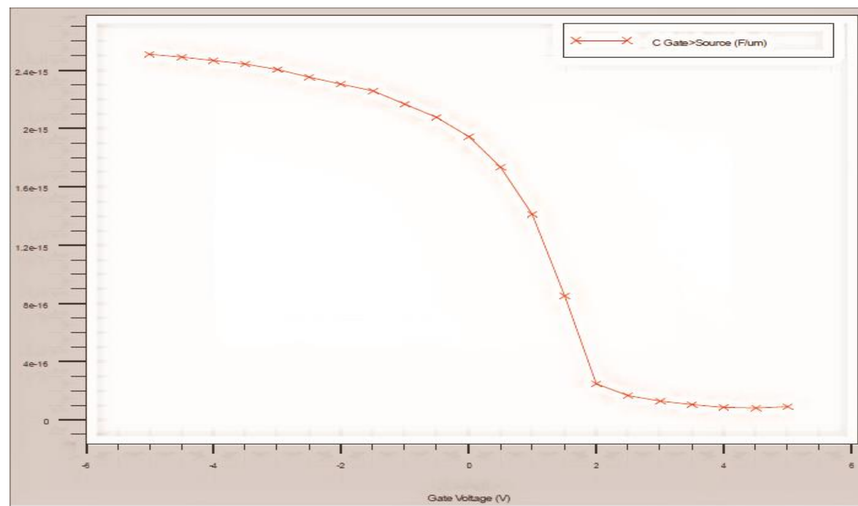

Figure 18. Low frequency C_{gs} plot (L: 200nm, Vd: 5V)

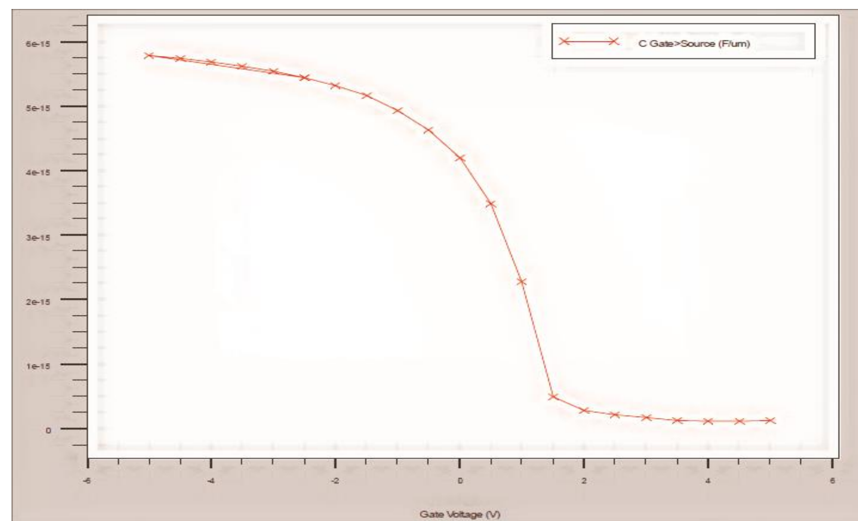

Figure 19. Low frequency C_{gs} plot (L: 350nm, Vd: 5V)

3. CONCLUSION

The present work deals with the design and simulation of GFET devices using device simulator software ATHENA and ATLAS. Two GFET devices were modeled and simulated with different gate lengths. The simulated devices showed MOSFET like operation characteristics with threshold voltages, drain current saturation etc. The current ON/OFF ratios for the GFET was obtained to be around 2.25. The electric field and the carrier concentration curve demonstrate the channel formation below the gate and hence the current flow. The basic GFET device characteristics are simulated in the present work and the simulated device show a good promise for circuit implementation.

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