Dynamic model of a DC-DC quasi-Z-source converter (q-ZSC)

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Article Info	ABSTRACT
	Two quasi-Z-source DC-DC converters (q-ZSCs) with buck-boost converter gain were recently proposed. The converters have advantages of continuous gain curve, higher gain magnitude and buck-boost operation at efficient duty ratio range when compared with existing q-ZSCs. Accurate dynamic models of these converters are needed for global and detailed overview by understanding their operation limits and effects of components sizes. A dynamic model of one of these converters is proposed here by first deriving the gain equation, state equations and state space model. A generalized small signal model was also derived before localizing it to this topology. The transfer functions (TF) were all derived, the poles and zeros analyzed with the boundaries for stable operations presented and discussed. Some of the findings include existence of right-hand plane (RHP) zero in the duty ratio to output capacitor voltage TF. This is common to the Z-source and quasi-Z-source topologies and implies control limitations. Parasitic resistances of the capacitors and inductors affect the nature and positions of the poles and zeros. It was also found and verified that rather than symmetric components, use of carefully selected smaller asymmetric components L1 and C1 produces less parasitic voltage drop, higher output voltage and current under the same conditions, thus better efficiency and performance at reduced cost, size and weight.

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1. INTRODUCTION

Impedance source converters (ZSC/ISC) couple converter's main circuit to its power source [1]. They provide additional features not obtained in prior current fed or voltage fed converters such as dead or overlap time in addition to their advantages [2].

Applicability of Z-source concept to ac-ac [3]–[5], ac-dc [6], dc-ac [7]–[12] and dc-dc [13], [14], [23], [15]–[22] power conversion generated a lot of interest and research resulting in the development of variant and new topologies [24]. First application of ZSC was the ZSI for fuel cell application [1] then drives [4].

Reference [25] proposed a modified impedance source converter (ZSC) called quasi-ZSC (q-ZSC) shown in Figure 1 by swapping the positions of switches and inductors to solve problems like discontinuous input current, high capacitor voltage requirement for the voltage fed ZSCs and high inductor current requirement for current fed ZSCs. Most of early ZSC and q-ZSCs [4], [26], [35]–[40], [27]–[34] focused on inverter applications except [5] on ac-ac converter and [6] on rectifiers. Reference [13] extended ZSC and q-ZSC concept to DC-DC applications by proposing four non-isolated DC-DC ZSC and q-ZSC topologies each, then [20], [22] proposed isolated DC-DC ZSCs after which several other isolated and non-isolated DC-DC converter topologies have been proposed.

The major difference between impedance source dc-ac (inverters) and DC-DC converters lies on how the output is taken. For inverters, it is taken across a switch while for the DC-DC converter, they are mostly taken across a capacitor [13] as shown in Figure 1 (b) and (c), although [15], [16], [18], [19], [21]–[23] took the output across a switch albeit with additional components in what is called PWM DC-DC impedance source converters. Reference [15] analysed the steady-state performance of such converters in continuous conduction mode (CCM).

References [29], [41]–[45] applied state space averaging [46] and Taylor's series expansion and derived the small signal analysis to investigate the dynamic characteristics of different ISI topologies. Accurate small signal model is needed to obtain a global and detailed overview of system dynamics by understanding system limits and components sizes [44]. It is based on the assumption of perturbations around steady-state operating point [47]. Small signal perturbations ($\mathbf{e.g.}$ $\tilde{\mathbf{d}}(\mathbf{t}), \tilde{\mathbf{v}}_{\mathbf{g}}(\mathbf{t}), \tilde{\mathbf{\imath}}_{\mathbf{g}}(\mathbf{t})$) are applied to the steady state duty ratio (D) and input variables (e.g. Vg and Ig) to obtain the small signal model. These perturbations causes the dynamic state variables ($\mathbf{e.g.}$ $\mathbf{v_{C1}, v_{C2}, i_{L1}}$ and $\mathbf{i_{L2}}$) to vary (by $\tilde{\mathbf{v}}_{\mathbf{C1}}, \tilde{\mathbf{v}}_{\mathbf{C2}}, \tilde{\mathbf{\imath}}_{\mathbf{L1}}$ and $\tilde{\mathbf{\imath}}_{\mathbf{L2}}$ respectively).

Use of small signal models to obtain dynamic models for controller design makes them very important. They are also used to obtain the transfer functions between state variable and system input by assuming other system inputs to be zero [41], [44], [48].

Interestingly, the existing publications on dynamic models of ISCs [41], [44], [45], [48]–[51] focused on inverters. This is mainly due to the fact highlighted by [15] that majority of the literature on ISCs focuses on the inverter mode of operation although [52] worked on PWM DC-DC converter. DC-DC ZSC/q-ZSCs are not very popular due to common deficiencies like lack of buck-boost capability at the efficient duty ratio range of [0.35 to 0.65] [53], discontinuous gain curve and higher components count as compared with the traditional buck-boost converter (BBC).

However, more findings are making ISCs overcome these challenges such as [54], [55] where the gain and continuous gain curve of BBC were achieved using non-isolated q-ZSC topologies. These topologies produced higher magnitude output voltages and currents than the corresponding buck-boost converters thus giving them potential advantages.

In this paper, the concept of dynamic modelling is extended to the DC-DC q-ZSC. This Extension is important because their applicability is increasing while there are no or very few existing dynamic models of them.

The modelling began by first considering an ideal circuit to derive the ideal gain equation. Next, non-symmetric, real components were considered rather than the simple symmetric or ideal q-ZSC. The use of non-symmetric components allows identifying the individual effect of each component while non-ideal components allow analyzing the effects of the parasitic resistances of the components.

As common to circuits that change over switching cycle, state space averaging [46] was used to describe the circuit. State space averaging requires generating sets of equations, with each representing a switching state [47] and then averaged over the switching period.

ISCs can be controlled with or without shoot-through [34] or open state. This converter was controlled without using shoot-through or open states in order to enable fair comparisons with the traditional buck-boost converter which is operated using only two switching states (with dead-time) since they have identical gain equation.

Findings from this dynamic modelling show that the parasitic resistances of the capacitors and inductors are among the major factors that determine most of the poles and zeros and circuit efficiency as detailed in the discussion section.

2.   CIRCUIT ANALYSIS

This section is classified into two: gain derivation and state equations derivation. Circuit analysis was done using ideal and real circuits for the gain and state equations derivation respectively. The analyses were done using two switching modes with respect to S_1 while S_2 is complementarily switched with respect to S_1 giving rise to two operation modes shown in Figure 2. The duty ratio of the modes are $'D'$ and $'1-D'$ for modes I and II respectively. C_1, C_2, L_1 and L_2 are capacitors and inductors with currents I_{C1}, I_{C2}, I_{L1} and I_{L2}, and parasitic resistances R_1, R_2, r_1, and r_2 respectively while V_g, I_g, R_O and I_O are input voltage, input current, load resistance and load current respectively.

2.1. Gain Derivation

For simplicity, the ideal circuit of Figure 1(b) was used to derive the topology's ideal gain equation by assuming parasitic resistances R_1, R_2 and r_1, r_2 of the capacitors and inductors of Figure 2 to be negligible.

Mode 1: In this mode as shown in Figure 2(b), S_1 is ON while S_2 is OFF. The duty ratio for this mode is D.

$$V_{L1} = V_O - V_{C1} \tag{1}$$

$$V_{L2} = V_g \tag{2}$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 2(c). The duty ratio for this mode is $D' = 1 - D$.

$$V_{L1} = V_g - V_{C1} \tag{3}$$

$$V_{L2} = V_O \tag{4}$$

Applying Volt-Second-Balance on L_1 and L_2 yields

$$\bar{V}_{L1} = DV_O + V_g - V_{C1} - DV_g = 0 \tag{5}$$

$$\bar{V}_{L2} = DV_g - V_O(D - 1) = 0 \tag{6}$$

From (6),

$$V_O = -\frac{D}{1 - D}V_g \tag{7}$$

(7) Is the ideal steady-state output voltage for this converter. It is the same as the ideal steady state output voltage of buck-boost converter where the two switches are switched complimentarily and D is the duty ratio of S_1 [55].

2.2. State equations derivation

The non-ideal circuits of Figure 2 were used to derive the state equations. The circuit's two operation modes are presented in Figure 2(b) and Figure 2(c) and their duty ratios are "D" and "$1 - D$" for mode I and mode II respectively. $\dot{V}_{C1}, \dot{V}_{C2}, \dot{I}_{C1}$ and $\dot{I}_{L2}$ are the state variables while input voltage (V_g), input current (I_g), and output current (I_O) were chosen as inputs while capacitor voltages V_{C1} and V_{C2}, input current (I_g) and output voltage (V_O) as outputs. This is to identify their suitability for controller design as will be revealed by the averaged model.
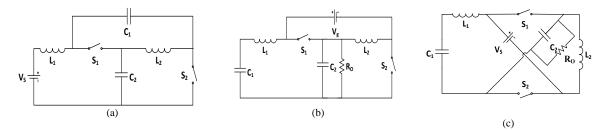

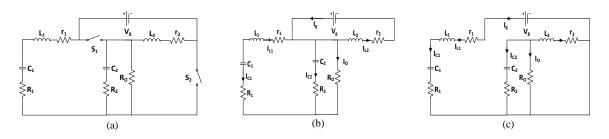Figure 1. (a) Generic q-ZSC (b) Derived DC-DC q-ZSC

Figure 2. (a) Considered circuit with parasitic resistances (b) Circuit in mode I (c) Circuit in mode II

Mode I: In this mode as shown in Figure 2(b), S_1 is ON while S_2 is OFF. L_2 is charged by the input voltage due to the resulting parallel connection. The load, C_1, L_1 and C_2 are all isolated from the input voltage. C_1 and L_1 discharge together to the load while the output filter C_2 absorbs the ac ripples. The mode equations are

$$\dot{V}_{C1} = \frac{I_{L1}}{C_1} \tag{8}$$

$$\dot{V}_{C2} = -\frac{I_{L1}}{C_2} - \frac{I_O}{C_2} \tag{9}$$

$$\dot{I}_{L1} = -\frac{V_{C1}}{L_1} - \left(\frac{R_1 + r_1}{L_1}\right)I_{L1} + \frac{I_O R_O}{L_1} \tag{10}$$

$$\dot{I}_{L2} = -\frac{I_{L2}r_2}{L_2} + \frac{V_g}{L_2} \tag{11}$$

Expressing in state space form $\dot{X}_i = A_i X + B_i U$ where i = 1 for mode 1 yields

$$\dot{X}_1 = \begin{bmatrix} \dot{V}_{C1} \\ \dot{V}_{C2} \\ \dot{I}_{L1} \\ \dot{I}_{L2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & 0 & \frac{-1}{C_2} & 0 \\ \frac{-1}{L_1} & 0 & \frac{-(R_1 + r_1)}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-r_2}{L_2} \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_{L1} \\ I_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} \\ 0 & 0 & \frac{R_O}{L_1} \\ \frac{1}{L_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ I_g \\ I_O \end{bmatrix} \tag{12}$$

For the output, V_{C1}, V_{C2}, I_g and V_O are considered and the output equations are

$$V_{C1} = V_{C1} \tag{13}$$

$$V_{C2} = V_{C2} \tag{14}$$

$$I_g = -I_{L2} \tag{15}$$

$$V_O = I_O R_O \tag{16}$$

Expressing the output equations in the state space for $Y_i = E_i X + F_i U$ where i indicates the mode, i = 1 for mode 1 and i = 2 for mode 2.

$$Y_1 = \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_g \\ V_O \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_{L1} \\ I_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_O \end{bmatrix} \begin{bmatrix} V_g \\ I_g \\ I_O \end{bmatrix} \tag{18}$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 2(c). During this interval, C_1 and L_1 are charged by the input voltage V_g due to the series connection between them while L_1 is isolated from the supply. L_1 discharges to the load while the output filter absorbs the ripples.

$$\dot{V}_{C1} = \frac{I_{L1}}{C_1} \tag{19}$$

$$\dot{V}_{C2} = -\frac{I_{L2}}{C_2} - \frac{I_O}{C_2} \tag{20}$$

$$\dot{I}_{L1} = -\frac{V_{C1}}{L_1} - \left(\frac{R_1 + r_1}{L_1}\right)I_{L1} + \frac{V_g}{L_1} \tag{21}$$

$$\dot{I}_{L2} = -\frac{I_{L2}r_2}{L_2} + \frac{I_O R_O}{L_2} \tag{22}$$

Expressing in state space form $\dot{X}_i = A_i X + B_i U$ where $i = 2$ for mode 2 yields

$$\dot{X}_2 = \begin{bmatrix} \dot{V}_{C1} \\ \dot{V}_{C2} \\ \dot{I}_{L1} \\ \dot{I}_{L2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{C_2} \\ \frac{-1}{L_1} & 0 & \frac{-(R_1 + r_1)}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-r_2}{L_2} \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_{L1} \\ I_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} \\ \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{R_O}{L_2} \end{bmatrix} \begin{bmatrix} V_g \\ I_g \\ I_O \end{bmatrix} \tag{23}$$

The output equations for mode II are:

$$V_{C1} = V_{C1} \tag{24}$$
$$V_{C2} = V_{C2} \tag{25}$$
$$I_g = -I_{L1} \tag{26}$$
$$V_O = I_O R_O \tag{27}$$

Expressing the output in the form $Y_i = E_i X + F_i U$ where $i = 2$ for mode 2 yields

$$Y_2 = \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_g \\ V_O \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_{L1} \\ I_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_O \end{bmatrix} \begin{bmatrix} V_g \\ I_g \\ I_O \end{bmatrix} \tag{28}$$

The state equations are then averaged and expressed as

$$\dot{X} = AX + BU \tag{29}$$

$$Y = EX + FU \tag{30}$$

Where $A = \sum_{i=1}^{n} A_i D_i, B = \sum_{i=1}^{n} B_i D_i, E = \sum_{i=1}^{n} E_i D_i, F = \sum_{i=1}^{n} F_i D_i$, n is the number of switching states involved, i = switched state and D is the duty ratio of the switched state. For this circuit, n = 2 since two switching states are involved (as in typical buck-boost converter), $D_1 = D$ and $D_2 = D' = 1 - D$ for modes I and II respectively. Therefore, $A = A_1 D + A_2(1 - D)$, $B = B_1 D + B_2(1 - D)$, $E = E_1 D + E_2(1 - D)$ and $F = F_1 D + F_2(1 - D)$.

$$\dot{X} = \begin{bmatrix} \dot{V}_{C1} \\ \dot{V}_{C2} \\ \dot{I}_{L1} \\ \dot{I}_{L2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & 0 & \frac{-D}{C_2} & \frac{-(1-D)}{C_2} \\ \frac{-1}{L_1} & 0 & \frac{-(R_1+r_1)}{L_1} & \frac{0}{L_1} \\ 0 & 0 & 0 & \frac{-r_2}{L_2} \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_{L1} \\ I_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_2} \\ \frac{(1-D)}{L_1} & 0 & \frac{DR_O}{L_1} \\ \frac{D}{L_2} & 0 & \frac{(1-D)R_O}{L_2} \end{bmatrix} \begin{bmatrix} V_g \\ I_g \\ I_O \end{bmatrix} \tag{31}$$

$$Y = \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_g \\ V_O \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & -(1-D) & -D \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ I_{L1} \\ I_{L2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_O \end{bmatrix} \begin{bmatrix} V_g \\ I_g \\ I_O \end{bmatrix} \tag{32}$$

(31) And (32) are the modelled averaged steady-state equations of the circuit. The choice of V_O and I_O as output and input respectively resulted in the feedforward matrices in (18), (28) and (32) nonzero. If V_O is not considered as output, all these feedforward matrices will be zero. However, the choice of Ig as both output and input didn't

affect the feedforward matrices nor any input matrix because the system's steady-state response is independent of the input I_g but V_g and I_O. This is important in controller design.

3. SMALL SIGNAL ANALYSIS

Small signal perturbations $\tilde{d}(t), \tilde{v}_g(t), \tilde{\imath}_g(t)$ and $\tilde{\imath}_O(t)$ are applied to the steady-state duty ratio (D) and input variables (V_g, I_g, and I_O) respectively to obtain the small signal model. These perturbations cause the dynamic state variables v_{C1}, v_{C2}, i_{L1} and i_{L2} to vary by $\tilde{v}_{C1}, \tilde{v}_{C2}, \tilde{\imath}_{L1}$ and $\tilde{\imath}_{L2}$ respectively [56]. The relationship between a dynamic variable x, its steady state value X and perturbation $\tilde{x}$ is given as

$$x = X + \tilde{x} \tag{33}$$

Differentiating (33) with respect to time yields

$$\dot{x} = \dot{X} + \dot{\tilde{x}} \tag{34}$$

Steady-state variables in (29) are substituted with dynamic variables for small signal analysis to yield (35)

$$\dot{x} = (A_1 d + A_2(1 - d))x + (B_1 d + B_2(1 - d))u \tag{35}$$

Substituting (33) and (34) into (35), neglecting products of two small signal perturbations and rearranging yields

$$\dot{X} + \dot{\tilde{x}} = AX + BU + A\tilde{x} + B\tilde{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\tilde{d} \tag{36}$$

(36) Is the generalised large signal state equation for a model. Matching steady state and perturbation terms together shows

$$\dot{X} = AX + BU = 0 \tag{37}$$

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\tilde{d} \tag{38}$$

(37) = 0 because derivative of a constant (steady state) $\dot{X} = 0$. (37) Is the generalised steady state model while (38) is generalised small signal model.
Simplifying (36) further yields

$$X = -BUA^{-1} \tag{39}$$

Similarly, for the steady state output $Y = EX + FU$, its dynamic signal after small signal analysis is given as

$$y = Y + \tilde{y} = EX + FU + E\tilde{x} + F\tilde{u} + [(E_1 - E_2)X + (F_1 - F_2)U]\tilde{d} \tag{40}$$

(40) Is the generalized large signal output equation for a model. Matching steady state and perturbation terms together shows

$$Y = EX + FU \tag{41}$$

$$\tilde{y} = E\tilde{x} + F\tilde{u} + [(E_1 - E_2)X + (F_1 - F_2)U]\tilde{d} \tag{42}$$

(41) Is the generalized steady state output equation while (42) is the generalised small signal equation.
Substituting (39) into (41) yields

$$Y = -EBUA^{-1} + FU \tag{43}$$

$$Y = (F - EBA^{-1})U \tag{44}$$

Evaluating and simplifying (38) yields (45) to (48)

$$\dot{\tilde{v}}_{C1} = \frac{\tilde{i}_{L1}}{C_1} \tag{45}$$

$$\dot{\tilde{v}}_{C2} = \frac{-D\tilde{i}_{L1} - (1-D)\tilde{i}_{L2} - \tilde{i}_0 + (I_{L2} - I_{L1})\tilde{d}}{C_2} \tag{46}$$

$$\dot{\tilde{i}}_{L1} = \frac{-\tilde{v}_{C1} - (R_1 + r_1)\tilde{i}_{L1} + (1-D)\tilde{v}_g + (DR_0)\tilde{i}_0 + (I_0 R_0 - V_g)\tilde{d}}{L_1} \tag{47}$$

$$\dot{\tilde{i}}_{L2} = \frac{-r_2 \tilde{i}_{L2} + D\tilde{v}_g + (1-D)R_0 \tilde{i}_0 + (V_g - I_0 R_0)\tilde{d}}{L_2} \tag{48}$$

Taking Laplace transform and simplification yields

$$sC_1 \tilde{v}_{c1}(s) = \tilde{i}_{L1}(s) \tag{49}$$

$$sC_2 \tilde{v}_{c2}(s) = -D\tilde{i}_{L1}(s) - (1-D)\tilde{i}_{L2}(s) - \tilde{i}_0(s) + (I_{L2} - I_{L1})\tilde{d}(s) \tag{50}$$

$$(sL_1 + R_1 + r_1)\tilde{i}_{L1}(s) = -\tilde{v}_{C1}(s) + (1-D)\tilde{v}_g(s) + (DR_0)\tilde{i}_0(s) + (I_0 R_0 - V_g)\tilde{d}(s) \tag{51}$$

$$(sL_2 + r_2)\tilde{i}_{L2}(s) = \tilde{i}_{L2}(s) + D\tilde{v}_g(s) + R_0(1-D)\tilde{i}_0(s) + (V_g - I_0 R_0)\tilde{d}(s) \tag{52}$$

Further simplification and substitutions yields

$$\tilde{v}_{c1}(s) = \frac{(1-D)\tilde{v}_g(s) + (DR_0)\tilde{i}_0(s) + (I_0 R_0 - V_g)\tilde{d}(s)}{(sL_1 + R)(sC_1 + 1)} \tag{53}$$

$$\tilde{v}_{c2}(s) = -\frac{s^2(L_1 + L_2) + s(R + r_2) + \frac{1}{C_1}}{(s^2 C_1 L_1 + sC_1 R + 1)(sL_2 + r_2)s\frac{C_2}{C_1}} DD'\tilde{v}_g$$

$$- \frac{s^3 L_1 L_2 + s^2(L_2(D^2 R_0 + R) + L_1(R_0 D'^2 + r_2)) + s(R_0 D'^2 R + r_2(R + D^2 R_0) + \frac{L_2}{C_1}) + \frac{R_0 D'^2 + r_2}{C_1}}{(s^2 C_1 L_1 + sC_1 R + 1)(sL_2 + r_2)s\frac{C_2}{C_1}} \tilde{i}_0(s)$$

$$+ \frac{s^3 L_1 L_2 I + s^2(L_1 r_2 I + L_2 RI + DL_2 V - D'L_1 V) + s(Rr_2 I + \frac{L_2}{C_1}I + Dr_2 V + Dr_2 - D'RV) + \frac{r_2 I - D'V}{C_1}}{(s^2 C_1 L_1 + sC_1 R + 1)(sL_2 + r_2)s\frac{C_2}{C_1}} \tilde{d}(s) \tag{54}$$

$$\tilde{i}_{L1}(s) = \frac{SC_1(1-D)\tilde{v}_g(s) + SC_1 DR_0 \tilde{i}_0(s) + SC_1(I_0 R_0 - V_g)\tilde{d}(s)}{s^2 C_1 L_1 + sC_1 R + 1} \tag{55}$$

$$\tilde{i}_{L2}(s) = \frac{D\tilde{v}_g(s) + R_0(1-D)\tilde{i}_0(s) + (V_g - I_0 R_0)\tilde{d}(s)}{sL_2 + r_2} \tag{56}$$

where $R = R_1 + r_1$, $V = V_g - V_0$, $D' = 1 - D$ and $I = I_{L2} - I_{L1}$.

The small signal equations of the states $\tilde{v}_{c1}(s)$ and $\tilde{v}_{c2}(s)$ as shown in (53) and (54) are not identical, likewise $\tilde{i}_{L1}(s)$ and $\tilde{i}_{L2}(s)$ as shown in (55) and (56) are also non identical. An explanation to this non-identicality is due to the asymmetry of this topology. This asymmetry is explained by the difference in the gain curves obtained when taking the output across C_1 as done in [13] and when taken across C_2 as done in this presentation. The gain of the two variant topologies shows that for any given operational parameters, $V_{C1} \neq V_{C2}$. The models presented in [41], [44] have the above-mentioned states to be identical because inverters were considered and not DC-DC converter thus the topologies are entirely different. However, the poles of $\tilde{i}_{L1}(s)$ and $\tilde{i}_{L2}(s)$ are contained in the poles of $\tilde{V}_{C2}(s)$ thus (55) and (56) could be re-written as

$$\tilde{\imath}_{L1}(s) = \frac{SC_1(1-D)\tilde{v}_g(s) + SC_1 DR_0 \tilde{\imath}_0(s) + SC_1(I_0 R_0 - V_g)\tilde{d}(s)}{\left(s^2 C_1 L_1 + sC_1 R + 1\right)(sL_2 + r_2)s\dfrac{C_2}{C_1}} \; (sL_2 + r_2)s\frac{C_2}{C_1} \tag{55a}$$

$$\tilde{\imath}_{L2}(s) = \frac{D\tilde{v}_g(s) + R_0(1-D)\tilde{\imath}_0(s) + (V_g - I_0 R_0)\tilde{d}(s)}{\left(s^2 C_1 L_1 + sC_1 R + 1\right)(sL_2 + r_2)s\dfrac{C_2}{C_1}} \left(s^2 C_1 L_1 + sC_1 R + 1\right)s\frac{C_2}{C_1} \tag{56b}$$

3.1. Transfer functions

The small signal models presented in (53) to (56) were used to obtain the transfer functions ($G_{input}^{\overline{state}}$) between state variable and system input. This was done by considering one system input at a time and assuming other system inputs to be zero [41], [44], [48].

$$G_{\tilde{v}_g}^{\tilde{v}_{C1}} = \frac{(1-D)}{(sL_1 + R)(sC_1 + 1)} \tag{57}$$

$$G_{i_0}^{\tilde{v}_{C1}} = \frac{DR_0}{(sL_1 + R)(sC_1 + 1)} \tag{58}$$

$$G_{\tilde{d}}^{\tilde{v}_{C1}} = \frac{(I_0 R_0 - V_g)}{(sL_1 + R)(sC_1 + 1)} \tag{59}$$

$$G_{\tilde{v}_g}^{\tilde{v}_{C2}} = -\frac{[s^2(L_1 + L_2) + s(R + r_2) + \frac{1}{C_1}]DD'}{(s^2 C_1 L_1 + sC_1 R + 1)(sL_2 + r_2)s\dfrac{C_2}{C_1}} \tag{60}$$

$G_{\tilde{\imath}_0}^{\tilde{v}_{C2}}$

$$= -\frac{s^3 + s^2(\frac{L_2(D^2 R_0 + R) + L_1(R_0 D'^2 + r_2)}{L_1 L_2}) + s(\frac{R_0 C_1 D'^2 R + r_2 C_1(R + D^2 R_0) + L_2}{L_1 L_2 C_1}) + \frac{R_0 D'^2 + r_2}{L_1 L_2 C_1}}{(s^2 C_1 L_1 + sC_1 R + 1)(sL_2 + r_2)s\dfrac{C_2}{C_1}} \tag{61}$$

$G_{\tilde{d}}^{\tilde{v}_{C2}}$

$$= \frac{s^3 L_1 L_2 I + s^2(L_1 r_2 I + L_2 RI + DL_2 V - D'L_1 V) + s(Rr_2 I + \frac{L_2}{C_1}I + Dr_2 V + Dr_2 - D'RV) + \frac{r_2 I - D'V}{C_1}}{(s^2 C_1 L_1 + sC_1 R + 1)(sL_2 + r_2)s\dfrac{C_2}{C_1}} \tag{62}$$

$$G_{\tilde{v}_g}^{\tilde{\imath}_{L1}} = \frac{SC_1(1-D)}{s^2 C_1 L_1 + sC_1 R + 1} \tag{63}$$

$$G_{\tilde{\imath}_0}^{\tilde{\imath}_{L1}} = \frac{SC_1 DR_0}{s^2 C_1 L_1 + sC_1 R + 1} \tag{64}$$

$$G_{\tilde{d}}^{\tilde{\imath}_{L1}} = \frac{SC_1(I_0 R_0 - V_g)\tilde{d}}{s^2 C_1 L_1 + sC_1 R + 1} \tag{65}$$

$$G_{\tilde{v}_g}^{\tilde{\imath}_{L2}} = \frac{D}{sL_2 + r_2} \tag{66}$$

$$G_{\tilde{\imath}_0}^{\tilde{\imath}_{L2}} = \frac{R_0(1-D)}{sL_2 + r_2} \tag{67}$$

$$G_{\tilde{d}}^{\tilde{\imath}_{L2}} = \frac{(V_g - I_0 R_0)\tilde{d}(s)}{sL_2 + r_2} \tag{68}$$

4.   ANALYSIS

The poles and zeros of the transfer functions are discussed in this section. Roots of functions not greater than degree 2 are fully discussed while those of degree 3 and 4 are just introduced due to the complexity involved. Pole-zero maps have been used to analyse dynamic models of dc-ac ISCs [41], [44], [45], [48], [49], [51], analytical method is used here for analyses due to the asymmetry of this topology which resulted in (62) having so many variables.

a.   Starting with the first transfer function $G_{\tilde{V}_g}^{\tilde{V}_{C1}}$, together with $G_{\tilde{I}_0}^{\tilde{V}_{C1}}$ and $G_{\tilde{d}}^{\tilde{V}_{C1}}$, they have two poles all negative located at $s = -\frac{R_1 + r_1}{L_1}$ and $s = \frac{-1}{C_1}$. They all have no zero.

b. $G_{\tilde{V}_g}^{\tilde{V}_{C2}}$ together with $G_{\tilde{I}_0}^{\tilde{V}_{C2}}$ and $G_{\tilde{d}}^{\tilde{V}_{C2}}$, they have four poles all non-positive located at $0, -\frac{r_2}{L_2}$ and $-\frac{R}{2L_1} \pm$ $\frac{\sqrt{\left(\frac{R}{L_1}\right)^2 - \left(\frac{4}{C_1 L_1}\right)}}{2}$. The pole $-\frac{R}{2L_1} + \frac{\sqrt{\left(\frac{R}{L_1}\right)^2 - \left(\frac{4}{C_1 L_1}\right)}}{2}$ is also non positive because $\frac{\left(\frac{R}{L_1}\right)^2 - 4\left(\frac{1}{C_1 L_1}\right)}{4} \not> \left(\frac{R}{2L_1}\right)^2 \Rightarrow \frac{-1}{C_1 L_1} \not> 0$ since C_1 and L_1 are all positive. Provided $\left(\frac{R}{L_1}\right)^2 \geq 4\left(\frac{1}{C_1 L_1}\right)$, or simply $L_1 \leq \frac{C_1}{4} R^2$, it has all real non-positive poles. It has two zeros at $-\frac{R+r_2}{2(L_1+L_2)} \pm \sqrt{\left(\frac{R+r_2}{2(L_1+L_2)}\right)^2 - \left(\frac{1}{C_1(L_1+L_2)}\right)}$ all the zeros are negative because $\left(\frac{R+r_2}{2(L_1+L_2)}\right)^2 - \left(\frac{1}{C_1(L_1+L_2)}\right) \not\geq \left(\frac{R+r_2}{2(L_1+L_2)}\right)^2$ since $\frac{-1}{C_1(L_1+L_2)} \not\geq 0$ due to the fact that both C_1, L_1 and L_2 are all positive.

c. $G_{\tilde{I}_0}^{\tilde{V}_{C2}}$ has three zeros and their locations can be analysed based on the given operating conditions because the polynomial being of degree three and with so many parameters makes it difficult to present a generalised analysis.

d. $G_{\tilde{d}}^{\tilde{V}_{C2}}$ has three zeros and are given by the roots of the polynomial $s^3 L_1 L_2 I + s^2(L_1 r_2 I + L_2 RI + DL_2 V - D'L_1 V) + s(Rr_2 I + \frac{L_2}{C_1} I + Dr_2 V + Dr_2 - D'RV) + \frac{r_2 I - D'V}{C_1}$. Analysing the behaviour of all the possible roots of this cubic polynomial analytically is complex and involves so much mathematics beyond the scope of this paper because I and V are variables whose values vary for different operating points. This is evident as [41], [44] also analysed their quadratic $G_{\tilde{d}}^{\tilde{V}_{C1}}$ by considering the parameters of a given circuit under given conditions. However, limited cases will be considered such as

$I_{L1} = I_{L2}$. If $I_{L1} = I_{L2}$, the polynomial reduces to degree two as

$s^2 + s\left(\frac{Dr_2 + \frac{Dr_2}{V} - D'R}{DL_2 - D'L_1}\right) - \frac{D'}{(DL_2 - D'L_1)C_1}$. Its roots are given by

$-\frac{Dr_2 + \frac{Dr_2}{V} - D'R}{2(DL_2 - D'L_1)} \pm \sqrt{\left(\frac{Dr_2 + \frac{Dr_2}{V} - D'R}{2(DL_2 - D'L_1)}\right)^2 - \frac{D'}{(DL_2 - D'L_1)C_1}}$.

$I_{L1} = I_{L2}$ and $V_g = V_O$, the equation reduces to sDr_2 thus the zero exist at origin ($s = 0$).

As shown by these two cases, the nature of the zeros varies for different points. An important point to note is that right-hand plane (RHP) zero may exist outside the conditions of case II. The existence of this RHP zero was also noticed in ZSI and q-ZSI which implies control limitations and high gain instability [41], [44], [45], [48], [49] thereby destabilizing the feedback loop.

e. $G_{\tilde{V}_g}^{\tilde{I}_{L1}}, G_{\tilde{I}_0}^{\tilde{I}_{L1}}$ and $G_{\tilde{d}}^{\tilde{I}_{L1}}$ have all negative poles located at $-\frac{R}{2L_1} \pm \frac{\sqrt{\left(\frac{R}{L_1}\right)^2 - \left(\frac{4}{C_1 L_1}\right)}}{2}$. The poles are all negative because $\left(\frac{R}{L_1}\right)^2 - \left(\frac{4}{C_1 L_1}\right) \not\geq \left(\frac{R}{L_1}\right)^2$ since $\frac{-4}{C_1 L_1} \not\geq 0$. The poles are real provided $L_1 \leq C_1 \left(\frac{R}{2}\right)^2$. They all have single zero and is located at $s = 0$.

f. $G_{\tilde{V}_g}^{\tilde{I}_{L2}}, G_{\tilde{I}_0}^{\tilde{I}_{L2}}$ and $G_{\tilde{d}}^{\tilde{I}_{L2}}$ have a single pole and no zero. The pole is located at $s = -\frac{r_2}{L_2}$.

From the above analysis, it can be deduced that the transfer functions $G_{\tilde{V}_g}^{\tilde{V}_{C1}}, G_{\tilde{I}_0}^{\tilde{V}_{C1}}$ and $G_{\tilde{d}}^{\tilde{V}_{C1}}$ derived from the state $\tilde{v}_{c1}(s)$ and $G_{\tilde{V}_g}^{\tilde{I}_{L2}}, G_{\tilde{I}_0}^{\tilde{I}_{L2}}$ and $G_{\tilde{d}}^{\tilde{I}_{L2}}$ derived from the state $\tilde{i}_{L2}(s)$ are generally stable regardless of parameter values. All their poles are negative-real and have no zeros. Smaller L_1 and C_1 increase the stability of the transfer functions $G_{\tilde{V}_g}^{\tilde{V}_{C1}}, G_{\tilde{I}_0}^{\tilde{V}_{C1}}$ and $G_{\tilde{d}}^{\tilde{V}_{C1}}$ by pushing their poles away from origin. Also, smaller L_2 will increase the system stability due to $G_{\tilde{V}_g}^{\tilde{I}_{L2}}, G_{\tilde{I}_0}^{\tilde{I}_{L2}}$ and $G_{\tilde{d}}^{\tilde{I}_{L2}}$ by pushing their poles further away from the origin. Smaller values of L_2 rather than larger values of r_2 are preferred because r_2 being a parasitic resistance will increase non-ideality such as parasitic voltage drop thereby reducing efficiency.

The transfer functions $G_{\tilde{v}_g}^{\tilde{i}_{L1}}, G_{\tilde{i}_O}^{\tilde{i}_{L1}}$ and $G_{\tilde{d}}^{\tilde{i}_{L1}}$ derived from the state $\tilde{i}_{L1}(s)$ have marginal gain stability due to zero at the origin which implies control limitation [44]. Although all their poles are all negative, oscillations may occur if $L_1 > C_1 \left(\frac{R}{2}\right)^2$ due to the existence of a complex conjugate pair, else, the poles are negative and real with a smaller value of L_1 pushing them further away from the origin.

It is now clear that the transfer functions $G_{\tilde{v}_g}^{\tilde{v}_{C2}}, G_{\tilde{i}_O}^{\tilde{v}_{C2}}$ and $G_{\tilde{d}}^{\tilde{v}_{C2}}$ derived from $\tilde{v}_{c2}(s)$ are the most crucial because they indicate marginal stability due to the existence of a pole at origin and oscillation may occur if $L_1 > \frac{C_1}{4} R^2$ due to the existence of complex conjugate pole pair. The zeros of $G_{\tilde{v}_g}^{\tilde{v}_{C2}}$ are all negative. From all the above analysis, it shows that the possibility of positive roots only exists in the zeros of $G_{\tilde{i}_O}^{\tilde{v}_{C2}}$ and $G_{\tilde{d}}^{\tilde{v}_{C2}}$ which signifies control limitation and high gain instability and also exists in the ZSI and q-ZSI. This shows that the ZSI, q-ZSI and this DC-DC q-ZSC are non-minimum phase systems [48].

5.   VERIFICATION

To verify these findings, operations of two converters were compared by simulating their performance on input voltage $V_g = 12$ V, duty ratio D = 0.63 and 7 Ω load using MATLAB SIMULINK. On one side was a converter based on arbitrary symmetric components as $C_1 = C_2 = 400 \,\mu F, L_1 = L_2 = 500 \,\mu H$, $R_1 = R_2 = 0.03$ Ω, $r_1 = r_2 = 0.47$ Ω while on the other was another converter with carefully selected asymmetric components based on the optimization equations derived in (62) by only modifying the optimization capacitor and inductor to $C_1 = 80$ µF and $L_1 = 4$ µH as shown in Table 1. The new smaller values of C_1 and L_1 pushes the poles of $G_{\tilde{v}_g}^{\tilde{v}_{C1}}, G_{\tilde{d}}^{\tilde{v}_{C1}}$ and $G_{\tilde{i}_O}^{\tilde{v}_{C1}}$ further away on the left hand plane (LHP).

Although the values of R_1 and r_1 are proportional to C_1 and R_1 respectively, and each can influence the position, the choice of smaller L_1 and C_1 are preferred due to the inefficiency associated with parasitic resistances and other constraints such as weight and size associated with larger capacitors and inductors. The new values of C_1 and L_1 also ensures that the poles of the TFs of $\tilde{v}_{C2}$ and $\tilde{i}_{L1}$ are real and non-positive instead of the complex pole that existed from $C_1 = 400$ µF and $L_1 = 500$ µH. The response of the two circuits with respect to output voltage (V_O), output current (I_O) and input current (I_g) are presented in Figure 3. Figure 4 (a) shows the ideal gain curve of the converter.

Their operations were also compared using ideal components by neglecting the parasitic resistances R_1, R_2, r_1 and r_2 for both the optimized and symmetric circuits in order to compare their output voltages with the ideal steady state output voltage of (7) and identify the effects of the parasitic resistances as shown in Figure 4(b) and (c).

Table 1. Parameter values used for simulation

Parameter	Value	
	Symmetric	Optimized
V_g (V)	12	12
D	0.63	0.63
f (KHz)	100	100
C_1 (µF)	400	80
C_2 (µF)	400	400
L_1 (µH)	500	4
L_2 (µH)	500	500
R_1 (Ω)	0.03	0.03
R_2 (Ω)	0.03	0.03
r_1 (Ω)	0.47	0.47
r_2 (Ω)	0.47	0.47
Load (Ω)	7	7

6.   RESULTS AND DISCUSSION

Results of Figure 3 confirm the validity of these equations because the output voltage and output current of the optimized circuit are 15.25 V and 2.18 A against 13.15 V and 1.87 A obtained without optimization respectively. This is because the optimization capacitor C_1 and inductor L_1 were selected based on the equations derived from this model as discussed in the Analysis and Verification sections rather than symmetry. This increase represents a magnitude increase of 16.35 % and 16.58% for the output voltage and output current

respectively. The optimized outputs both have ripples of $< 3\%$. The wave shape of the input current changed from the previous pulsating square wave to saw-tooth after the optimization as shown in Figure 3(c).

Plot of the ideal gain against duty ratio of the converter obtained from (7) is shown in Figure 4(a). From (7), the magnitude of the ideal steady-state output voltage for this converter at input voltage (V_g) of 12 V and duty ratio (D) of 0.63 is 20.43 V. This is greater than the average output voltages of 15.25 V and 13.15 V obtained from simulation results of Figure 3(a) for both the optimized real and the symmetric real circuits respectively due to voltage drops across the parasitic resistances. The parasitic voltage drops are dependent on the magnitude of the parasitic resistances and the currents flowing in the circuits. This also shows that the optimized circuit has less parasitic voltage drop than the symmetric (non-optimized) circuit thus implying higher efficiency. This is further verified in Figure 4(b) and (c) where responses of the same circuits without parasitic resistances are also presented. The ideal circuits' steady-state responses in Figure 4(b) shows increased output voltages to about 20.43 V and 19.20 V due to the elimination of parasitic voltage drops. This implies that the response of the simulated ideal optimized circuit is the same as the ideal analytical output voltage magnitude of 20.43 V in (69), which is about 6.41 % higher than the 19.20 V for the ideal symmetric circuit. This further verifies the validity of the model derived here.
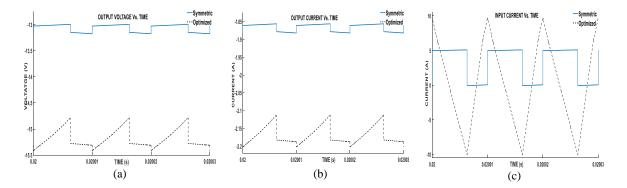

Figure 3. Simulation results of the same converter but different parameters with the solid blue line representing a symmetric circuit and the dashed black line representing a carefully selected (optimized) values based on this modelling (a) Output Voltage (b) Output Current (c) Input Current
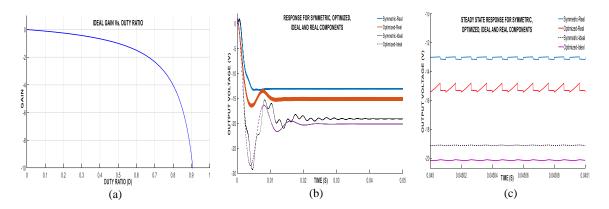

Figure 4. (a) Converter's ideal gain curve (b) Converter's transient response for 0>t<0.05s using symmetric-real, optimized-real, symmetric-ideal and optimized-ideal components (c) Convert's steady state response using symmetric-real, optimized-real, symmetric-ideal and optimized-ideal components

7.   CONCLUSION

A dynamic model of a DC-DC q-ZSC with buck-boost converter gain has been presented. The modelling considered non-symmetric non-ideal capacitors and inductors. The use of non-ideal components was fruitful because it was found that they have a significant effect on the poles and zero positions of most of the transfer functions. It was also found that similar to the existing impedance source converters, there may also exist right-hand plane (RHP) zero in the duty ratio to output capacitor voltage. It was also found and verified that rather than using symmetric components, use of carefully selected smaller asymmetric components produces

less parasitic voltage drop, higher output voltage and current under the same conditions. This means better performance and efficiency at reduced cost, size and weight because smaller components could be used to achieve the required optimization ratios where applicable.

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