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Proposal and design methodology of switching mode low dropout regulator for bio-medical applications

Kenya Kondo[1], Hiroki Tamura[2], Koichi Tanno[3]
[1]Interdisciplinary Graduate School of Agriculture and Engineering, University of Miyazaki, Japan
[2]Department of Environmental Robotics, University of Miyazaki, Japan
[3]Department of Electrical and System Engineering, University of Miyazaki, Japan

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ABSTRACT

The switching operation based low dropout (LDO) regulator utilizing on-off control is presented. It consists of simple circuit elements which are comparator, some logic gates, switched capacitor and feedback circuit. In this study, we target the application to the power supply circuit for the analog front end (AFE) of bio-medical system (such as daily-used bio-monitoring devices) whose required maximum load current is 50 μA. In this paper, the design procedure of the proposed LDO has been clarified and actual circuit design using the procedure has been done. The proposed LDO has been evaluated by SPICE simulation using 1P 2M 0.6 μm CMOS process device parameters. From simulation results, we could confirm that the low quiescent current of 1 μA with the output ripple of 5 mVpp. The circuit area is 0.0173 mm^2 in spite of using 0.6 μm design rules. The proposed circuit is suitable for adopting to the light load and low frequency applications.

Corresponding Author:

Koichi Tanno,
Department of Electrical and System Engineering,
Institute of Education and Research for Engineering, University of Miyazaki,
1-1 Gakuenkibanadai-Nishi, Miyazaki, 889-2192, Japan.
Email: tanno@cc.miyazaki-u.ac.jp

1. INTRODUCTION

Recently expanding demands for bio-medical devices have driven extensive research on low-power mixed-signal integrated circuit technologies [1-6]. The building blocks of the analog front-end (AFE) in the bio-medical system-on-chip (SoC) like as instrumentation amplifier (IA), programmable gain amplifier (PGA), low-pass filter (LPF) and analog-to-digital converter (ADC) require the power supply voltages suitable for each, therefore the multiple low dropout (LDO) regulators are implemented as the post-regulators following the dc-dc converters to achieve high-efficiency power management solution [5-6]. Although the conventional analog-LDOs (ALDOs) have some advantages like as low-noise, high power supply rejection ratio (PSRR) and high accuracy, they occupy the large circuit area due to power MOS transistor operated in saturation region [7-9]. This causes the circuit area increase of the power management unit (PMU) in SoC, therefore the importance of developing area-efficient LDO is growing up. On the other hand, the dynamic range and frequency range of the bio-potential signals are limited such as μV to mV in the dynamic range and sub-1 Hz to a few kHz in the frequency [10]. In the bio-medical signal processing, the on-chip or off-chip high-pass and low-pass filters which have the very low cut-off frequency are often used to eliminate dc voltage (ac-coupling) and unexpected high frequency noise [3]–[6],[10]. On the signal band design aspect, since AFE eliminates out-of-band noise by own LPF, the power supply noise specification at high frequency can be alleviated. Therefore, the switching power supply circuit like as digital-LDOs (DLDOs) can be applied to AFE of the bio-medical

SoC. However, DLDO has a complicated system architecture and its circuit design becomes difficult.

As an ultra-low area LDO, the switching mode LDO utilizing the on-off hysteretic control have been proposed in [15]. Although its maximum output current ability is small as 100 μA, its circuit design is very simple by utilizing on-off hysteretic control, and the circuit area is very small as 0.001 mm^2. Thus, this is very effective method for area minimization. In the bio-medical application, since the amplifier and filter used in AFE treat a small dynamic range and low frequency band, these circuits are often designed by using the subthreshold region [4]. Therefore, large output current of LDO in this application is not required. However, since its output ripple voltage is large as 47 mV and the ripple frequency (switching frequency) is low as a few kHz, its output ripple may interfere with the signal band of the AFE of the bio-medical SoC. Furthermore, the LDO proposed in [15] uses the Schmitt trigger inverter to define the magnitude of the output ripple, therefore design for reducing output ripple is essentially difficult. Hence, [15] states that this topology is suitable only for circuits with low sensitivity to supply voltage ripples such as digital circuits.

In order to enable the area-efficient switching mode LDO application to bio-medical AFE, in this paper, we propose a method to control the ripple voltage and switching frequency with circuit delay. The proposed circuit consists of comparator, logic circuit, switched capacitor and feedback circuit. From mathematical analysis of the switching operation, the design procedure of output ripple and switching cycle time of the proposed regulator can be clarified. The ripple voltage and switching frequency are controlled by the response time of the comparator which is tuned by adjusting the tail current of the comparator. From this feasibility study, we confirmed the proposed circuit can be adopted to AFE of bio-medical system when the output ripple of the proposed circuit is designed to eliminate properly by LPF in the AFE.

This paper consists of 5 chapters. Chapter 2 presents the basic topology and detail of the design guideline derivation of the proposed topology. Chapter 3 presents the practical circuit design example. The simulation results are shown in Chapter 4, followed by the conclusion in Chapter 5.

2. CONVENTIONAL SWITCHING MODE LDO

Figure 1 (a) and (b) respectively show the circuit schematic and the conceptual waveform of conventional switching mode LDO which consists of Schmitt trigger comparator and pass switch [15]. Schmitt trigger comparator consists of Schmitt trigger inverter and pre-amplifier. The on/off time of the pass switch depends on the hysteresis voltage V_{hys} and delay time T_{delay} of Schmitt trigger comparator, and the output voltage ripple Δv_{out} also depends on them. In general, the hysteresis voltage of Schmitt trigger inverter is large variation because of it has high sensitivity with the process variation and mismatch of the transistor, and it is difficult to design it smaller than a few tens of mV. Therefore, design for reducing output ripple of the conventional switching mode LDO is essentially difficult.

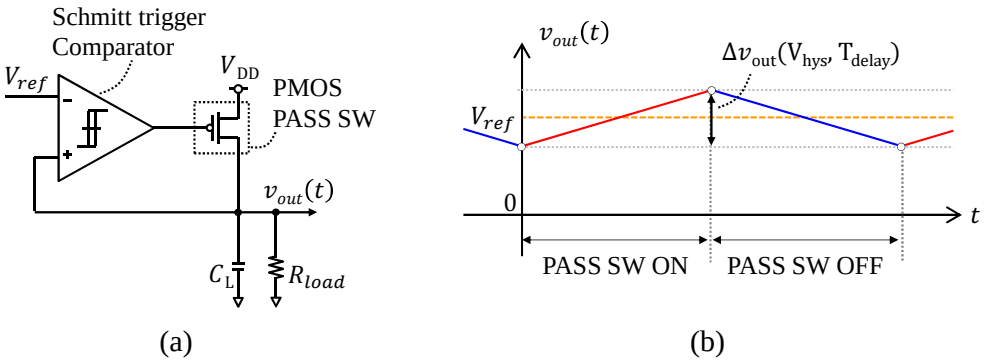


Figure 1. Conventional switching mode LDO. (a) Circuit schematic. (b) Conceptual waveform.

3. CONCEPT OF PROPOSED CIRCUIT AND DERIVATION OF DESIGN GUIDELINES

Figure 2 (a) shows the conceptual circuit model of the proposed circuit. The proposed circuit consists of switched capacitor circuit, logic circuit, comparator and feedback circuit. The switched capacitor circuit as the output stage consists of the PMOS switch with on resistance R_{out} and decoupling capacitor C_L. V_{DD} is the

power supply voltage. The resistor R_{load} means the load resistor, and I_{load} is provided by the proposed circuit. The logic circuit is simple logic gate like as the inverter and NAND gate, and are implemented for adjusting size of the output PMOS switch. Its total propagation delay time is T_{delay}. The feedback circuit senses the output voltage $v_{out}(t)$, and it feedbacks $\beta v_{out}(t)$ to input. The feedback factor is $\beta = R_{fb1}/(R_{fb1} + R_{fb2})$. The comparator compares the voltage between the reference voltage V_{ref} and $\beta v_{out}(t)$, and it controls the on/off time of the switched capacitor circuit. The equivalent circuit of the comparator can be modeled by the ideal quantizer and the amplifier which has the finite DC gain $A_v = g_m R$ and time constant RC as shown in top left of Figure 2 (a). Where $v_e(t)$ is the input voltage of the comparator, $v_{amp}(t)$ is the output voltage of the amplification stage, $v_{comp}(t)$ is the output voltage of the ideal quantizer, g_m is the transconductance, R is the equivalent output resistance of the transconductance amplifier, C is the parasitic capacitance which is total capacitance of the output node of the transconductance amplifier. The average output voltage V_{out} in the steady state is given as follows. This equation is identical to general LDO.

$$V_{out} = \frac{A_v}{1 + \beta A_v} V_{ref} \tag{1}$$

In the following subsections, the circuit operation in the steady state is analyzed in detail, and the design guidelines of the circuit parameters with regards to the circuit specification are defined.

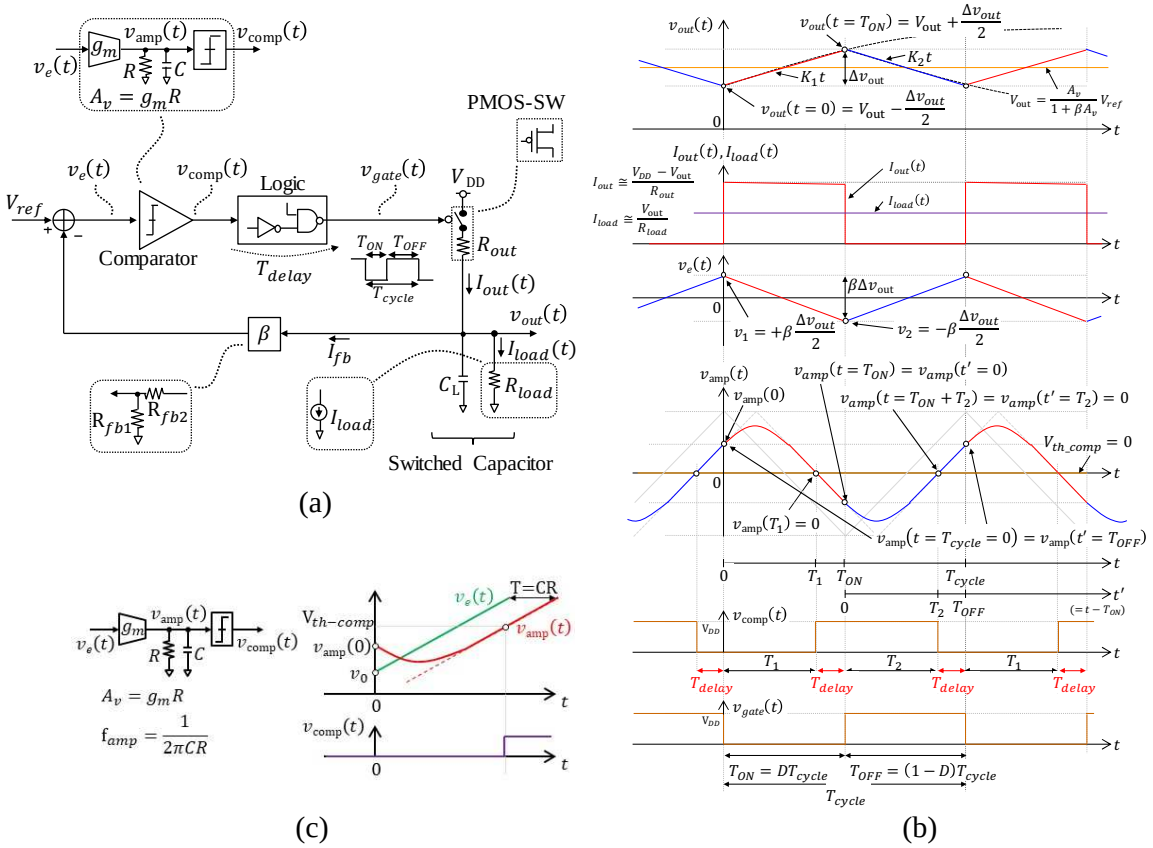


Figure 2. Conceptual models of the proposed circuit. (a) Circuit model. (b) Typical waveforms in the steady state under the condition of the duty ratio 50%. (c) Transient ramp response of the comparator.

3.1. Design Guideline of Output Switched Capacitor

Figure 2 (b) shows the typical waveforms of each node in the steady state. In the beginning, we analyze the charge and discharge operation of the output switched capacitor circuit in the steady state. It clarifies the design guideline of the output PMOS switch R_{out} when the design parameters V_{out}, V_{DD}, R_{load} (I_{load}) are

given as a specification. The charging time T_{ON} and the discharging time T_{OFF} are automatically controlled by the negative feedback. The switching cycle time T_{cycle} is given by $T_{ON} + T_{OFF}$.

In the charging period ($0 \leqq t < T_{ON}$), the PMOS switch turns on, and charge operation occurs by RC step response. The behavior of $v_{out}(t)$ is presented by differential equation (2).

$$\frac{R_{load}}{R_{out} + R_{load}} V_{DD} = C_L R'_{out} \frac{dv_{out}(t)}{dt} + v_{out}(t) \tag{2}$$

where $R'_{out} = R_{out}R_{load}/(R_{out} + R_{load})$, and the current of the feedback circuit $I_{fb} = V_{ref}/R_{fb1}$ is neglected by setting $R'_{out} \ll R_{fb1} + R_{fb2}$. The solution of (2) is given as follows by first order approximation of Maclaurin's expansion and assuming as $T_{ON} \ll C_L R'_{out}$.

$$v_{out}(t) = \frac{R_{load}}{R_{out} + R_{load}} V_{DD} \left\{1 - e^{-\frac{t}{C_L R'_{out}}}\right\} + v_{out}(t=0) e^{-\frac{t}{C_L R'_{out}}} \simeq \frac{\frac{V_{DD} - v_{out}(t=0)}{R_{out}} - \frac{v_{out}(t=0)}{R_{load}}}{C_L} t + v_{out}(t=0) \tag{3}$$

In the discharging period ($T_{ON} \leqq t < T_{cycle}$), the PMOS switch turns off, and discharge operation occurs. To easily calculation, we assume as $t = T_{ON} \rightarrow t' = 0$. The behavior of $v_{out}(t)$ and its solution are given as (4) and (5) in the same way as before and assuming as $T_{OFF} \ll C_L R_{load}$.

$$0 = C_L R_{load} \frac{dv_{out}(t')}{dt'} + v_{out}(t') \tag{4}$$

$$v_{out}(t') = v_{out}(t'=0) e^{-\frac{t'}{C_L R_{load}}} \simeq -\frac{v_{out}(t'=0)}{C_L R_{load}} t' + v_{out}(t'=0) \tag{5}$$

Next, we discuss about the output ripple Δv_{out}, switching duty ratio and size of the output PMOS switch. The first terms of (3) and (5) mean the slew rate of charge and discharge, respectively. Where we assume approximately as $v_{out}(t=0) \simeq v_{out}(t'=0) \simeq V_{out}$ about these first terms, and we define as $I_{out} = (V_{DD} - V_{out})/R_{out}$ and $I_{load} = V_{out}/R_{load}$. Therefore, the behavior of $v_{out}(t)$ at one cycle operation is summarized as (6).

$$v_{out}(t) \simeq \begin{cases} +\frac{I_{out} - I_{load}}{C_L} t + v_{out}(0) = K_1 t + v_{out}(0) & (0 \leqq t < T_{ON}) \\ -\frac{I_{load}}{C_L}(t - T_{ON}) + v_{out}(T_{ON}) = K_2(t - T_{ON}) + v_{out}(T_{ON}) & (T_{ON} \leqq t < T_{cycle}) \end{cases} \tag{6}$$

where $K_1 = (I_{out} - I_{load})/C_L$ and $K_2 = -I_{load}/C_L$ are the charge and discharge slew rate, respectively. The output ripple voltage Δv_{out} of each cycle and the duty ratio D of the switching give following relations by focusing transient swing of $v_{out}(t)$.

$$\Delta v_{out} = K_1 T_{ON} = -K_2(T_{cycle} - T_{ON}) = -K_2 T_{OFF} \tag{7}$$

$$D = \frac{T_{ON}}{T_{cycle}} = \frac{-K_2}{K_1 - K_2} = \frac{I_{load}}{I_{out}} = \frac{I_{load}}{\frac{V_{DD} - V_{out}}{R_{out}}} \tag{8}$$

From (7) and (8), following relations are given.

$$\begin{cases} T_{ON} = DT_{cycle} \\ T_{OFF} = (1 - D)T_{cycle} \end{cases} \tag{9}$$

$$\Delta v_{out} = K_1 D T_{cycle} = -K_2(1 - D)T_{cycle} \tag{10}$$

Equation (8) can be rewritten as (11).

$$I_{out} = \frac{V_{DD} - V_{out}}{R_{out}} = \frac{I_{load}}{D} \tag{11}$$

The drain-source current of PMOS transistor in linear region is $I_{ds} = \mu C_{ox} K_p\{(V_{gs} - V_{th})V_{ds} - V_{ds}^2/2\}$, where μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, K_p is the aspect ratio $(= W/L)$ of the output PMOS switch. V_{gs}, V_{ds} and V_{th} are the gate-source voltage, the drain-source voltage and the threshold voltage, respectively. The current through the output PMOS switch is given as follows.

$$I_{out} = \mu C_{ox} K_p\{(V_{DD} - V_{th})(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}\} \tag{12}$$

From (11) and (12), K_p is given as follows.

$$K_p \geqq \frac{I_{load-max}}{\mu C_{ox}\{(V_{DD} - V_{th})(V_{DD} - V_{out}) - \frac{(V_{DD}-V_{out})^2}{2}\}D} \tag{13}$$

where $I_{load-max}$ is the required load current and $V_{DD} - V_{out}$ means the dropout voltage. The size of the output PMOS switch can design based on (13).

3.2. Derivation of Relationship between T_{cycle}, Δv_{out} and Circuit Parameters by Theoretical Transient Response Analysis

Next, the output voltage ripple Δv_{out} and the switching cycle T_{cycle} are analyzed in detail. T_{cycle} is determined by the delay time of the control logic T_{delay} and the response time of the comparator. The behavior of the comparator can be represented by the ramp response as shown in Figure 2 (c), where $V_{th-comp}$ is the threshold voltage of the ideal quantizer, and v_0 is the initial value of the input ramp waveform. When K is the slew rate of the input ramp waveform, the input voltage of the comparator can be given by $v_e(t) = Kt + v_0$. If the initial value of $v_{amp}(t)$ is defined as $v_{amp}(t = 0)$, the differential equation and the solution of $v_{amp}(t)$ are given as follows.

$$A_v(Kt + v_0) = CR\frac{dv_{amp}(t)}{dt} + v_{amp}(t) \tag{14}$$

$$v_{amp}(t) = A_v K\left\{t - CR(1 - e^{-\frac{t}{CR}})\right\} + A_v v_0(1 - e^{-\frac{t}{CR}}) + v_{amp}(t = 0)e^{-\frac{t}{CR}} \tag{15}$$

By using (15), the behavior of $v_{amp}(t)$ at one cycle shown in Figure 2(b) can be analyzed in detail. To easily calculation, we focus on the magnitude information, and define $D = 50\%$ and $V_{th-comp} = 0$. In this condition, the output voltages at the inflection points can be expressed as $v_{out}(t = 0) = V_{out} - \Delta v_{out}/2$ and $v_{out}(t = T_{ON}) = V_{out} + \Delta v_{out}/2$. T_1 and T_2 are the response time which $v_{amp}(t)$ reaches until $V_{th-comp}$ in on and off period, respectively.

$$\begin{cases} T_1 = T_{ON} - T_{delay} \\ T_2 = T_{OFF} - T_{delay} \end{cases} \tag{16}$$

A) Charging period $(0 \leqq t < T_{ON})$

In the charging period of $(0 \leqq t < T_1)$, the initial value of $v_e(t)$ is $v_1 = +\beta\Delta v_{out}/2$ in case of focusing on the magnitude information, and the final value of $v_{amp}(t)$ is $v_{amp}(t = T_1) = 0$. Using these conditions and Eq. (15), the following equation is given.

$$v_{amp}(t = 0) = \beta A_v\left[+\frac{\Delta v_{out}}{2}(1 - e^{+\frac{T_1}{CR}}) + K_1\left\{CR - (CR - T_1)e^{+\frac{T_1}{CR}}\right\}\right] \tag{17}$$

In the period of $(0 \leqq t < T_{ON})$, $v_{amp}(t = T_{ON})$ is given by using (15) and (17) as follows.

$$v_{amp}(t = T_{ON}) = \beta A_v\left[+\frac{\Delta v_{out}}{2}(1 - e^{-\frac{T_{delay}}{CR}}) + K_1\left\{(CR - T_{ON}) - (CR - T_1)e^{-\frac{T_{delay}}{CR}}\right\}\right] \tag{18}$$

B) Discharging period ($T_{ON} \leqq t < T_{cycle}$) To easily calculation, we define $t = T_{ON} \rightarrow t' = 0$ and $t = T_{cycle} \rightarrow t' = T_{OFF}$. In the period of ($0 \leqq t' < T_2$), the initial value of $v_e(t')$ is $v_2 = -\beta\Delta v_{out}/2$, and the final value of $v_{amp}(t')$ is $v_{amp}(t' = T_2) = 0$. Using these condition and (15), the following equation is given.

$$v_{amp}(t'=0) = \beta A_v \left[-\frac{\Delta v_{out}}{2}(1 - e^{+\frac{T_2}{CR}}) + K_2 \left\{ CR - (CR - T_2)e^{+\frac{T_2}{CR}} \right\} \right] \tag{19}$$

In the period of ($0 \leqq t' < T_{OFF}$), $v_{amp}(t' = T_{OFF})$ is given by using (15) and (19) as follows.

$$v_{amp}(t' = T_{OFF}) = \beta A_v \left[-\frac{\Delta v_{out}}{2}(1 - e^{-\frac{T_{delay}}{CR}}) + K_2 \left\{ (CR - T_{OFF}) - (CR - T_2)e^{-\frac{T_{delay}}{CR}} \right\} \right] \tag{20}$$

C) Derivation of T_{cycle} and Δv_{out}

As shown in Figure 2(b), since the initial and final values of $v_{amp}(t)$ in each period are equal, (21) and (22) are given.

$$v_{amp}(t=0) = v_{amp}(t' = T_{OFF}) \tag{21}$$

$$v_{amp}(t = T_{ON}) = v_{amp}(t'=0) \tag{22}$$

Equations (23) and (24) are derived from (17) to (22), respectively.

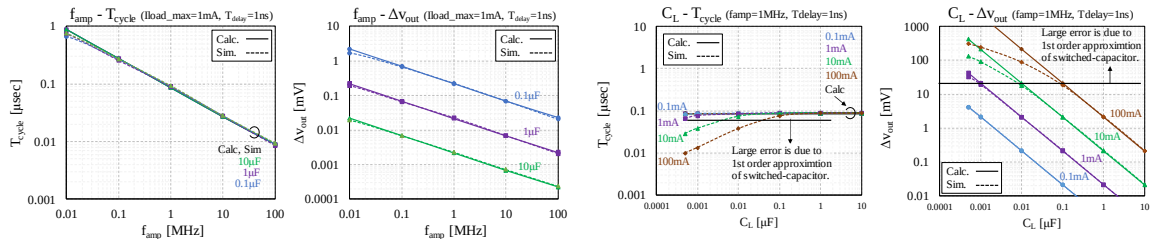
$$+\frac{\Delta v_{out}}{2}(1 - e^{+\frac{T_{ON}-T_{delay}}{CR}}) + K_1 \left\{ CR - (CR - T_{ON} + T_{delay})e^{+\frac{T_{ON}-T_{delay}}{CR}} \right\} = -\frac{\Delta v_{out}}{2}(1 - e^{-\frac{T_{delay}}{CR}}) + K_2 \left\{ (CR - T_{OFF}) - (CR - T_{OFF} + T_{delay})e^{-\frac{T_{delay}}{CR}} \right\} \tag{23}$$

$$-\frac{\Delta v_{out}}{2}(1 - e^{+\frac{T_{OFF}-T_{delay}}{CR}}) + K_2 \left\{ CR - (CR - T_{OFF} + T_{delay})e^{+\frac{T_{OFF}-T_{delay}}{CR}} \right\} = +\frac{\Delta v_{out}}{2}(1 - e^{-\frac{T_{delay}}{CR}}) + K_1 \left\{ (CR - T_{ON}) - (CR - T_{ON} + T_{delay})e^{-\frac{T_{delay}}{CR}} \right\} \tag{24}$$

From (9) and (10), (23) and (24) are the function of T_{cycle}. Since these equations are transcendental, they are difficult to solve algebraically. Therefore, we set $Error_1$ and $Error_2$ as the difference of both sides of (23) and (24), and numerically solve T_{cycle} from condition that $Error_1$ and $Error_2$ become zero. $Error_1$ and $Error_2$ are given as follows by using (23), (24), (9) and (10).

$$\begin{aligned} Error_1 = &+ \frac{K_1 DT_{cycle}}{2}(2 - e^{+\frac{DT_{cycle}-T_{delay}}{CR}} - e^{-\frac{T_{delay}}{CR}}) + K_1 \left\{ CR - (CR - DT_{cycle} + T_{delay})e^{+\frac{DT_{cycle}-T_{delay}}{CR}} \right\} \\ &- K_2 \left\{ (CR - (1-D)T_{cycle}) - (CR - (1-D)T_{cycle} + T_{delay})e^{-\frac{T_{delay}}{CR}} \right\} = 0 \end{aligned} \tag{25}$$

$$\begin{aligned} Error_2 = &- \frac{K_1 DT_{cycle}}{2}(2 - e^{+\frac{(1-D)T_{cycle}-T_{delay}}{CR}} - e^{-\frac{T_{delay}}{CR}}) + K_2 \left\{ CR - (CR - (1-D)T_{cycle} + T_{delay})e^{+\frac{(1-D)T_{cycle}-T_{delay}}{CR}} \right\} \\ &- K_1 \left\{ (CR - DT_{cycle}) - (CR - DT_{cycle} + T_{delay})e^{-\frac{T_{delay}}{CR}} \right\} = 0 \end{aligned} \tag{26}$$



(a) (b)

Figure 3. Verification results of T_{cycle} and Δv_{out} ($D = 50\%$). (a) f_{amp} dependence. (b) C_L and $I_{load-max}$ dependence.

Table 1. Component parameters for equivalent model verification.

Component name	(a) f_{amp} dependence	(b) C_L and $I_{load-max}$ dependence	Unit
$I_{load-max}$	1	0.1, 1, 10, 100	mA
V_{DD}	2	2	V
V_{ref}	0.5	0.5	V
A_v	1000	1000	-
$\beta = \frac{R_{fb1}}{R_{fb1}+R_{fb2}}$	$\frac{500\ kohm}{500\ kohm+1300\ kohm}$	$\frac{500\ kohm}{500\ kohm+1300\ kohm}$	-
V_{out}	1.8	1.8	V
R_{out}	200	2000, 200, 20, 2	ohm
D	50	50	%
C_L	0.1, 1, 10	0.0005, 0.001, 0.01, 0.1, 1, 10	μF
$f_{amp} = \frac{1}{2\pi CR}$ @	0.001, 0.01, 0.1, 1, 10, 100	1	MHz
T_{delay}	1	1	nsec

Equations (25) and (26) are complicated, but they can be easily solved by using the spreadsheet software. Here, (25) and (26) derive same solution T_{cycle} on the condition of $D = 50\%$. The dependence analysis of the various circuit parameters by using (25) and (10) are shown as follows. Figure 3 shows the comparison between calculated and simulated (by using circuit model shown in Figure 2(a)) values of T_{cycle} and Δv_{out} under the conditions shown in Table 1. Where $f_{amp} = 1/(2\pi CR)$ is the cut-off frequency of the amplification stage of the comparator. From Figure 3(a), we can confirm that T_{cycle} and Δv_{out} depend on f_{amp} (also depend on T_{delay}, but it isn't shown), and Δv_{out} can reduce by adjusting larger f_{amp} and selecting larger C_L. f_{amp} can adjust by the bias current of the comparator, and T_{delay} should be designed to minimize the number of gate stages of the logic circuit. To minimize Δv_{out}, f_{amp} should be high (T_{cycle} should be small), it causes increase of the bias current of the comparator and the switching current. Therefore, Δv_{out} has trade-off with current consumption.

From Figure 3 (b), we can confirm that Δv_{out} depends on C_L and $I_{load-max}$. We can find the differences between calculation and simulation results when C_L and $I_{load-max}$ are small and large, respectively. These differences are caused by the first order approximation as mentioned in derivation of (3) and (5). However, our design target is smaller range of $I_{load-max}$ and Δv_{out}. Thus, we can estimate circuit characteristics with good accuracy by using derived equations. T_{cycle} is not affected C_L and $I_{load-max}$, and Δv_{out} strongly depends on C_L and $I_{load-max}$. In the practical design, C_L and $I_{load-max}$ are given by the target specification. Therefore, we should design Δv_{out} by adjusting f_{amp}.

3.3. Current Consumption

The average current consumption of the proposed circuit is sum of three components which are the static bias current of the comparator I_{comp}, the current of the feedback resistor I_{fb} and the average switching current of the switching parts I_{sw}.

$$I_{DD} = I_{comp} + I_{fb} + I_{sw} = I_{comp} + \frac{V_{ref}}{R_{fb1}} + \sum_i \frac{C_i V_{DD}^2}{T_{cycle}} \tag{27}$$

where, C_i is the capacitance of each switching node in logic circuit and the gate capacitance of the output PMOS switch.

3.4. Design Guideline of the Proposed LDO

From previous discussion, we showed that the circuit characteristics of the proposed LDO can be clarified by mathematical analysis. Therefore, we can define design guideline and estimate performance of the proposed circuit. Firstly, the size of output PMOS switch is designed by using (13). Secondly, in order to achieve the required Δv_{out}, the relationship between T_{cycle}, Δv_{out} and circuit parameters is estimated by (25) or (26). Next, f_{amp} is estimated by the necessary response time of the comparator, which can be tuned by adjusting the tail current of the comparator. The design flow is shown in Figure 4.

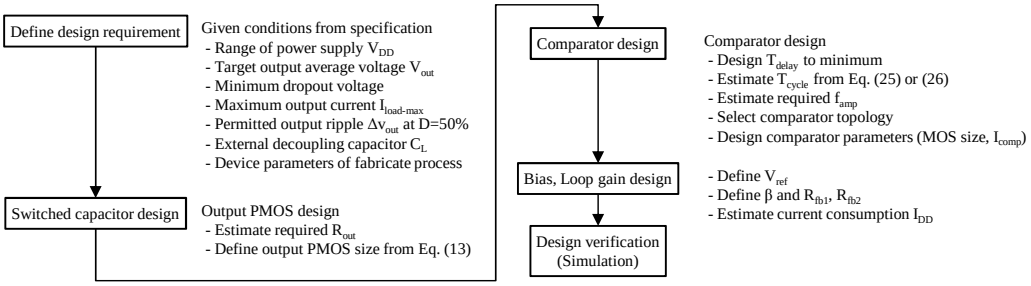


Figure 4. Design flow of proposed LDO.

4. CIRCUIT IMPLEMENTATION

The complete schematic of the proposed regulator and evaluated test bench are shown in Figure 5 (a). The circuit surrounded by blue dot line is proposed LDO. In this study, we implemented two functions that two selectors for the output current ability (OUTSEL[1:0]) and power mode (PMSEL). The function tables for selectors are shown in bottom left of Figure 5 (a). The output current ability selector selects the number of active PMOS switches (M_{P0} - M_{P3}). This function can be used to change the output current ability by selecting the number of parallel connection of PMOS switches. The implementation of the automatic adjustment of this function is future work. The power mode selector is implemented to select low power mode (PMSEL=$(0)_2$) or low ripple mode (PMSEL=$(1)_2$) depending on the required operation mode. In detail, it adjusts the tail current of the comparator $I_{TAILCOMP}$. If the required noise specification of the load circuit of LDO is severely, then the operation mode will be set to the low ripple mode and LDO operates on smaller output ripple. We consider the parasitic impedance (inductance L_P and resistance R_P) model like as package and socket surrounded by green dot line in Figure 5 (a) for estimating practical characteristics. The circuits surrounded by red dot line is the bio-medical AFE which consists of IA and LPF to evaluate for influence of LDO output ripple. IA architecture consists of Fully Balanced Differential Difference Amplifier (FBDDA) and Differential Difference Amplifier (DDA) proposed in [3]. The LPF is 3rd-order gm-C LPF based on standard PMOS differential amplifiers. The input signal V_{IN} is sinusoidal wave which is magnitude of 10 μV_{pp} and frequency of 500 Hz. The external output capacitive load (10 pF) of AFE is equivalent input capacitance of the oscilloscope. Figure 5 (b) shows the schematic of comparator. We selected PMOS input differential pair and low input reference voltage V_{ref} for lower supply voltage operation. The negative resistance circuit in the comparator is implemented to enhance the transient response on reasonable lower bias current.

The feasibility design specifications and component parameters of LDO are listed in Table 2 and 3, respectively. In this study, we use 1P 2M 0.6 μm CMOS process for evaluation of combination with our existing AFE circuits [3]. The output PMOS switch is sized with a suitable margin for process, voltage, and temperature (PVT) variations by using (13). The default value of OUTSEL[1:0] is $(11)_2$ in this design. R_{fb1} and R_{fb2} are selected large value for reducing static current consumption. As mentioned previously, Δv_{out} can be designed by adjusting f_{amp}, it means that the tail current of the comparator $I_{TAILCOMP}$ should be selected by considering the device performance of MOS transistors. From the specification of test design, the tail currents of low power and low ripple mode are respectively set 0.25 μA and 2.25 μA in order to consider reasonable performance and power consumption. When the operation mode changed to low ripple mode, the output ripple voltage reduced to about 1 mV instead of consuming large quiescent current. The layout diagram is shown in Figure 5 (c). From this layout diagram, the circuit area is about 0.0173 mm^2 in spite of using 0.6 μm design rules.

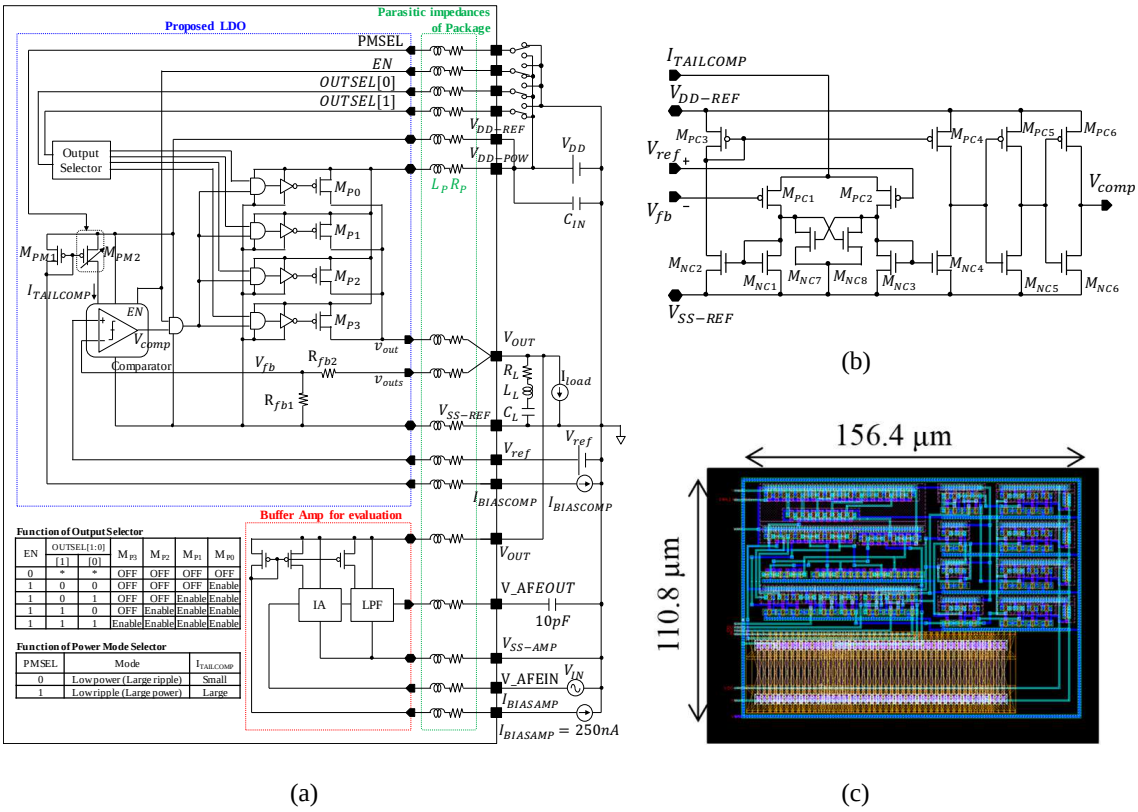


Figure 5. Designed circuit, simulated test bench and layout. (a) Overview of circuit and test bench. (b) Schematic of comparator. (c) Layout diagram of LDO.

Table 2. Design specifications of test design.

Circuit	Item	value
LDO	CMOS Process	1P 2M 0.6 μm CMOS
	Temperature range	–20 to 95 °C
	Power supply V_{DD}	1.9 V - 2.2 V
	Output voltage V_{out}	1.8 V
	Minimum dropout voltage $V_{do_{min}}$	0.1 V
	Maximum load current $I_{load-max}$	50 μA
	External decoupling capacitor C_L	0.1 μF
	Permitted output ripple voltage	$\leq$ 10 mV (I_{load} = 5 μA - 50 μA)
	Permitted output ripple frequency	$\gg$ 10 kHz (I_{load} = 5 μA - 50 μA)
AFE	Power supply voltage	1.8 V
	Power supply current	10 μA - 20 μA
	Minimum input signal magnitude	10 μVpp
	Input signal frequency range	$\leq$ 1 kHz
	Total gain	68 dB
	LPF cutoff frequency	2 kHz
	PSRR	$\leq$ -60 dB ($\geq$ 10 kHz)

Table 3. Component parameters of LDO.

Component name	Size / value	Component name	Size / value
$M_{P0} - M_{P3}$	6 μm / 0.6 μm, m=1	R_{fb1}	1 Mohm
PMOS of inverters	2.4 μm / 0.6 μm, m=1	R_{fb2}	2.6 Mohm
NMOS of inverters	1.2 μm / 0.6 μm, m=1	C_{IN}	0.1 μF
PMOS of NANDs	2.4 μm / 0.6 μm, m=1	C_L	0.1 μF
NMOS of NANDs	2.4 μm / 0.6 μm, m=1	R_L	10 mohm
M_{PM1}	2.4 μm / 0.6 μm, m=2	L_L	100 pH
M_{PM2}	2.4 μm / 0.6 μm, m=2 or 18	R_P	100 mohm
$M_{PC1} - M_{PC4}$	2.4 μm / 0.6 μm, m=4	L_P	2 nH
$M_{PC5} - M_{PC6}$	2.4 μm / 0.6 μm, m=1	V_{ref}	0.5 V
$M_{NC1} - M_{NC4}$	1.2 μm / 0.6 μm, m=4	$I_{BIASCOMP}$	250 nA
$M_{NC5} - M_{NC6}$	1.2 μm / 0.6 μm, m=1		
$M_{NC7} - M_{NC8}$	1.2 μm / 0.6 μm, m=3		

5. SIMULATION RESULTS

The proposed circuit has been evaluated by using SPICE simulator with 1P 2M 0.6 μm CMOS process device parameters. The nominal conditions are $V_{DD} = 2.0\ V$, 27 °C and OUTSEL[1:0]=$(11)_2$ and PMSEL=$(0)_2$.

Figure 6 shows the typical waveforms when the load current is changed from 10 μA to 50 μA, and the operation mode is also changed from low power mode to low ripple mode at 0.6 msec simultaneously. The output waveform shows no ringing and overshoots other than the switching ripple. The offset voltage of V_{out} between two modes is enough small as 3.5 mV. Figure 7 shows the load regulation and power supply voltage dependence at nominal condition. From Figure 7 (a), the load regulation is less than 1 mV under the condition that the range of I_{load} is 0 μA to 50 μA. The line regulation is about 10.3 mV/V (0.57 %/V) under the condition that I_{load} is 50 μA and V_{DD} is from 1.9 V to 2.2 V. The quiescent current I_{DD} is about 1 μA from Figure 7 (b). We can also confirm that the maximum Δv_{out} and minimum F_{cycle} (=1/T_{cycle}) are 5.2 mV and 19 kHz, respectively from Figures 7 (c) and (d). From Figure 7 (e), we could confirm that the duty ratio increases with increasing of I_{load}. The current efficiency is also increase with increasing of I_{load} from Figure 7(f). The PVT variations of fundamental performances are shown in Figures 8(a) to (f). The evaluated corner conditions are TT (typical NMOS and PMOS), SS (slow NMOS and slow PMOS) and FF (fast NMOS and fast PMOS). V_{DD} and temperature ranges are from 1.9 V to 2.2 V and from –20 °C to 95 °C, respectively. This results show reasonable performance with satisfying the design specification shown in Table 2. Figure 8 depicts PVT variation of load regulation and supply voltage dependence.

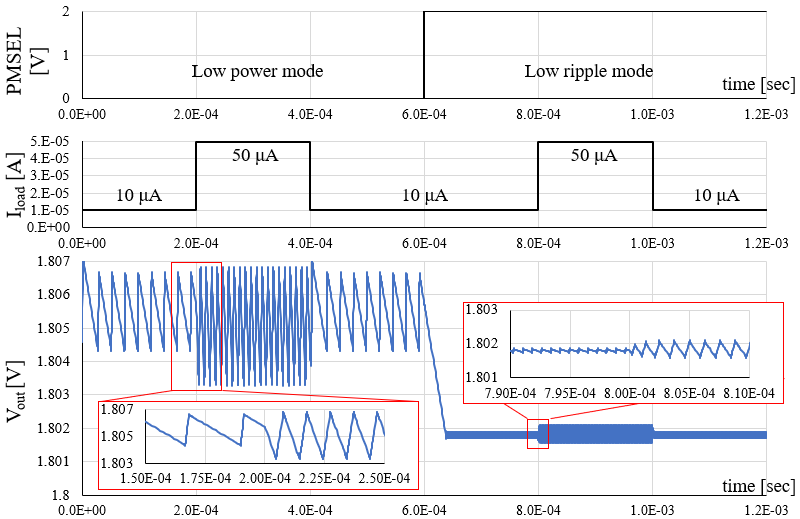


Figure 6. Typical transient waveform.

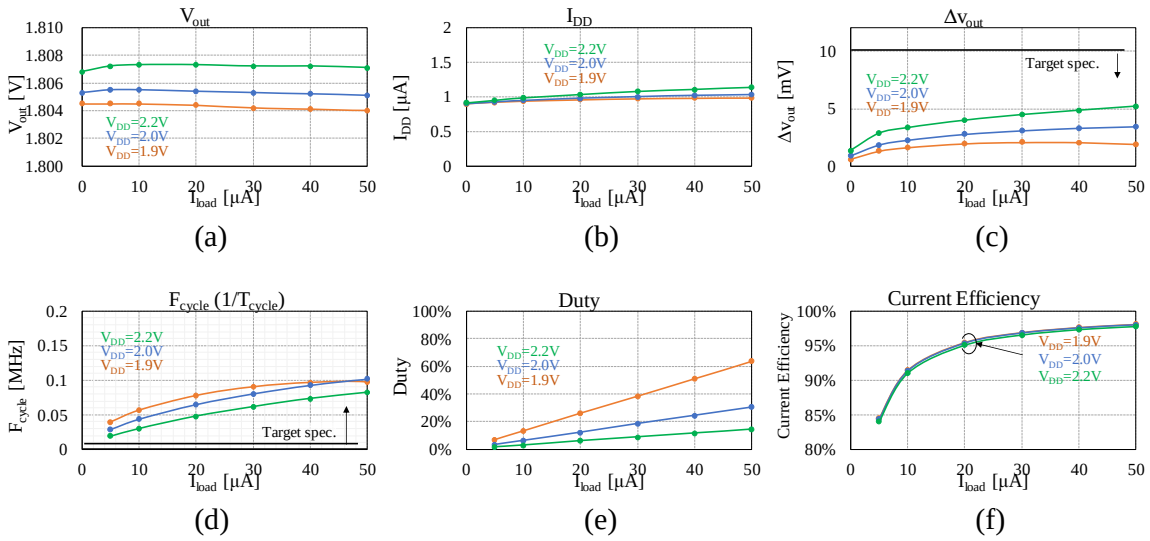


Figure 7. Load regulation and supply voltage dependence in typical condition.

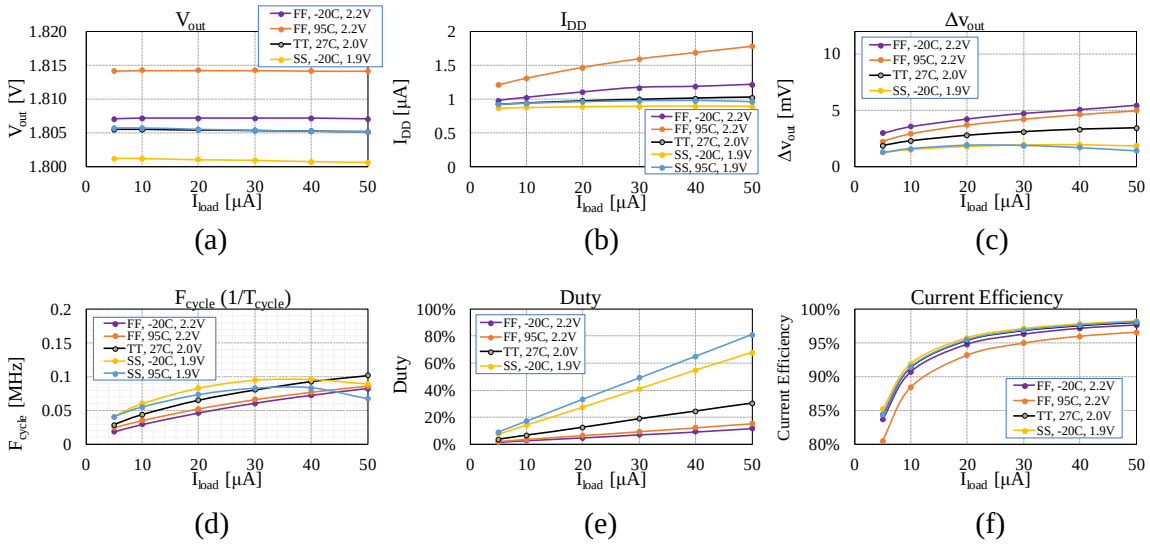


Figure 8. PVT variation of load regulation and supply voltage dependence.

The startup waveform with the PVT variations are shown in Figure 9 (a). The load condition is I_{load}=50 μA (R_{load}=36kohm). From this result, we confirm that the proposed LDO operates properly without ringing and over/undershoot. Figure 9 (b) shows the PSRR characteristics of LDO under the condition that V_{DD} is 2.0 V and magnitude of power supply noise is 30 mV_{pp}. The PSRR in low frequency is about –40 dB. The peak PSRR in high frequency band depends on the output voltage ripple at the switching frequency F_{cycle}. However, it does not matter because its high frequency noise will be attenuated by LPF of AFE as described later.

Figure 10 shows the characteristic comparison of low power and low ripple mode. When the operation mode is switched to low ripple mode, Δv_{out} is effectively reduced as shown in Figure 10 (a), whereas the current efficiency is worse as depicted in Figure 10 (b). This phenomena has been clarified by mathematical analysis in section 2 and we could confirm the trade off between Δv_{out} and I_{DD}.

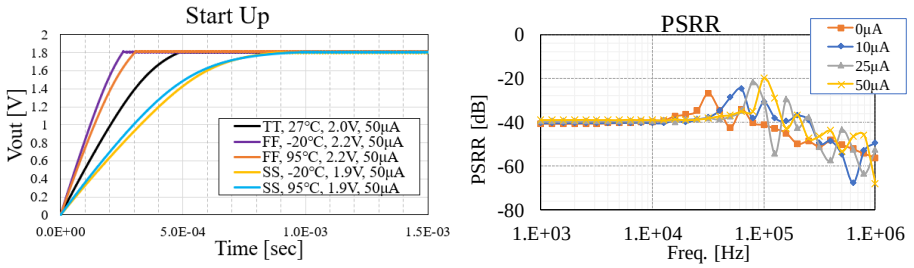


Figure 9. Startup waveforms and PSRR characteristics.

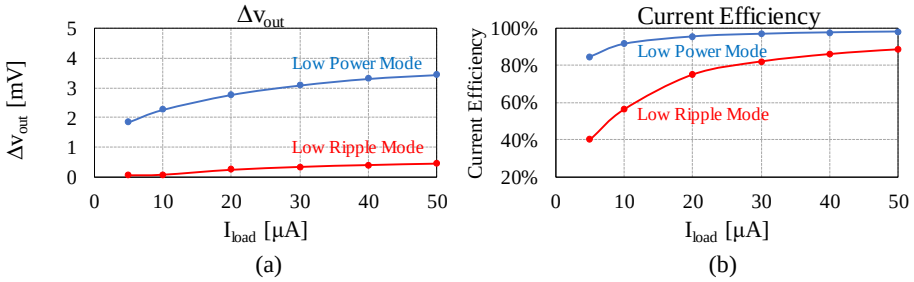


Figure 10. Characteristic comparison of low power and low ripple mode.

Figure 11 shows the characteristics when the proposed LDO is applied to AFE. Figure 11 (a) shows the transfer gain and PSRR of AFE. Since the transfer gain reaches lower than 0 dB at over 20 kHz and PSRR is lower than –60 dB, the high frequency ripple noise of LDO will be expected to attenuate effectively. The monitoring evaluation of AFE is simulated. Figure 11 (b) shows the FFT analysis of Vout, V_AFEIN and V_AFEOUT shown in Figure 5 (a). We could confirm that the high frequency ripple of LDO does not affect to performance of AFE.

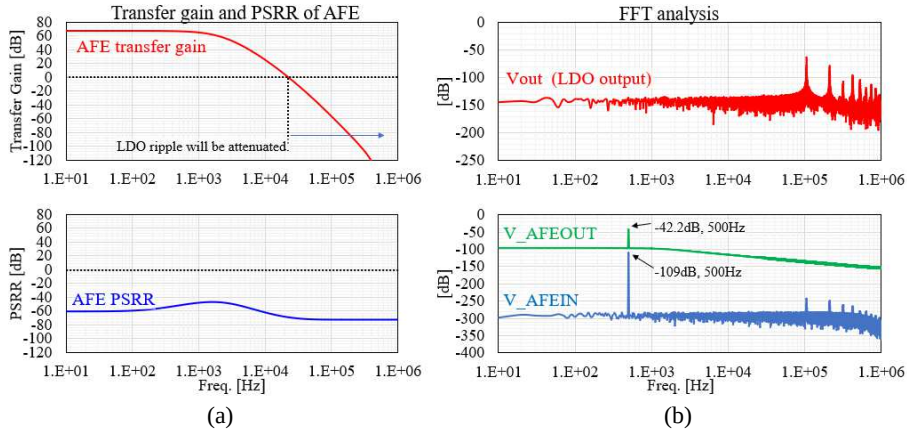


Figure 11. AFE characteristics applying the LDO as power supply. (a) Transfer gain and PSRR of AFE. (b) FFT analysis result of AFE.

A detailed comparison of the proposed circuit with the regulators presented in the past is listed in Table 4. Two kinds of design examples of the proposed LDO are shown. In order to compare with various prior circuits under the same condition, we use two kinds of figure of merit (FoM).

$$FoM_1 = Area \times \frac{\Delta v_{out}}{C_L} \tag{28}$$

$$FoM_2 = Area \times \frac{\Delta v_{out}}{C_L} \times \frac{I_{DD}}{I_{lout-max}} \tag{29}$$

FoM_1 is proposed in [15]. FoM_2 is used to compare for considering the current efficiency aspect. Although the appropriate application of the proposed LDO is low load current and low frequency circuit, FoMs of the proposed LDO is enough reasonable. In addition, since the circuit and design procedure of the proposed LDO is very simple, we can reuse the identical circuit topology to across multiple fabrication process.

Table 4. Comparison of LDO regulators.

	Units	[8]	[9]	[11]	[12]	[14]	[15]	This work	
Technology	μm	0.35	0.13	0.065	0.065	0.18	0.13	0.6	
Control		Analog	Analog	Digital	Digital	Analog assisted Digital	On-off	On-off	
Clock frequency	MHz	-	-	1	50	1	Self oscillation	Self oscillation	
Power supply voltage V_{DD}	V	1.05 to 3.5	1.9 to 3.6	0.5 to 1.2	0.6 to 1.1	1.2	1.9 to 3.3	1.9 to 2.2	
Output average voltage V_{out}	V	0.9	1.52	0.35 to 0.45	0.4 to 1.0	0.95	1.8	1.8	
Temperature range	°C	N/A	N/A	N/A	N/A	N/A	N/A	–20 to 95	
Output decoupling capacitor C_L	μF	1	0.003	0.1	0.001	0.01	0.2	0.1	1
Maximum output current $I_{out-max}$	mA	50	0.08	0.2	100	11	0.1	0.05	1
Quiescent current I_{DD}	μA	4.04 to 164	0.65	2.7	60	14.2 to 242	0.98 to 12.5	0.90 to 1.14	0.96 to 1.35
Current efficiency	%	99.67	99.2	98.7	99.9	93.3 to 99.6	N/A	97.7	99.9
Line Regulation	mV/V	1.061	1.4	3.1	3	15	36	10.3	12
Load Regulation	mV/mA	0.0614	0.01	0.65	0.06	0.63	50	11.1	1.11
Vout ripple voltage	mV	-	27	3	3	6 to 13	47	5.2	8.12
Area	mm^2	0.053	0.016	0.72	0.01	0.036	0.001225	0.0173	0.0200
FoM_1		0.35	144.00	21.60	30.00	46.80	0.29	0.90	0.16
FoM_2		1.147	1170.0	291.60	18.0	1029.60	35.98	21.55	0.22

6. CONCLUSION

In this paper, we have proposed the switching operation based LDO. Its design procedure has been clarified by mathematical analysis. This proposed circuit has been designed and simulated using 1P 2M 0.6 μm CMOS process device parameters. From the simulation results, we confirmed that the proposed circuit is suitable for light load current and low frequency signal application like as bio-medical AFE. The implementation of the automatic output current ability control function using digitally control is future work.

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BIOGRAPHY OF AUTHORS

Kenya Kondo was born in Miyazaki, Japan, on February 11, 1979. He received the B.E. and M.E. degrees from the Faculty of Engineering, University of Miyazaki, Miyazaki, Japan, in 2001 and 2003, respectively. He joined in ROHM Co., Ltd., from 2003 to 2005, where he worked for the power management LSI development. He moved and is currently working as an analog design engineer in Sony LSI Design Inc since 2006. And he is currently working toward the Ph.d. degree in University of Miyazaki.

Hiroki Tamura received the B.E and M.E degree from Miyazaki University in 1998 and 2000, respectively. From 2000 to 2001, He was an Engineer in Asahi Kasei Corporation, Japan. In 2001, He joined Toyama University, Toyama, Japan, where He was a Technical Official in Department of Intellectual Information Systems. In 2006, He joined Miyazaki University, Miyazaki, Japan, where He was an Assistant Professor in Department of Electrical and Electronic Engineering. In 2012, He is currently a Professor in the Department of Environmental Robotics. His main research interests are Neural Networks and Optimization Problems. In recent years, He has the interest in Biomedical Signal Processing using Soft Computing.

Koichi Tanno was born in Miyazaki, Japan, on April 22, 1967. He received B. E. and M. E. degrees from the Faculty of Engineering, University of Miyazaki, Miyazaki, Japan, in 1990 and 1992, respectively, and Dr. Eng. degree from Graduate School of Science and Technology, Kumamoto University, Kumamoto, Japan, in 1999. From 1992 to 1993, he joined the Microelectronics Products Development Laboratory, Hitachi, Ltd., Yokohama, Japan. He was engaged in research on low-voltage and low-power equalizer for read channel LSI of hard disk drives. In 1994, he joined University of Miyazaki, where he is currently a Professor in the Department of Electrical and Systems Engineering. His main research interests are in analog integrated circuit design and multiple-valued logic circuit design. Dr. Tanno is a member of IEEE.