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CMOS ring oscillator delay cell performance: a comparative study

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ABSTRACT

A common voltage-controlled oscillator (VCO) architecture used in the phase locked loop (PLL) is the ring oscillator (RO). RO consist of number of inverters cascaded together as the input of the first stage connected to the output of the last stage. It is important to design the RO to be work at desired frequency depend on application with low power consumption. This paper presents a review the performance evaluation of different delay cell topologies the implemented in the ring oscillator. The various topologies analyzed includes current starved delay cell, differential delay cell and current follower cell. Performance evaluation includes frequency range, frequency stability, phase noise and power consumption had been reviewed and comparison of different topologies has been discussed. It is observed that starved current delay cell have lower power consumption and the different of the frequency range is small as compared to other type of delay cell.

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1. INTRODUCTION

Basically, oscillator is a frequency translation that translate information signal with time reference. There is variation of oscillator with different principle operation, frequency oscillation and its noise performance. For instant, voltage-controlled oscillator (VCO) is one type of oscillator that output oscillation frequency can be varied by varying the amplitude of its input signal. There are two architectures of VCO namely; the ring oscillator and the LC oscillator.

Ring oscillator is widely used in the communication system design especially in the wireless ssystem [1]–[5] and FPGA application [6], [7] because of its wide tuning range, making them more robust over process and temperature variations. It also use used to study the degradation of logic CMOS circuit [8], [9]. Many trade-offs in terms of speed, power, area and application domain need to be considered in designing a ring oscillator. Thus, it is important to determine accurate frequency oscillation of the ring oscillator so that the designer able to make informed decisions regarding these trade-offs.

This paper is organized as follows. Section 2 discuss the basic concept of ring oscillator and the equations related to oscillation frequency that have been derived in previous works. In Section 3 investigates the available delay topologies used ring oscillator. Section 4 compares the performance and discuss the advantage and disadvantages of each topology. Section 5 presents our conclusions.

2. BASIC CONCEPT OF RING OSCILLATOR

Basically, ring oscillator is comprised of an odd number of NOT gates whose output oscillates between two voltage levels, representing '1' and '0'. The NOT gate is cascade in chain where the output of the last stage fed back to the input of the first. The oscillation can be achieved when circuit provide phase shift of 2π and unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages[10]. The remaining π phase shift is provided by a DC inversion. The most basic ring oscillator is simply a chain of single ended digital inverters because they have better thermal noise performance than their differential CMOS counterparts and can achieve better phase-noise performance for a given power dissipation [11], [12].

Figure 1 shows a block diagram of 5 stage ring oscillator that constructed by 5 inverters. In this ring oscillator, the output of each inverter is used as input for the next one and the last output is fed back to the input of the first inverter. Ring oscillator is commonly used in the process technology development to characterize the process performance[6], [8], [13], [14]. It also widely uses as clock generator, voltage controlled oscillator [15]–[18] and phase locked loop [19], [20].

First, let the output of the first inverter is a low indicate by '0' and its transfer the signal to the input of the second inverter. We know that an inverter will invert the input signal that pass through it. So, the second inverter's output must switch to a high condition indicates as '1'. This is how the oscillator oscillate its signal through the N number of stages implies in the circuit. The output of last inverter will transfer its signal to the input of the first inverter. This process will repeat indefinitely, resulting in the voltage at each node oscillating.

One of the important parameter of the ring oscillator is its oscillation frequency (f_{osc}) that depends on the number of stages (n) and the delay time (t_d) of each stage as expressed in (1) [10], [18], [21]. The oscillation frequency depends on the delay time of each stage consider the propagation delay for both transition low-to-high (t_{pLH}) and high-to-low (t_{pHL}). The delay occurs due to the time taken by the transistor gate capacitance to charge before current can flow from source to drain. Thus, the output of every unit changes after a certain amount of time after the input has changed. As the number of stages increase the total delay increases and hence the output frequency decreases. When all the individual units are made up of identical circuits, the delay due to one unit can be calculated by dividing the total delay with the number of stages.

$$f_{OSC} = \frac{1}{2\pi t_d} \quad (1)$$

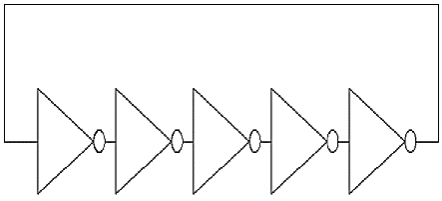

Figure 1. The block diagram of five stage ring oscillator [17], [22]

3. TYPE OF DELAY CELL IN RING OSCILLATOR

3.1. Current starved delay cell based voltage controlled ring oscillator

In real time, the supply voltage, VDD of a ring oscillator circuit varies and the voltage variation produce an output frequency variation. Thus, current is needed to be supply at each inverter to ensure the output frequency is stable. This can be done by using current starved inverter as shown in Figure 2, whereby it controls the amount of current to charge and discharge the capacitive load each stage. M1 and M2 operates as current source that limits the current through M3 and M4. M3 and M4 is an inverter and now it is said starved for current. The input control voltage controls the current of M5 and M6 and the values are mirrored in each inverter or current source voltage.

Figure 3 shows a current starved delay cell implemented in the voltage-controlled ring oscillator. It consists of five stages of ring oscillator whereby NMOS transistor work as current sources and the two PMOS transistor used in the delay cell. A current limiter circuit denotes by M1 and M13 is required in this type of structure such that it can limit the current through PMOS inverter. The tuning range of the circuit is

improved, the frequency linearity is increases and the power consumption is reduced when implementing this delay cell [22].

Besides, Niko and Adrijan had implemented current starved delay five stage current starved ring oscillator [23] as shown in Figure 4. The current variation in this circuit is almost zero when $V_{RF}=V_{FVC}$ and thus the oscillation frequency is stable and independent of current variation. In this circuit, the current I_{osc} is never be zero to ensure the safe starts and the frequency of the oscillator is depending on the current value. Thus, this delay cell independent of the current variation and it is temperature dependent.

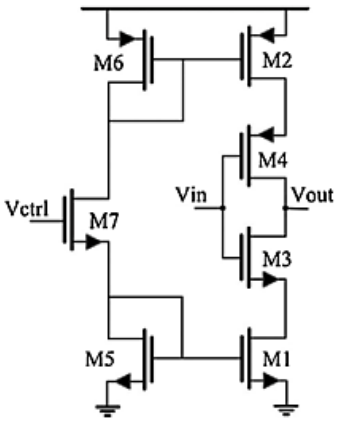

Figure 2. The current starved inverter [18], [24]

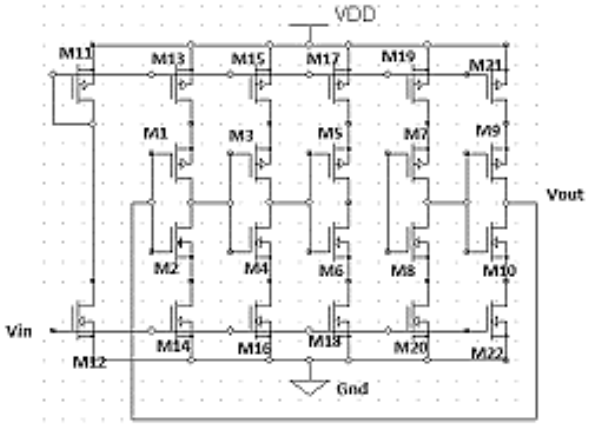

Figure 3. The schematic current starved delay cell based voltage controlled ring oscillator [22]

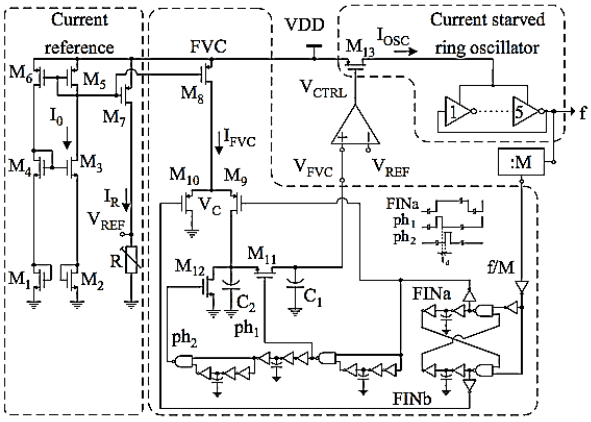

Figure 4. Circuit level Implementation of current staved ring oscillator based on the feedback loop architecture [23]

3.2 Differential delay cell

Another famous topology is the differential delay cell as illustrates in Figure 5. Basically, there are 2 delay paths in this circuit. The normal delay path, the differential output delay stage connects to the input of the next stage of the primary loop. Meanwhile, the skewed delay path is connected to secondary loop input of the next-second stage. This skewed delay path reduces delay time and phase noise of the circuit [23]. This type of delay cell preserves the high speed and low noise performance [25]. A differential four stage dual delay-path ring oscillated had been presented in [26] with two stable operation mode. The use of differential inverter delay stages has advantages over the use of single-ended delay stages, primarily because there is little distortion in the output [27].

The parameters that affect the frequency oscillation is given by (2). By varying tail current in delay stage, I_{SS} and peak-to-peak amplitude of the voltage waveform, V_{SW} the oscillation frequency is voltage controlled with constant load capacitance, C_L, number of stages, *n*, and delay of each stage in the ring oscillator, *t*. To the first order, V_{SW} increases as the I_{SS} increases and the frequency remains constant. Also,

it is often desirable to maintain a constant voltage swing during operation because if the swing is small, it increases the jitter, and if the swings are large, a higher supply voltage is needed for differential operation.

$$f_{osc} = \frac{I_{SS}}{2ntC_L V_{SW}} \quad (2)$$

It is reported that the ring oscillators based on a differential delay stage are very popular due to their immunity to disturbances on the supply line [28]. The phase noise of the differential ring oscillator has been investigated in [23], [29]-[32]. However, as technology scales, the timing jitter effect will become prominent because the transistor operate between saturation and triode mode and not taken into consideration in [23], [29].

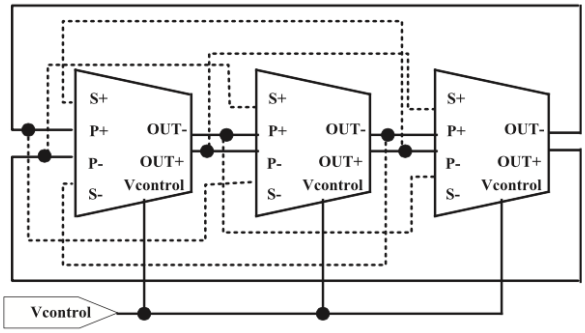

Figure 5. Multiple-pass loop structure of three stage ring oscillator with differential delay [25]

3.3 Source follower delay cell

The frequency of the ring oscillator depends on the device parameter and its voltage supply. As we know that the ring oscillator that implemented in the digital circuit application require high speed logic switching. Thus, noise on the voltage supply line need to take into consideration in designing the ring oscillator. A source follower delay cell proposed to reject the supply even without calibration or other additional regulation as shown in Figure 6 [33]. This delay cell isolates the supply through the transistor output resistance and reduce supply sensitivity. Supply isolation is provided by the primary source follower path through M1 meanwhile voltage gain is provided by inverting-latch secondary path through M2. It is necessary to sustain oscillation forcing complementary node to be out of 180^0 out of phase. By adjusting differential tuning voltage, the frequency is controlled by the phase-shift/bias network.

Power dissipation increases when using low-dropout regulator due to the higher supply voltage and extra circuitry. In [34], both power and ground noises are isolated by using a differential supply-regulated tuning technique. Another method uses a source follower to couple the control voltage directly to a differential pair in place of a DC current source, which makes the biasing less robust.

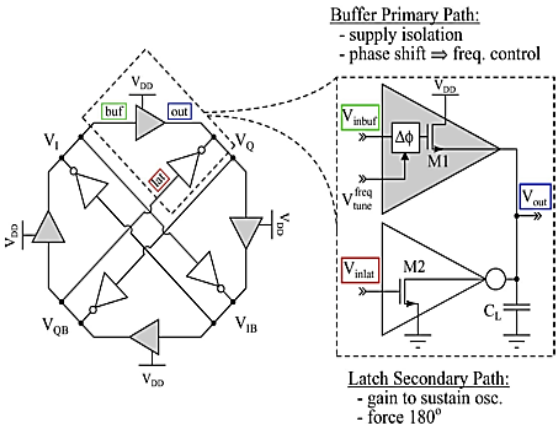

Figure 6. A conceptual block diagram of ring oscillator with source follower delay cell [35]

4. COMPARISON STUDY OF EACH TOPOLOGY

It is reported that the current starved gives better frequency linearity [36] and the oscillation of the frequency is device parameter and process dependent [22]. However, the oscillator does not require a stable current to obtain frequency that independent of voltage and temperature variation [37] due to the negative feedback in the oscillator. The power consumption is a bit higher as reported in [22] and to minimize the power consumption of the oscillator, the number of stages N, supply voltage V_{dd} and tail current I_{tail} should all be minimized [2], [37], [33], [34]. The current starved voltage-controlled oscillator improved jitter by adding D flip flop in the circuit [36]. A jitter is a variation of the reference signal with respect to ideal position in time and the impacts the data transmission quality [2].

In order to achieve better control voltage and frequency range for low voltage and wide tuning range voltage-controlled ring oscillator a new differential delay cell with complementary current control has been developed in [25]. Higher control voltage increases the current of each stage and decreases the delay time of each stage, and thus, increases the oscillation frequency [31], [38]. The differential delay cell able to reduce flicker noise contribution to the phase noise in the ring oscillator circuit by maximizing the number of stage [39] and thus channel length of the device need to be reduce. This lead to higher leakage current due to the short channel effect occur in the device. This problem can be reduced by using different type of device technology. A work presented in [40] proposed Double-gate (DG) FinFETs, the second gate is added opposite the traditional (first) gate, which have been recognized for their potential to better control short-channel effects (SCE) and as well as to control leakage current.

Basically, in this paper three type of delay cells implemented in the ring oscillator circuit is discussed in the Section III. The performance of the ring oscillator can be evaluated by measuring its oscillation frequency or frequency range, phase noise and power dissipation. A comparison parameters of different delay cell for ring oscillator is tabulated in Table 1. Each delay cell implemented in the ring oscillator has their own advantages and disadvantage thus it is important to know what the purpose and goal is in designing the circuits. From Table 1 it can be concluded that current starved delay cell is preferable to be use in the ring oscillator circuit due to its low power consumption compare to differential delay cell.

Table 1. Parameter Comparison Based On the Type of Delay Circuit Implemented in Ring Oscillator

Delay Circuit Type	Current Starved Delay				Differential Delay Cell					Source Follower delay cell
Year [publication]	2015 [22]	2013 [37]	2013 [36].	2012 [41]	2012 [39]	2012 [4]	2011 [26]	2011 [25]	2009 [42]	2012 [35]
Technology (nm)	180	180	180	180	350	180	180	180	130	90
Number of Stages	5	5	3	3	3		4	3	2	-
Supply Voltage (v)	2.5	1.2	1.8	1.8	3	1.8	-	1	1.3	-
Oscillation Frequency (mhz)	-	-	-	100 & 150	-	-	-	-	-	-
Frequency Range (ghz)	0.00132 – 0.00326	0.00384 – 0.00380	0.53 – 2.348	-	-	-	-	-	-	-
Tuning Range (ghz)	69.11	-	-	-	-	3.125 - 5.26	1.77 - 1.92	0.479 - 4.09	1.82 – 10.18	0.63 – 8.1
Phase Noise	-	-	-	-	0.076 Magnitude or -11.19 dB	-	−102 dBc/Hz @ 1 MHz, −123.4 dBc/Hz @ 10 MHz	−93 dBc/Hz @ 1 MHz	−121.7 dBc/Hz @ 5.6-GHz	-106 to -88 dBc/Hz at 10-MHz
Power (mw)	0.0042	0.0051	0.848	0.437 & 0.537	-	0.621	~ 13	13	5	7 - 26
Area (mm^2)	-	0.009	-	-	-	-	0.002214	0.0080772	-	-

5. CONCLUSION

This paper presented a comparative study of delay cell in the ring oscillator includes starved current delay cell, differential delay cell and current follower cell. The discussions are based on the design parameters and technology process variation in the recent research of ring oscillator for low voltage application. In conclusion, it is observed that starved current delay cell have lower power consumption and the different of the frequency range is small compared to other two type of delay cell as presented in Table 1. This type of delay cell can be implemented in 0.18 μm CMOS technology.

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