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Small-signal modeling of current-mode controlled modular DC-DC converters using the state-space algebraic approach

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ABSTRACT

Small-signal models are useful tools to preliminary understand the dynamics of interconnected systems like modular dc-dc converters which find a wide range of industrial applications. This work proposes a state-space-based averaged small-signal model in symbolic form for a peak current-mode controlled parallel-input/parallel-output buck converter operating in the continuous-conduction mode. In modeling the converter power-stage each module is independently represented. For modeling the current-mode control the state-space algebraic approach is used to incorporate the current-mode control-law into the power-stage equations. For each module two parasitic elements in addition to the current-loop sampling action are included in the derivation. Furthermore, the control-to-output voltage transfer functions are presented in symbolic form for two cases of interest: the first when the converter has two non-identical modules to study the effect of inductor mismatch, and the second when the converter is composed of n-connected identical modules to assess the effect of varying the number of modules. All responses from PSIM cycle-by-cycle simulations are in good agreement with the mathematical model predictions up to half the switching frequency.

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1. INTRODUCTION

For more than two decades the modular approach in designing dc-dc converters has been employed to satisfy certain input/output requirements that cannot be efficiently met by single-cell converters. With this approach two or more single-cell converters are connected in a variety of arrangements to comply with design requirements. Several arrangements have been reported in the literature serving a wide range of applications such as distributed power systems, dedicated dc power supplies, and renewable energy systems. The four basic arrangements are: the parallel-input/parallel-output (PIPO), the parallel-input/series-output (PISO), the series-input/parallel-output (SIPO), and the series-input/series-output (SISO). Various dc-dc converter topologies like the buck and buck-based [1-19], the boost and boost-based [11, 19-29], and the buck-boost-based [25, 30-32] have been used for the constituent modules of modular converters. The semiconductor devices employed in these converters are commonly driven using pulse-width modulation (PWM) techniques with the converter being operated under voltage-mode control (VMC) or current-mode control (CMC) [1, 2, 4, 6-10, 12, 13, 16, 17, 19-26, 31, 32].

Whether the converter is operated under VMC or CMC, initial investigation of the dynamics of modular dc-dc converters is traditionally performed using small-signal (SS) transfer functions. Averaging techniques such as state-space averaging [33] and circuit averaging [34] are widely used for the SS modeling

of the power stages of these converters. Due to the complexity of modular converters SS modeling is often based on reduced-order (RO) power-stage models, where the modular converter is substituted by an equivalent single-cell one. Nevertheless RO models do not always give detailed description of the SS behavior and therefore a full-order model of the power stage, where each of the constituent modules is independently represented, becomes necessary [11].

For CMC converters, in addition to the power-stage model, a CMC-stage law has to be included into the development of the model. One of the CMC schemes that finds a wide popularity in the power supply industry is the ramp-compensated peak CMC (PCMC) traditionally used for single-cell dc-dc converters due to its advantages over VMC such as better line-noise rejection, and automatic overload protection. An Accurate SS model of PCMC requires the inclusion of the sampling effect of the current loop in its structure. Such a model can be added to the power-stage SS model in two ways: the first can be classified as circuit-oriented where a separate transfer-function block is interfaced with the power-stage model [1, 6, 7, 10, 12, 19, 21, 22, 26, 32], and the second is the state-space algebraic approach where the PCMC law is augmented with the power-stage matrices. The algebraic approach requires more mathematical manipulation but is more general since it allows the CMC converter model to be obtained in symbolic state-space form. This approach has been used for the SS modeling of single-cell PCMC dc-dc converters [35-37]. It has also been employed for one type of PCMC modular arrangements, namely the PISO structure, but with the assumption that the constituent modules are identical and the components are ideal [13, 25].

Among the modular arrangements the PIPO architecture has been widely used for power supply designs with several paralleling schemes being employed most of which are classified and evaluated in [3], and [26]. One of these schemes adopts the ramp-compensated PCMC. Small-signal modeling of PCMC PIPO converters has partially appeared in several publications [1, 6, 7, 10, 19, 21, 22, 26], but the ones that included parasitic elements and the sampling effect of the current loop have relied on RO models for power-stage modeling and the circuit-oriented approach for CMC modeling [1, 19, 21, 22]. There is no published work that combines a detailed power-stage SS model with an accurate CMC-stage law in a symbolic state-space form for PCMC PIPO converters. With the continuous interest in modular converters more research is needed into the area of SS of the PIPO architecture and other basic arrangements of modular converters. In fact, recent publications [38-40] show that there is still a need to improve existing models of the single-cell dc-dc converters.

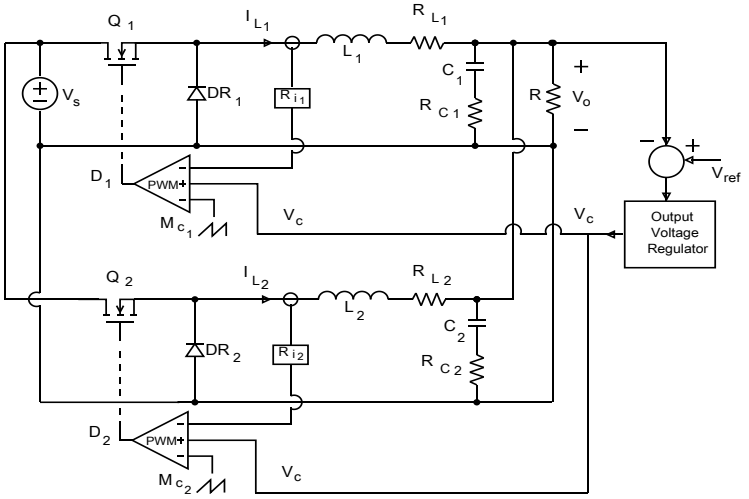
The contribution of this paper is: (1) we propose a state-space-based averaged SS model in symbolic form for a PCMC PIPO buck converter operating in the continuous-conduction mode. In modeling the power stage each module is independently represented. For CMC modeling the state-space algebraic approach is used to incorporate the PCMC law into the power-stage equations. The sampling effect of the current loop and two parasitic elements, namely the inductor internal resistance and the capacitor equivalent series resistance are included in the derivation. (2) Based on the proposed model, the control-to-output voltage expressions are derived in symbolic form for two cases of interest: The first is a two-module PCMC PIPO converter with mismatched circuit parameters to study the effect of inductor mismatch; and the second is a PCMC PIPO converter consisting of *n*-connected identical modules to assess the effect of varying the number of modules. These issues have not been addressed before and are amenable to investigation. It will be shown in the sequel that for circuit parameters based on a standard design, the inductor mismatch has small effect on the gain and phase of the control-to-output voltage responses at low frequencies, while varying the number of modules has a noticeable impact on the low-frequency region of these responses.

The rest of this paper is organized as follows: Section 2 and the Appendix present the procedure used to construct the power-stage and CMC-stage models. Section 3 discusses the derivation of the control-to-output voltage expressions and the responses generated from feeding these expressions into Matlab. It also presents PSIM "ac sweep" simulation results for comparison. The conclusion is given in Section 4.

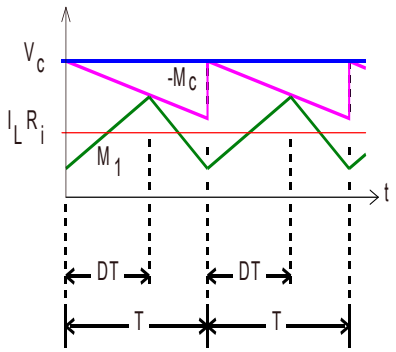
2. SMALL-SIGNAL MODELING

Figure 1(a) shows a two-module PCMC PIPO buck converter. The control of each module can be explained with the help of Figure 1(b): A constant-frequency clock starts the switching cycle (T) and transistor ON time. Inductor current (i_L) sensed by resistor (R_i) is compared with control voltage (V_C), generated by the voltage feedback loop. Transistor duty-ratio (D) is determined when the sensed inductor current whose rising slope [$M_1 = (V_S - V_O)*R_i / L$] reaches a peak value set by V_C. A compensating ramp with slope (M_C) is needed to eliminate instability when $D > 0.5$ [41]. The converter works in the continuous-conduction mode; the inductance and switching frequency are chosen such that i_L never falls to zero.

Current-mode control results in an inner (current) loop that regulates the inductor current. The controller in the outer (voltage) loop generates the value of V_C needed to regulate the output voltage (V_O) at a desired value. The controller's design is outside the scope of this work.



(a)



(b)

Figure 1. (a) Schematic of PCMC PIPO buck converter, (b) Supporting waveforms at steady state

2.1. Power-stage modeling

Figure 2 shows the power stage of the converter of Figure 1(a) with transistors Q1 and Q2 replaced by switches S_{11} and S_{21} respectively. Diodes DR_1 and DR_2 are substituted by switches S_{12} and S_{22} respectively. Capacitor C_e is the parallel combination of C_1 and C_2 while resistor R_e represents the parallel equivalence of R_{C1} and R_{C2}. A current source is added across the load to include the effect of changes in load current.

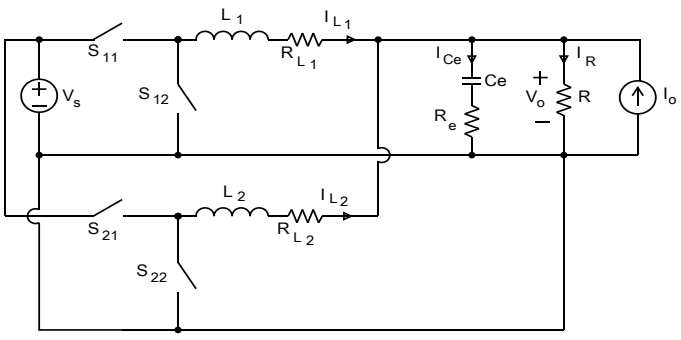


Figure 2. Schematic of the circuit used for power stage modeling

State-space equations (SSEs) describing the converter modes of operation are derived using circuit equations. After time averaging and SS linearization (details in Appendix) the SSEs representing the power stage are

$$\dot{\hat{\mathbf{x}}} = \frac{d}{dt}\begin{bmatrix}\hat{\imath}_{L1}\\ \hat{\imath}_{L2}\\ \hat{v}_{ce}\end{bmatrix} = \begin{bmatrix}\frac{-(R_{L1}+R_p)}{L_1} & \frac{-R_p}{L_1} & \frac{-R_p}{L_1R_e}\\ \frac{-R_p}{L_2} & \frac{-(R_{L2}+R_p)}{L_2} & \frac{-R_p}{L_2R_e}\\ \frac{R_p}{R_eC_e} & \frac{R_p}{R_eC_e} & \frac{-R_p}{RR_eC_e}\end{bmatrix}\begin{bmatrix}\hat{\imath}_{L1}\\ \hat{\imath}_{L2}\\ \hat{v}_{ce}\end{bmatrix} + \begin{bmatrix}\frac{V_s}{L_1} & 0 & \frac{D_1}{L_1} & \frac{-R_p}{L_1}\\ 0 & \frac{V_s}{L_2} & \frac{D_2}{L_2} & \frac{-R_p}{L_2}\\ 0 & 0 & 0 & \frac{R_p}{R_eC_e}\end{bmatrix}\begin{bmatrix}\hat{d}_1\\ \hat{d}_2\\ \hat{v}_s\\ \hat{\imath}_o\end{bmatrix} \quad (1)$$

Where the symbol (^) represents SS variations and

$$R_e = \frac{R_{c1}R_{c2}}{R_{c1}+R_{c2}}\,;\, R_p = \frac{R\,R_e}{R+R_e} \quad (2)$$

$$C_e = C_1 + C_2 \quad (3)$$

2.2. CMC-stage modeling

The "New Continuous Time" technique [41] for the SS modeling of single-cell PWM PCMC dc-dc converters is widely accepted and will be adopted for this work. Based on this technique, the SS model of the converter under consideration is shown in Figure 3. For each module, the CMC model includes: the modulator gain F_m, the sampling gain of the current loop H_L, and the feedforward gains H_S and H_O created when the current feedback path is closed.

a. Module pulse-width modulator gain

The modulator gains of a module 1 and module 2 can be respectively written as

$$F_{m1} = \frac{1}{(M_{11}+M_{C1})T} = \frac{1}{\left(\frac{R_{i1}(V_S-V_O)}{L_1}+M_{C1}\right)T}\,;\, F_{m2} = \frac{1}{(M_{12}+M_{C2})T} = \frac{1}{\left(\frac{R_{i2}(V_S-V_O)}{L_2}+M_{C2}\right)T} \quad (4)$$

b. Sampling gain of the module current loop

The CMC converter is considered a sample-and-hold system. Sampling gain is approximated by a double right-hand plane zero at half the switching frequency. For modules 1 and 2 sampling gains are respectively

$$H_{L1} \cong R_{i1}\left(1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2}\right)\,;\, H_{L2} \cong R_{i2}\left(1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2}\right) \quad (5)$$

Where $Q_z = -2/\pi$ and $\omega_n = \pi/T$

c. Input voltage feedforward gain

A Feedforward gain of the input voltage is created when the module current loop is closed. An improvement to the feedforward gain of [41] is presented in the analysis of [42] for the single-cell buck converter. It adds a high-frequency zero to the gain proposed in [41]. The input voltage feedforward gains of module 1 and module 2 can be respectively expressed as

$$H_{S1} = \frac{TR_{i1}}{2L_1} - \frac{D_1^2T^2R_{i1}(3-2D_1)}{12L_1}s\,;\, H_{S2} = \frac{TR_{i2}}{2L_2} - \frac{D_2^2T^2R_{i2}(3-2D_2)}{12L_2}s \quad (6)$$

d. Output voltage feedforward gain

When the module current loop is closed a feedforward gain of the output voltage is also created. The output voltage feedforward gains of module 1 and module 2 respectively are

$$H_{o1} = \frac{(1-D_1)^2TR_{i1}}{2L_1}\,;\, H_{o2} = \frac{(1-D_2)^2TR_{i2}}{2L_2} \quad (7)$$

Referring to the block diagram of Figure 3, the duty-ratio laws of module 1 and module 2 become

$$\hat{d}_1 = F_{m1}(\hat{v}_c - H_{L1}\hat{\imath}_{L1} + H_{s1}\hat{v}_s + H_{o1}\hat{v}_o)\,;\, \hat{d}_2 = F_{m2}(\hat{v}_c - H_{L2}\hat{\imath}_{L2} + H_{s2}\hat{v}_s + H_{o2}\hat{v}_o) \quad (8)$$

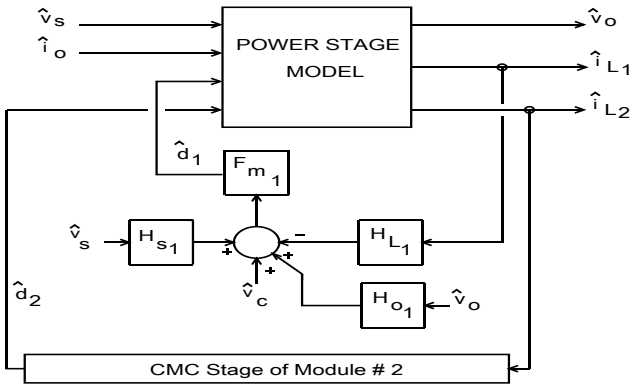


Figure 3. Small-signal block diagram of CMC control

3. CONTROL-TO-OUTPUT VOLTAGE CHARACTERISTICS

Applying Laplace transforms to (1), and substituting for each module its respective duty ratio given by (8), we get

$$\begin{bmatrix} s\hat{\imath}_{L1} \\ s\hat{\imath}_{L2} \\ s\hat{v}_{ce} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1} \\ \hat{\imath}_{L2} \\ \hat{v}_{ce} \end{bmatrix} + \begin{bmatrix} B_{11} & B_{12} & B_{13} \\ B_{21} & B_{22} & B_{23} \\ 0 & 0 & B_{33} \end{bmatrix} \begin{bmatrix} \hat{v}_c \\ \hat{v}_s \\ \hat{\imath}_o \end{bmatrix} \quad (9)$$

Where the *A* and *B* entries are given in Table 1.

The (9) represents the SS model of the two-module converter with current loops closed and voltage loop open. The SS model represented by (9) is suitable for the control of each module individually.

Table 1. Summary of the expressions of (9)

Elements	Equations	Elements	Equations
A_{11}	$\frac{V_s F_{m1}(H_{L1} + H_{o1}R_p) - R_{L1} - R_p}{L_1}$	B_{11}	$\frac{V_s F_{m1}}{L_1}$
A_{12}	$\frac{R_p(V_s F_{m1} H_{o1} - 1)}{L_1}$	B_{12}	$\frac{D_1 + V_s F_{m1} H_{s1}}{L_1}$
A_{13}	$\frac{R_p(V_s F_{m1} H_{o1} - 1)}{L_1 R_e}$	B_{13}	$\frac{R_p(V_s F_{m1} H_{o1} - 1)}{L_1}$
A_{21}	$\frac{R_p(V_s F_{m2} H_{o2} - 1)}{L_2}$	B_{21}	$\frac{V_s F_{m2}}{L_2}$
A_{22}	$\frac{V_s F_{m2}(H_{L2} + H_{o2}R_p) - R_{L2} - R_p}{L_2}$	B_{22}	$\frac{D_2 + V_s F_{m2} H_{s2}}{L_2}$
A_{23}	$\frac{R_p(V_s F_{m2} H_{o2} - 1)}{L_2 R_e}$	B_{23}	$\frac{R_p(V_s F_{m2} H_{o2} - 1)}{L_2}$
$A_{31} = A_{32}$	$\frac{R_p}{R_e C_e}$	B_{33}	$\frac{R_p}{R_e C_e}$
A_{33}	$\frac{-R_p}{R R_e C_e}$		

3.1. Case 1: Control-to-output voltage with mismatched inductor values

The control-to-output voltage transfer function is of interest to the power supply designer because it provides a tool for voltage-feedback control design. Referring to the converter of Figure 1(a) we have

$$v_o = v_{ce} + s v_{ce} C_e R_e \quad (10)$$

Therefore the control-to-output voltage is

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{\hat{v}_{ce}}{\hat{v}_c}(1 + sC_e R_e) \quad (11)$$

From (9) the control-to-output capacitor voltage can be derived as

$$\frac{\hat{v}_{ce}}{\hat{v}_c} = \frac{s+k_2/k_1}{s^3-k_3s^2+k_4s+k_5} \quad (12)$$

Where

$$k_1 = A_{31}B_{11} + A_{32}B_{21} \quad (13a)$$

$$k_2 = B_{21}(A_{12}A_{31} - A_{11}A_{32}) + B_{11}(A_{21}A_{32} - A_{22}A_{31}) \quad (13b)$$

$$k_3 = A_{11} + A_{22} + A_{33} \quad (13c)$$

$$k_4 = A_{11}(A_{22} + A_{33}) - A_{12}A_{21} - A_{13}A_{31} + A_{22}A_{33} - A_{23}A_{32} \quad (13d)$$

$$k_5 = A_{11}(A_{23}A_{32} - A_{22}A_{33}) + A_{12}(A_{21}A_{33} - A_{23}A_{31}) + A_{13}(A_{22}A_{31} - A_{21}A_{32}) \quad (13e)$$

Where the *A* and *B* entries are given in Table 1.

It should be noted here that elements A_{11} and A_{22} in (12) depend on the sampling effect terms given by (5), and therefore the numerator of (12) is third order while the denominator is of the fifth order. Using (11) the effect of mismatch between modules on the control-to-output voltage response can be assessed. As an example, a difference of 50% is assumed between inductances L_1 and L_2. Inductance mismatch can be less than this, but the worst-case scenario is behind this choice. Circuit parameters used are:

L_1 = 50 µH; L_2 = 75 µH; $R_{L1} = R_{L2}$ = 20 mΩ; V_S = 40 V; V_O = 24 V; R = 2.4 Ω; $R_{i1} = R_{i2}$ = 0.1 Ω
$C_1 = C_2$ = 10 µF; $R_{C1} = R_{C2}$ = 50 mΩ; switching frequency f_S = 100 kHz

The (11) is programmed into Matlab. The control-to-output voltage responses are depicted in Figure 4, and Figure 5 with ramp amplitudes V_{ramp} = 0.16 V and 0.59 V respectively. These values are chosen to demonstrate the underdamped and damped responses. The responses when identical inductors are used are also plotted for comparison. In addition, the figures illustrate PSIM "ac sweep" results. The "ac sweep" allows users to obtain frequency responses with the circuit being in its original switched-mode form. Good agreement can be generally observed between the model predictions and PSIM results up to half the switching frequency. Matlab pole-zero locations are given in Table 2. From Figure 4, Figure 5, and Table 2 the following can be realized:

a. When identical inductors are used with V_{ramp} = 0.16 V, Figure 4 shows that the converter control-to-output voltage response becomes similar to that of the single PCMC buck. The behavior, after pole-zero cancellation, is influenced by a real left-hand plane (LHP) pole at low frequencies. At high frequencies there is a real LHP zero at $1/(C_eR_e)$. In addition, there is a complex pole at half the switching frequency ($f_S/2$) which is responsible for the peaking observed. This double pole is due to the sampling effect of the current loop. The *Q* of this second-order pole is controlled using the compensation ramp. As in single-cell PCMC converters [41], the equation used to decide on the size of ramp required to prevent peaking at $f_s/2$ is

$$Q = \frac{1}{\pi[(1-D)(1+M_c/M_1)-0.5]} \quad (14)$$

Critical damping of the second-order pole is achieved with V_{ramp} = 0.59 V as shown in Figure 5. This corresponds to slope ratio M_C/M_1 = 1.84. Table 2 shows that by increasing V_{ramp} to 0.59V the double pole splits into two real LHP poles: One of these poles moves towards the low-frequency region and the other to frequencies beyond $f_S/2$.

b. With mismatched inductors and V_{ramp} = 0.16 V, the double zero cancels out with the nearest double pole as Table 2 shows. Figure 4 indicates a slight decrease in the dc gain. Also, a small phase difference and less peaking at $f_S/2$ can be observed. The effective slope ratio is

$$\frac{M_{c2}}{M_{12}} = \frac{0.16/T}{R_i(V_S-V_O)/L_2} = \frac{0.16/(10\times10^{-6})}{0.1(40-24)/(75\times10^{-6})} = 0.75 \xrightarrow{yields} Q = \frac{1}{\pi[(1-0.6)(1+0.75)-0.5]} = 1.592$$

and the damping ratio = 0.5/*Q* = 0.314, which is close to the damping ratio of 0.312 predicted by Matlab.

When V_{ramp} = 0.59 V, Figure 5 shows a slight decrease in the dc gain for the case of mismatched inductors, and there is around 2 dB drop in the gain and a phase difference of 6 degrees at 20 kHz. The figure also shows an overdamped response since

$$\frac{M_{c2}}{M_{12}} = \frac{0.59/T}{R_i(V_s-V_o)/L_2} = \frac{0.59/(10\times10^{-6})}{0.1(40-24)/(75\times10^{-6})} = 2.76 \xrightarrow{yields} Q = \frac{1}{\pi[(1-0.6)(1+2.76)-0.5]} = 0.316$$

and the damping ratio = 1.581. Matlab, however, gives a damping ratio of 1 because the roots of the fifth-order denominator are all first-order poles.

To ensure good current sharing between the mismatched modules, each module should have its own ramp generator as shown in Figure 1(a). Good current sharing can be achieved by controlling the ramp slope difference (M_{C1}–M_{C2}). Current-mode control provides an excellent current sharing without compromising the system's reliability and modularity [19].

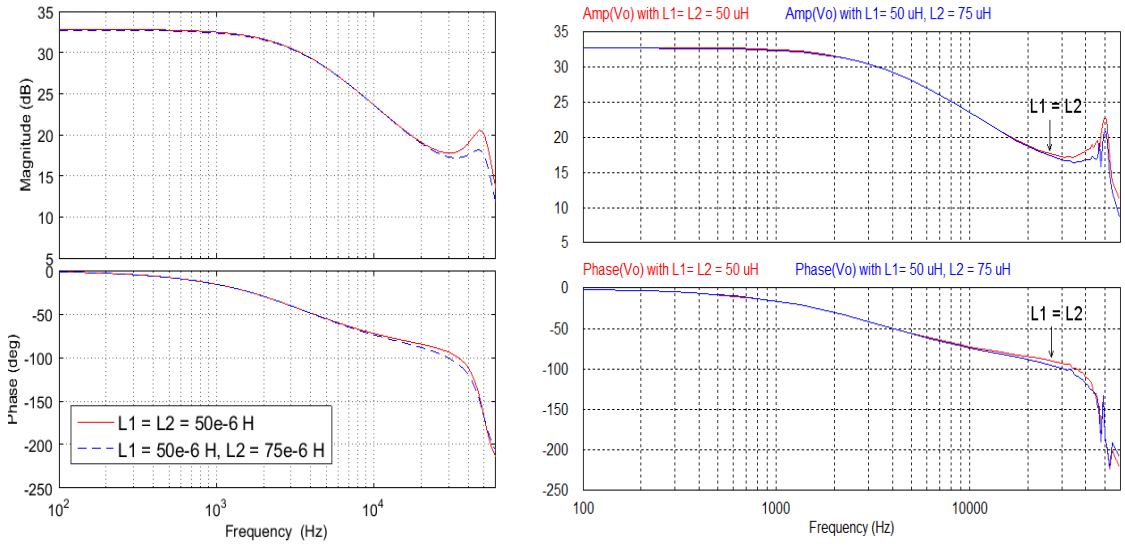


Figure 4. Comparison of control-to-output voltage responses when identical and non-identical inductors are used with V_{ramp} = 0.16 V. left traces: model predictions; right traces: PSIM results

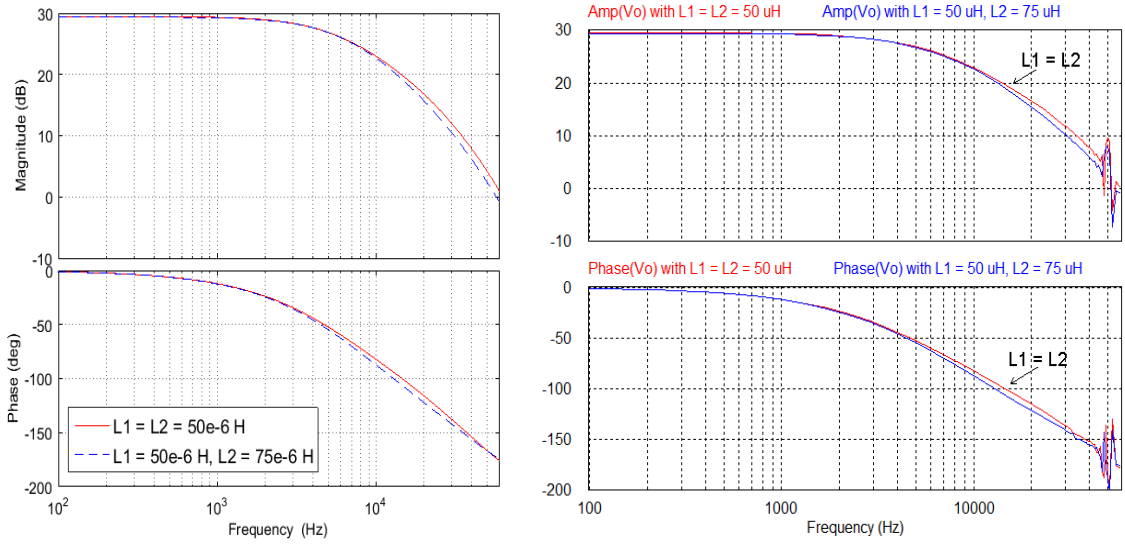


Figure 5. Comparison of control-to-output voltage responses when identical and non-identical inductors are used with Vramp = 0.59 V. left traces: model predictions; right traces: PSIM results

Table 2. Matlab pole-zero locations

	Under-damped Response (Ramp Amplitude = 0.16 V)				Damped Response (Ramp Amplitude = 0.59 V)			
	$L_1 = L_2 = 50$ µH	damp. ratio	$L_1 = 50$ µH $L_2 = 75$ µH	damp. ratio	$L_1 = L_2 = 50$ µH	damp. ratio	$L_1 = 50$ µH $L_2 = 75$ µH	damp. ratio
	-2e+06 + 0i		-2e+06 + 0i		-2e+06 + 0i		-2e+06	
zeros	-49348 + 3.106e+05i		-74022 + 3.057e+05i		-3.140e+05 +2373i		-6.593e+05	
	-49348 - 3.106e+05i		-74022 - 3.057e+05i		-3.140e+05 - 2373i		-1.504e+05	
	-48738 + 3.123e+05i	0.154	-49046 + 3.115e+05i	0.156	-3.538e+05 + 0i	1	-8.788e+05	1
	-48738 - 3.123e+05i	0.154	-49046 - 3.115 e+05i	0.156	-3.140e+05 + 2373i	0.997	-3.381e+05	1
poles	-49348 + 3.106e+05i	0.157	-98146 + 2.991e+05i	0.312	-3.140e+05 - 2373i	0.997	-2.831e+05	1
	-49348 - 3.106e+05i	0.157	-98146 - 2.991e+05i	0.312	-2.595e+05 + 0i	1	-1.019e+05	1
	-22365 + 0i	1	-22763 + 0i	1	-35804 + 0i	1	-38373	1

3.2. Case 2: Varying the number of modules

In this subsection, the state-space algebraic approach is applied for the small-signal modeling of the PCMC PIPO converter when (n) identical modules are used. The aim is to find an expression for the control-to-output voltage with (n) as a variable. The procedure used in the previous subsection is followed here.

Referring to (9), if identical modules are assumed we have $A_{11} = A_{22}$; $A_{12} = A_{21}$; $A_{13} = A_{23}$; $A_{31} = A_{32}$ and $B_{11} = B_{21}$; $B_{12} = B_{22}$; $B_{13} = B_{23}$. The control-to-output capacitor voltage can then be derived as

$$\frac{\hat{v}_{ce}}{\hat{v}_c} = \frac{2A_{31}B_{11}}{s^2 - s(A_{11}+A_{12}+A_{33}) + A_{33}(A_{11}+A_{12}) - 2A_{13}A_{31}} \quad (15)$$

With three and four identical modules the control-to-output capacitor voltage laws are respectively

$$\frac{\hat{v}_{ce}}{\hat{v}_c} = \frac{3A_{31}B_{11}}{s^2 - s(A_{11}+2A_{12}+A_{33}) + A_{33}(A_{11}+2A_{12}) - 3A_{13}A_{31}} \quad (16)$$

$$\frac{\hat{v}_{ce}}{\hat{v}_c} = \frac{4A_{31}B_{11}}{s^2 - s(A_{11}+3A_{12}+A_{33}) + A_{33}(A_{11}+3A_{12}) - 4A_{13}A_{31}} \quad (17)$$

In general, for (n) identical modules, the control-to-output capacitor voltage becomes

$$\frac{\hat{v}_{ce}}{\hat{v}_c} = \frac{nA_{31}B_{11}}{s^2 - s(A_{11}+(n-1)A_{12}+A_{33}) + A_{33}(A_{11}+(n-1)A_{12}) - nA_{13}A_{31}} \quad (18)$$

Substituting for A and B entries (Table 1) and using the fact that $R_e \ll R$, the (18) is approximated as

$$\frac{\hat{v}_{ce}}{\hat{v}_c} \cong \frac{nRF_mV_s}{RLC_es^2 + s[L + RC_e(R_L - F_mV_s(nR_eH_o + H_L) + nR_e)] + R_L - F_mV_s(nRH_o + H_L) + nR} \quad (19)$$

Where F_m, H_L, and H_O are given by (4), (5), and (7) respectively. Using (11) the control-to-output voltage is

$$\frac{\hat{v}_o}{\hat{v}_c} \cong \frac{nRF_mV_s(1 + sC_eR_e)}{RLC_es^2 + s[L + RC_e(R_L - F_mV_s(nR_eH_o + H_L) + nR_e)] + R_L - F_mV_s(nRH_o + H_L) + nR} \quad (20)$$

It can be noticed that the denominator of (20) is third order when we substitute for the sampling gain H_L. This indicates that having identical modules reduces the system's order from five to three. With identical modules and the same parameters of Subsection 3.1, Figure 6 shows the responses predicted by the derived model for n = 2, n = 3, and n = 4 with slope ratio M_C/M_1 = 0.5, while Figure 7 gives the responses when M_C/M_1 = 1.84. Each figure compares PSIM results with the model predications. Good agreement can be reported up to $f_S/2$. It can be observed that although varying the number of modules has no effect on the peaking at $f_S/2$ it does change the gain and phase responses at low frequencies. The significance of (20) is that it symbolically gives the control-to-output voltage response with n as a variable, with sampling gain and two parasitic elements included, which is a useful tool for designing the voltage feedback controller.

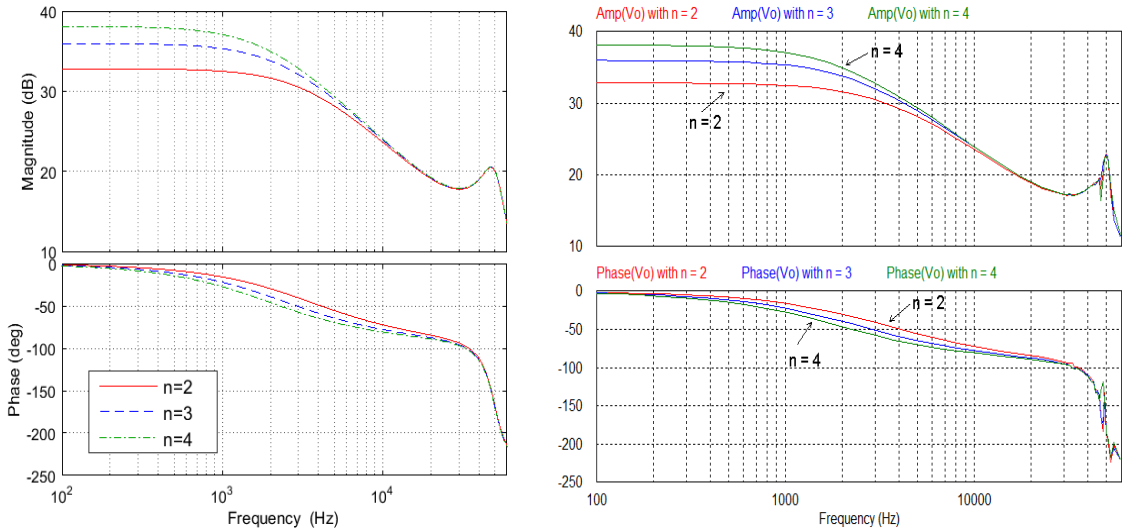


Figure 6. Control-to-output voltage response with n as a running parameter and $M_C/M_1 = 0.5$
left traces: model predictions; right traces: PSIM results

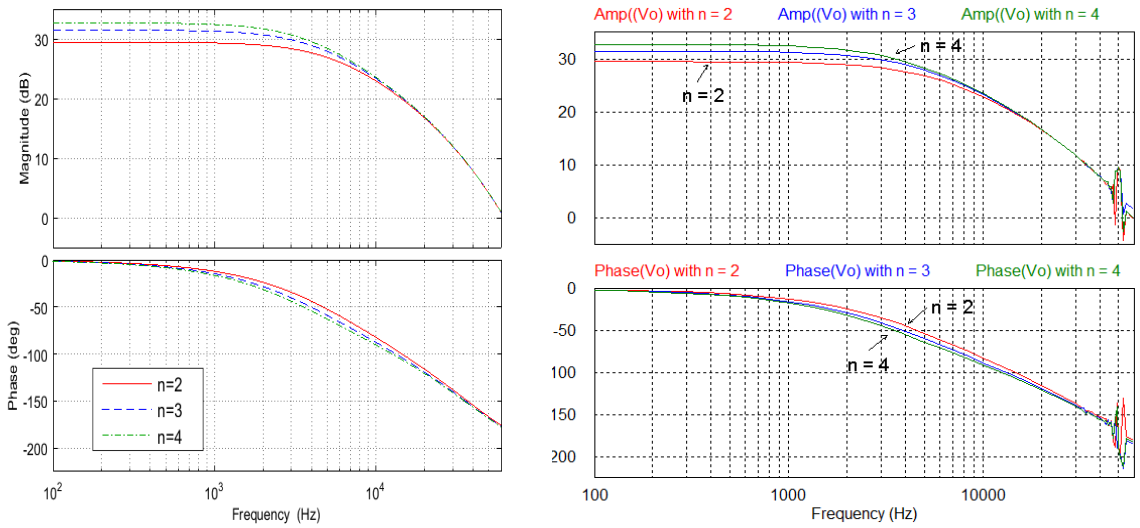


Figure 7. Control-to-output voltage response with n as a running parameter and $M_C/M_1 = 1.84$
left traces: model predictions; right traces: PSIM results

4. CONCLUSION

A state-space-based averaged small-signal model in symbolic form is developed for a PCMC PIPO buck converter operating in the continuous-conduction mode. The model combines a detailed power-stage model with an accurate CMC-stage law that includes the current-loop sampling action. Based on the proposed model, the control-to-output voltage transfers are derived in symbolic form for two cases: The first is when the converter has two mismatched modules taking inductor mismatch as an example, and the second with the converter having n-connected identical modules. The derived expressions, validated by PSIM simulations, are insightful and do not require much computation time to produce the converter responses. The control-to-output voltage is 5^{th} order for the case of mismatched modules and 3^{rd} order when identical modules are used. Peaking at half the switching frequency is present in both cases and the value of ramp to prevent it has been quantified. Peaking is affected by inductor mismatch but not by varying the number of modules. Inductor mismatch has small effect on the gain and phase of the control-to-output voltage response at low frequencies even when this mismatch reaches a hypothetical 50%. Varying the number of modules on the other hand has a noticeable impact on the low-frequency region of the control-to-output voltage response.

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APPENDIX: PROCEDURE FOR DERIVING THE POWER-STAGE SMALL-SIGNAL MODEL

Referring to Figure 2, there are four subintervals or modes of operation in a switching cycle as shown in the control sequence of Figure 8.

MODE 1: Subinterval [0 ~ ΦT]: S11 ON/ S12 OFF and S21 OFF/ S22 ON

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-(R_{L1}+R_p)}{L_1} & \frac{-R_p}{L_1} & \frac{-R_p}{L_1 R_e} \\ \frac{-R_p}{L_2} & \frac{-(R_{L2}+R_p)}{L_2} & \frac{-R_p}{L_2 R_e} \\ \frac{R_p}{R_e C_e} & \frac{R_p}{R_e C_e} & \frac{-R_p}{R R_e C_e} \end{bmatrix}}_{\mathbf{A_1}} \underbrace{\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix}}_{\mathbf{X}} + \underbrace{\begin{bmatrix} \frac{1}{L_1} & \frac{-R_p}{L_1} \\ 0 & \frac{-R_p}{L_2} \\ 0 & \frac{R_p}{R_e C_e} \end{bmatrix}}_{\mathbf{B_1}} \underbrace{\begin{bmatrix} V_s \\ I_o \end{bmatrix}}_{\mathbf{U}} \tag{21}$$

MODE 2: Subinterval [ΦT ~ D_1T]: S11 ON/ S12 OFF and S21 ON/ S22 OFF

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-(R_{L1}+R_p)}{L_1} & \frac{-R_p}{L_1} & \frac{-R_p}{L_1 R_e} \\ \frac{-R_p}{L_2} & \frac{-(R_{L2}+R_p)}{L_2} & \frac{-R_p}{L_2 R_e} \\ \frac{R_p}{R_e C_e} & \frac{R_p}{R_e C_e} & \frac{-R_p}{R R_e C_e} \end{bmatrix}}_{\mathbf{A_2}} \underbrace{\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix}}_{\mathbf{X}} + \underbrace{\begin{bmatrix} \frac{1}{L_1} & \frac{-R_p}{L_1} \\ \frac{1}{L_2} & \frac{-R_p}{L_2} \\ 0 & \frac{R_p}{R_e C_e} \end{bmatrix}}_{\mathbf{B_2}} \underbrace{\begin{bmatrix} V_s \\ I_o \end{bmatrix}}_{\mathbf{U}} \tag{22}$$

MODE 3: Subinterval [$D_1T \sim (\Phi+D_2)\,T$]: S11 OFF, S12 ON and S21 ON, S22 OFF

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-(R_{L1}+R_p)}{L_1} & \frac{-R_p}{L_1} & \frac{-R_p}{L_1 R_e} \\ \frac{-R_p}{L_2} & \frac{-(R_{L2}+R_p)}{L_2} & \frac{-R_p}{L_2 R_e} \\ \frac{R_p}{R_e C_e} & \frac{R_p}{R_e C_e} & \frac{-R_p}{R R_e C_e} \end{bmatrix}}_{\mathbf{A_3}} \underbrace{\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix}}_{\mathbf{X}} + \underbrace{\begin{bmatrix} 0 & \frac{-R_p}{L_1} \\ \frac{1}{L_2} & \frac{-R_p}{L_2} \\ 0 & \frac{R_p}{R_e C_e} \end{bmatrix}}_{\mathbf{B_3}} \underbrace{\begin{bmatrix} V_s \\ I_o \end{bmatrix}}_{\mathbf{U}} \tag{23}$$

MODE 4: Subinterval [$(\Phi+D_2)\,T \sim T$]: S11 OFF, S12 ON and S21 OFF, S22 ON

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{-(R_{L1}+R_p)}{L_1} & \frac{-R_p}{L_1} & \frac{-R_p}{L_1 R_e} \\ \frac{-R_p}{L_2} & \frac{-(R_{L2}+R_p)}{L_2} & \frac{-R_p}{L_2 R_e} \\ \frac{R_p}{R_e C_e} & \frac{R_p}{R_e C_e} & \frac{-R_p}{R R_e C_e} \end{bmatrix}}_{\mathbf{A_4}} \underbrace{\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{ce} \end{bmatrix}}_{\mathbf{X}} + \underbrace{\begin{bmatrix} 0 & \frac{-R_p}{L_1} \\ 0 & \frac{-R_p}{L_2} \\ 0 & \frac{R_p}{R_e C_e} \end{bmatrix}}_{\mathbf{B_4}} \underbrace{\begin{bmatrix} V_s \\ I_o \end{bmatrix}}_{\mathbf{U}} \tag{24}$$

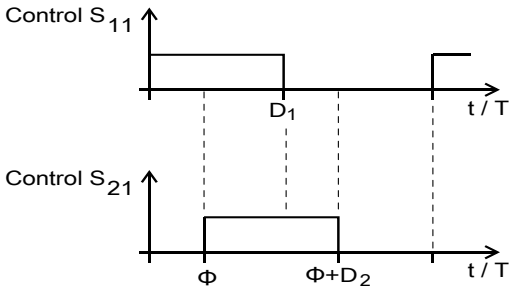

Figure 8. Switching sequence in one cycle of converter operation

Since the switching frequency is much higher than the natural frequency of a converter module, the four state-space descriptions can be replaced by a single state-space description which represents the power stage over a complete period. This is done by time averaging (21)-to-(24), doing so we get

$$\begin{aligned} \dot{\mathrm{X}} = {} & [\Phi \mathrm{A}_1 + (D_1 - \Phi)\mathrm{A}_2 + (D_2 - D_1 + \Phi)\mathrm{A}_3 + (1 - D_2 - \Phi)\mathrm{A}_4]\mathrm{X} + \\ & [\Phi \mathrm{B}_1 + (D_1 - \Phi)\mathrm{B}_2 + (D_2 - D_1 + \Phi)\mathrm{B}_3 + (1 - D_2 - \Phi)\mathrm{B}_4]\mathrm{U} \end{aligned} \tag{25}$$

Introducing small-signal perturbations $\mathrm{X} = \mathrm{X} + \hat{\mathrm{x}}$; $\mathrm{U} = \mathrm{U} + \hat{\mathrm{u}}$; $D = D + \hat{d}$ into (25), where symbol (^) means small-signal variations and $\hat{\mathrm{x}} \ll \mathrm{X}$; $\hat{\mathrm{u}} \ll \mathrm{U}$; $\hat{d} \ll D$, and keeping the ac terms we get

$$\begin{aligned} \dot{\hat{\mathrm{x}}} = {} & [\Phi(\mathrm{A}_1 - \mathrm{A}_2 + \mathrm{A}_3 - \mathrm{A}_4) + D_1(\mathrm{A}_2 - \mathrm{A}_3) + D_2(\mathrm{A}_3 - \mathrm{A}_4) + \mathrm{A}_4]\hat{\mathrm{x}} + \\ & [(\mathrm{A}_2 - \mathrm{A}_3)\mathrm{X} + (\mathrm{B}_2 - \mathrm{B}_3)\mathrm{U}]\hat{d}_1 + [(\mathrm{A}_3 - \mathrm{A}_4)\mathrm{X} + (\mathrm{B}_3 - \mathrm{B}_4)\mathrm{U}]\hat{d}_2 + \\ & [D_1(\mathrm{B}_2 - \mathrm{B}_3) + D_2(\mathrm{B}_3 - \mathrm{B}_4)]\hat{u} + \Phi[\mathrm{B}_1 - \mathrm{B}_2 + \mathrm{B}_3 - \mathrm{B}_4]\hat{u} \end{aligned} \tag{26}$$

The (26) represents a general linearized small-signal model. Substituting for matrices A1, A2, A3, A4, B1, B2, B3 and B4 into (26), we get (1) used for the power-stage model in Subsection 2.1.