International Journal of Electrical and Computer Engineering (IJECE)
Vol. 9, No. 5, October 2019, pp. 3432~3440
ISSN: 2088-8708, DOI: 10.11591/ijece.v9i5.pp3432-3440

How does technological parameters impact the static current gain of InP-based single heterojunction bipolar transistor?

Jihane Ouchrif, Abdennaceur Baghdad, Aicha Sahel, Abdelmajid Badri, Abdelhakim Ballouk
Department of Electrical Engineering, EEA&TI Laboratory, Faculty of Sciences and Techniques of Mohammedia, Hassan II University of Casablanca, Morocco

Article Info

Article history:

Received Sep 17, 2018
Revised Apr 6, 2019
Accepted Apr 13, 2019

Keywords:

Atlas
BBT.STD
Deckbuild
DevEdit
InP/InGaAs
SHBT
SRH
Static current gain
TCAD
Telecommunication

ABSTRACT

In telecommunication systems, Heterojunction Bipolar Transistors (HBTs) are used extensively due to their good electrical characteristics. The work presented in this paper aims to enhance the electrical performance of the InP / InGaAs Single Heterojunction Bipolar Transistor (SHBT) in terms of the static current gain β. Silvaco's TCAD tools were used for the simulation of the output characteristics of the studied electronic device. Initially, we used the interactive tool Deckbuild to define the simulation program and the device editor DevEdit to design the device structure, and we also used the simulator Atlas which allows the prediction of the electrical characteristics of most semiconductor devices. Because of several phenomena occuring within the electronic device SHBT, we added some physical models included in the simulator such as SRH, BBT.STD. Afterwards, we investigated the influence of doping concentrations of the base and the collector N_b and N_c on the electrical performance of the InP/InGaAs SHBT, and particularly in terms of the static current gain β. Finally, based on optimal values of the selected parameters, we have defined an optimized device that has a highest current gain β.

Corresponding Author:

Jihane Ouchrif,
Department of Electrical Engineering,
EEA&TI Laboratory, Hassan II University of Casablanca,
FST Mohammedia, PO Box 146 Mohammedia 20650, Morocco.
Email: ouchrif.jihane1@gmail.com

1. INTRODUCTION

Nowadays, ultra-fast and low-noise semiconductor devices are being more and more requested for communication and information systems. A semiconductor, as silicon, is a material that is neither a conductor of electricity, nor an insulator. It can be either one or the other according to various conditions. It has almost an empty conduction band and almost a filled valence band with a very narrow energy gap separating them. Semiconductor is principally classified into two categories : intrinsic and extrinsic. An intrinsic semiconductor is made of the semiconductor material in its extremely pure form, and the number of conduction electrons is equal to the number of holes. It has a poor conductivity. An extrinsic semiconductor is defined as an improved intrinsic semiconductor to whom was added a small amount of impurities by a process called doping, which changes its electrical behavior. The doping helps to improve the conductivity of the semiconductor. Extrinsic semiconductors are divided into two types, N-type or P-type, and this is due to the doping agents used [1].

III-V semiconductor materials are distinguished by their electronic transport properties, because they display a direct band gap and a high electronic mobility. They have excellent speed characteristics, and they are increasingly used for the manufacturing of electronic devices, they allow the operation of these devices at very high frequencies [2].

The transistors are considered as promising electronic devices for communication systems containing high data rate. They are used for some applications that need high gain [3]. As opposed to a homojunction, a heterojunction is a junction that happens between two different semiconductor materials having different gaps. In 1951, William Shokley proposed the heterojunction, and as reported elsewhere [4] the main goal of using the heterojunction is to improve semiconductor performances, because it gives an additional degree of freedom to devices in comparison to the homojunction [5].

Heterojunction bipolar transistors (HBTs) based on III-V semiconductor materials are interesting for power and high frequency applications [4, 5]. The use of wide bandgap emitters is the main raison of HBTs performances. Because, in the case where the emitter bandgap is larger than that in the base layer for an n-p-n HBT, a barrier is created to the forward injection of electrons by the bandgap discontinuity, and as a result a higher turn-on voltage is obtained for the emitter-base diode [6].

Recently, InP-InGaAs HBTs have become outstanding devices characterized by high speed performance, superior frequency performance [7, 8] and excellent current handling capability [9]. It is principally because of the small bandgap width of the material InGaAs used in the base layer that has high electron mobility, which results from very short transit times for the electrons crossing through the base [10].

The electrical performances of bipolar transistors were extensively studied and characterized by figures of merit, among them we cite the static current gain β, the maximum frequency of oscillation f_{max}, the cut-off frequency f_T, or by Emitter Coupled Logic (ECL) gate delay. However, the choice of the figure of merit depends on the application to which the transistor is intended [11]. This present paper aims to study the impact of two selected technological parameters of the SHBT on its electrical performance, more precisely on the static current gain β in order to improve it. The two selected parameters are : the doping concentrations of the base and collector layers, N_b and N_c.

The studied electronic device SHBT is composed of III-V semiconductor materials, an Indium Phosphide (InP) binary alloy and an Indium Gallium Arsenide (InGaAs) ternary alloy. Concerning the material growth and fabrication of the InP/InGaAs SHBT, the Metal Organic Chemical Vapor Deposition (MOCVD) was used in the past for the growth of the epitaxial layers of the SHBT. However, Molecular Beam Epitaxy (MBE) technique is relatively recent in comparison to MOCVD. The MBE materials are grown at a much lower temperature ~450 °C, but MOCVD materials at ~750 °C which have an impact on the device performances [12].

The Molecular Jet Epitaxy (MBE) technique is used for the growth of the epitaxial layers of the SHBT on Fe-doped semi-insulating (100) InP substrates [13]. According to literature, the growth is carried out at a low temperature of ~420°C and it used stoichiometric conditions for both materials the Phosphide and the Arsenide. The description of the different operational aspects which concern the phosphorus generation from a GaP decomposition is detailed in the papers [12, 13].

2. THE PROPOSED METHOD

2.1. TCAD tools of Silvaco

The big challenge for semiconductor manufacturers is to improve semiconductor processing technologies and devices respecting the constraints of time and cost. But thanks to TCAD tools of Silvaco, manufacturers have a reduced number of engineering wafers, their time and money are saved [14].

- Silvaco (Silicon Valley Corporation) [15] is the company that provides TCAD tools (Technology Computer Aided Design) for different markets such as photonics, power electronics, analog and HSIO design, advanced CMOS process….
- Atlas [16, 17] is a two and three dimensional device simulator. It allows users to predict the electrical behavior of any electronic device and it provides insight into the internal physical phenomena occurring within devices.
- DevEdit [18] is a structure and mesh editor, it can be used to either create a device from scratch or to remesh or edit an existing device. It creates standard structures that are easily integrated into Silvaco simulators and other support tools.
- Athena [19] is a simulator tool for semiconductor fabrication processes. It provides techniques to perform efficient simulation analysis that substitutes for costly real world experimentation.
- Deckbuild [20] is the environment where the simulation program is defined in through specific orders. Multiple simulators considered as inputs can be used with Deckbuild such as Athena, Atlas, DevEdit.
- TonyPlot [15] is the environment where the simulation results are displayed. It gives complete possibilities for visualization and analysis of the output characteristics.

The Figure 1 presents the inputs and the outputs of the device simulator Atlas. They are different types of input and output files for Atlas. They are two types for Atlas input files which are: a command file that contains the commands of the simulator described in statements part under Atlas in the Figure 1,

and a structure file that defines the structure to be simulated. Concerning the output files, they are three types: a runtime output which shows errors and warning messages during the simulation, a log file which stores currents and voltages, and the solution file which stores 2D and 3D data associated to values of the solution variables.

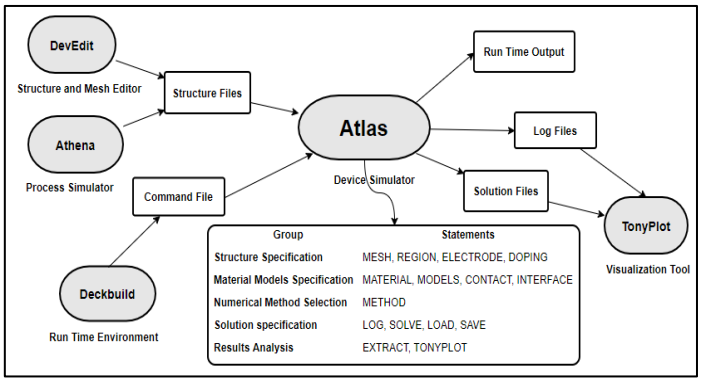

Figure 1. Inputs and outputs of Atlas [15]

2.2. Proposed Solution for the optimization of the static current gain

We have proposed the simulation steps shown in the Figure 2 to improve the static current gain β of the InP/InGaAs SHBT. Firstly, we designed the device structure using the Silvaco tool DevEdit respecting the structure characteristics. Secondly, we modelled physically and numerically the studied electronic device in 2D using the Atlas commands. Thirdly, we simulated the electrical characteristics of the device especially the I-V curve. We then extracted the static current gain β. After that, we selected two technological parameters which are the doping concentrations of the base and the collector N_b and N_c. We evaluated the influence of these parameters on the static current gain β and we understood how these parameters impact the static current gain. Finally, we defined an improved device characterized by a highest static current gain β.

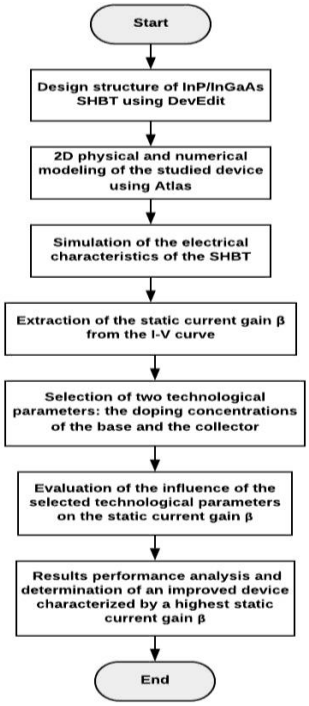

Figure 2. Flowchart indicating the simulation steps for the optimization of the static current gain

3. INP/INGAAS SHBT MODELLING

The device production relies on the fabrication process, but device modelling is necessary to understand the semiconductor device physics as the fabrication process and characterization related to the device. Device modelling is important to analyse output characteristics, and it is recently more momentous because it allows to virtually fabricate "Beyond Moore" devices as highlighted in the International Technology Roadmap for Semiconductor (ITRS) 2016 [21]. Thanks to device modelling, the designer can understand the semiconductor device and its physics [22].

3.1. INP/INGAAS SHBT Device Structure

We simulated the reference device structure InP/InGaAs SHBT based on the research papers [8], [10], the SHBT emitter surface is equal to 5x5 μm^2. This electronic device is composed of different epitaxial layers, namely the cap, Emitter 1, Emitter 2, Spacer, Base, Collector, Sub-collector, and Buffer. The semiconductor materials used are InP and InGaAs, the contacts are made from the material Gold.

The Table 1 contains the characteristics of the various epitaxial layers, such as their dopings, their thicknesses and the materials composing them. The design of the SHBT was performed using the TCAD tools of Silvaco, and more precisely the device structure editor DevEDIT [18].

Table 1. Layer structure of InP/InGaAs SHBT

Layer [8, 10]	Material [8, 10]	Doping (cm^(-3))	Thickness (nm) [8]
Emitter 1	$In_{0.47}Ga_{0.53}As$	n = $1x10^{17}$[8, 10]	135
Emitter 2	InP	n = $1x10^{17}$[8, 10]	40
Spacer	$In_{0.47}Ga_{0.53}As$	Intrinsic [8, 10]	5
Base	$In_{0.47}Ga_{0.53}As$	P =$1.5x10^{19}$[8, 10]	65
Collector	$In_{0.47}Ga_{0.53}As$	n = $1x10^{16}$ [8, 10]	630
Sub-collector	$In_{0.47}Ga_{0.53}As$	n = $1x10^{19}$[10]	500
Buffer	$In_{0.47}Ga_{0.53}As$	Intrinsic [8, 10]	10
Substrate	Semi-insulating InP [8, 10]		

The Figure 3 presents the two-dimensional illustration of the simulated InP/InGaAs Single Heterojunction Bipolar Transistor in the interactive visualization tool TonyPlot. The device structure is symmetrical characterized by two base contacts, two collector contacts and an emitter contact.

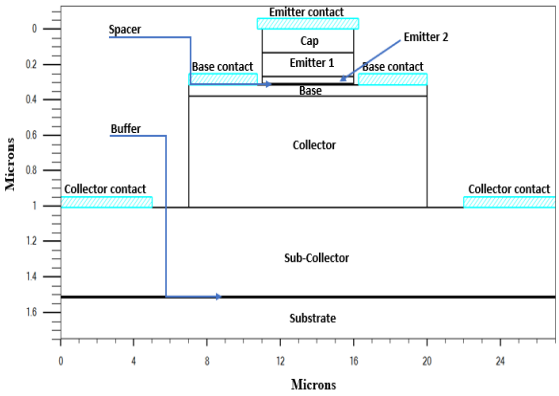

Figure 3. Epitaxial structure of InP/InGaAs SHBT

3.2. Physical Modelling

The effect of doping on electron and hole mobility for the SHBT was considered in the simulation, it was done by integrating the concentration dependent analytical mobility relative to the Caughey and Thomas mobility model. We based our work on the values of the Table 2 [8]. The effective mobility of electrons and holes in each region is defined by the Caughey - Thomas equation and expressed by the following [8, 23]:

$$\mu = \mu_{min}\left(\frac{T_L}{300}\right)^{\beta} + \frac{\mu_{max}\left(\frac{T_L}{300}\right)^{\delta} - \mu_{min}\left(\frac{T_L}{300}\right)^{\beta}}{1+\left(\frac{T_L}{300}\right)^{\gamma}\left(\frac{N}{N_C}\right)^{\alpha}} \quad (1)$$

where, β, δ and γ are the temperature dependent coefficients, T_L = 300 K.

Table 2. Mobility parameters for InP and $In_{0.47}Ga_{0.53}As$ materials

Parameter	InP	$In_{0.47}Ga_{0.53}As$
Electron		
$\mu_{max}(cm^2.V^{-1}.sec^{-1})$	4917	11599
$\mu_{min}(cm^2.V^{-1}.sec^{-1})$	300	3372
N_C (cm^{-3})	$6.4x10^{17}$	$8.9x10^{16}$
α	0.46	0.76
Hole		
$\mu_{max}(cm^2.V^{-1}.sec^{-1})$	151	331
$\mu_{min}(cm^2.V^{-1}.sec^{-1})$	20	75
N_V (cm^{-3})	$1x10^{17}$	$1x10^{18}$
α	0.96	1.37

The Table 2 contains the mobility parameters for the both semiconductor materials InP and $In_{0.47}Ga_{0.53}As$. μ_{max} and μ_{min} are the maximum and the minimum mobilities at low and high levels of doping, N_C and N_V are respectively the electron and hole densities in the conduction and valence bands. Physical models were integrated in the simulation to take into account the physical phenomena associated with SHBT device operation, the simulator Atlas contains several physical models [17] such as mobility models, recombination models, impact ionization, tunneling models and carrier injection models. Among the physical models added in the simulation, we cite the carrier statistic model BGN (Bandgap Narrowing), the recombination model SRH (Shockley read Hall), the Selberherr's model of the ionization impact (IMPACT SELB), the Tunnel effect model BBT.STD (Band-to-Band), and the optical model OPTR.

3.3. Numerical Modelling

The Newton method was used for the numerical modelling, it solves numerically a serie of semiconductor device equations [24] such as the equations of continuity of the carriers, Poisson's equation, the equations of the electric fields.

-Poisson's equation:

$$\text{div}\,(\varepsilon\,\nabla\psi) = \rho \tag{2}$$

where,

Ɛ: the dielectric constant of the material.

Ψ: the local voltage potential.

And ρ: the local charge density.

-The electric field $\vec{E}$:

$$\vec{E} = -\nabla\psi \tag{3}$$

-The carrier continuity equations for electrons and holes:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\,\text{div}\,(\overrightarrow{J_n}) + G_n - R_n \tag{4}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\,\text{div}\,(\overrightarrow{J_p}) + G_p - R_p \tag{5}$$

where,

$\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole currents.

G_n , G_p , R_n and R_p are respectively the generation and recombination rates for the electrons and holes.

-The drift and diffusion currents for electrons and holes:

$$\overrightarrow{J_n} = n.q.\mu_n.\vec{E} + q.D_n.\nabla n \tag{6}$$

$$\overrightarrow{J_p} = p.q.\mu_p.\vec{E} - q.D_p.\nabla p \tag{7}$$

where, μ_n and μ_p are the carrier mobilities, and D_n, D_p are the diffusion coefficients for electrons and holes.

4. RESULTS AND DISCUSSION

We have carried out a 2D physical and numerical modelling of an npn SHBT using Silvaco's TCAD tools. Figures below show the simulation results for the output electrical characteristics I_c - V_{ce} for constant values of base currents at room temperature (T= 300 K).

TCAD tools enable the simulation of electronic devices of various layers and materials, but furthermore it allows to modify the doping profile of each region for the studied electronic device [25]. Therefore, we evaluated the influence of the base and the collector doping concentrations N_b and N_c on the static current gain β of the InP/InGaAs SHBT for the same conditions of the reference device.

4.1. Output Electrical Characteristics

The Figure 4 presents the electrical output characteristics Ic-Vce of the Single Heterojunction Bipolar Transistor (SHBT). We plotted the function I_c= f (V_{ce}) at four constant values of base current from I_b= 2.5 µA to I_b= 10 µA with a step equal to 2.5 and for a V_{ce} which varies between 0 and 2 V. According to the I-V curve above, we noticed that the offset in turn-on voltage (Vceo) is of the order of 50 mv. The difference between the voltages of the heterojunction region and the homojunction region is the main cause of this offset. The InP/InGaAs SHBT static current gain is around 80.24 [26].

In order to define an improved Heterojunction Bipolar Transistor operating in microwave applications, we examinated the impact of technological parameters such as the base and the collector doping concentrations, and we determined the optimal values of these parameters which enable the optimization of the SHBT static current gain.

Figure 5 shows the output characteristics I_c= f (V_{ce}) at I_b = 10 µA and T= 300 K for different values of the doping concentration of the base layer. The Table 3 presents the current gain $\beta = I_c/I_b$ obtained for each base doping concentration N_b. Different values from $1x10^{20}$ cm^{-3} to $1x10^{18}$ cm^{-3} were investigated to understand the impact of this technological parameter.

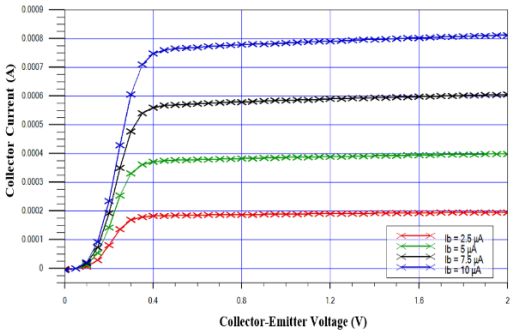

Figure 4. Simulated Ic -Vce Characteristics for the InP/InGaAs SHBT at T =300 K

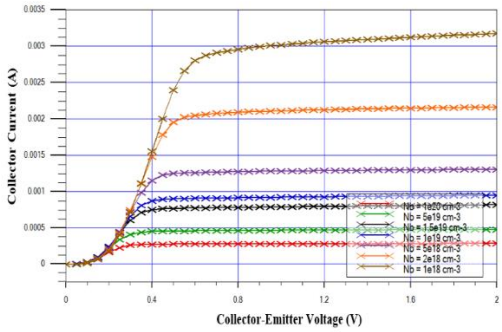

Figure 5. Output Characteristics I_c= f (V_{ce}) for different base doping concentrations N_b at I_b = 10 µA and T = 300 K

Then, according to the Figure 5 and the Table 3, we observed that when we reduce the doping concentration of the base layer, the static current gain increases. Therefore, it is the lowest base doping concentration equal to $1x10^{18}$ cm^{-3} which gives the highest static current gain of about 312.01. The improvement in this case is around 288.84% compared to the reference device. It is an important improvement.

Table 3. Impact of base doping concentration N_b on the static current gain of InP/InGaAs SHBT at I_b= 10 µA and T= 300 K

Base doping concentration N_b (cm^{-3})	I_b (µA)	I_c(mA)	Current gain β (A/A)
$1x10^{20}$	10	0.2797	27.97
$5x10^{19}$	10	0.4714	47.14
$1.5x10^{19}$	10	0.8024	80.24
$1x10^{19}$	10	0.9351	93.51
$5x10^{18}$	10	1.2934	129.34
$2x10^{18}$	10	2.1418	214.18
$1x10^{18}$	10	3.1201	312.01

Figure 6 illustrates the output characteristics I_c= f (V_{ce}) at I_b = 10 µA and T= 300 K for different values of collector doping concentration. Table 4 presents the results of the static current gain β according to the variation of the collector doping concentration N_c. The reference device has a collector doping concentration of 1x10^{16} cm^{-3} , the static current gain is about 80.24.

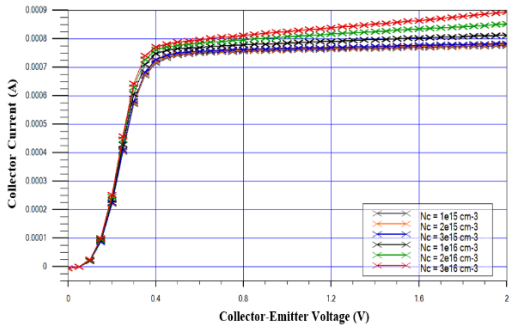

Figure 6. Output Characteristics I_c= f (V_{ce}) for different collector doping concentrations at I_b = 10 µA and T = 300 K

Table 4. Influence of the collector doping concentration on the static current gain of InP/InGaAs SHBT at I_b= 10 µA and T= 300 K

Collector doping concentration N_c (cm^{-3})	I_b (µA)	I_c(mA)	Current gain β (A/A)
3x10^{16}	10	0.8641	86.41
2x10^{16}	10	0.8342	83.42
1x10^{16}	10	0.8024	80.24
3x10^{15}	10	0.7762	77.62
2x10^{15}	10	0.7727	77.27
1x10^{15}	10	0.7693	76.93

It is clearly observed from the Figure 6 and the Table 4 that the static current gain increases slightly with the slight increase of the collector doping concentration. Therefore, it is the higher collector doping which gives the highest static current gain. Then, the collector doping concentration equal to 3x10^{16} cm^{-3} allows obtaining a static current gain higher slightly than that of the reference device, and equal to 86.41. The improvement is slight and it is around 7.68%.

The investigation of the both technological parameters: base and collector doping concentrations, led us to define an improved device according to the optimal values of the selected parameters giving the highest static current gain β, particularly a base doping concentration equal to 1x10^{18} cm^{-3} and a collector doping concentration equal to 3 x10^{16} cm^{-3}. After that, we simulated the optimized device structure following the same steps of the physical and numerical modelling of the reference device SHBT.

Figure 7 presents the curve of the output electrical characteristics I_c=f (V_{ce}) for the optimized device. The function I_c=f (V_{ce}) was plotted for four base currents I_b=2.5 µA, 5µA, 7.5 µA and 10 µA with the step of 2.5. We noticed that for a V_{ce} which varies from 0 to 2V, the offset in turn-on voltage is of the order of 50 mV, and it is the same as that of the reference device structure.

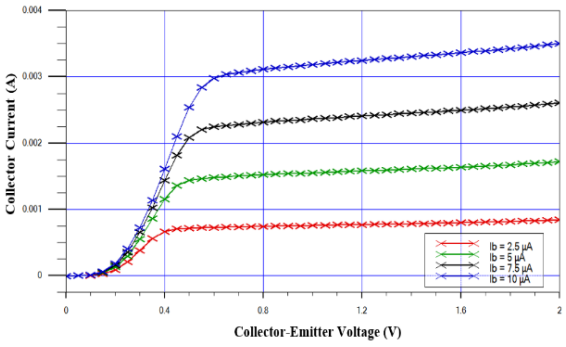

Figure 7. Output Characteristics I_c= f (V_{ce}) for the optimized device at T=300 K

We calculated the static current gain β for the SHBT improved device, it is around 335.93. We then observed that it is higher than that of the SHBT reference device which is equal to 80.24. In this case, there is a huge improvement estimated of the order of 318.65% compared to the reference device.

Other technological parameters were investigated in our other research paper [26] where we have reported that the base width W_b has an important impact on the static current gain β because when we reduce it, the static current gain increases in an important way, while for the emitter length L_e when we increase it the static current gain increases slightly. The reduction of transistor size has many advantages in different aspects especially in the technological one, among these advantages we cite the increase of operation speed and improvement of the device reliability by low power consumption, and smaller devices are required for various reasons, for that manufacturers are fabricating them in accelerating way, by example ultrafine transistors are intended for applications such as semiconductor integrated circuits [27, 28]. The base layer of the SHBT is the most important and critical layer of this device, because technological parameters related to the base layer such as the width and the doping concentration have an important impact on the static current gain β in comparison to other investigated parameters such as the emitter length and the collector doping concentration.

4.2. Comparison with other works

According to the presented results shown in the Table 5, we can notice that we reached a higher static current gain equal to 335.93 with our proposed work after optimization compared to other works.

Table 5. Comparison between the obtained static current gain and other works at T= 300 K

Ref	V_{ceo} (mV)	I_b (µA)	I_c (mA)	Current gain β (A/A)
Our work without optimization	50	10	0.8024	80.24
Proposed work after optimization	50	10	3.3593	335.93
Other work [7]	150	10	0.90	90
Our other work [26]	50	10	2.0718	207.18

5. CONCLUSION

In this work, a two-dimensional physical and numerical modelling was done using Silvaco's TCAD tools for the InP/InGaAs Single Heterojunction Bipolar Transistor. We have integrated in the simulation program the physical models such as SRH, BGN to consider the impact of the physical mechanisms that occur within the studied electronic device. Afterwards, we evaluated the doping concentration influence of the base and the collector layers N_b and N_c on the static current gain β. We then selected the values of these technological parameters that allow us to define an optimized device. We chose the base doping concentration equal to $1x10^{18}$ cm^{-3}, and the collector doping concentration equal to $3x10^{16}$ cm^{-3}. Consequently, the defined optimized device enables obtaining a higher static current gain β equal to 335.93. The estimated improvement is around 318.65%. Between all the investigated parameters, we have reported that technological parameters related to the base layer have a great impact on the static current gain β, these parameters are the base width W_b and the base doping concentration N_b. For our future work prospects, we plan to do an evaluation of the other technological parameters on the static current gain, and also to enhance the electrical performances of this electronic device for AC parameters.

REFERENCES

[1] M. N. Tandjaoui, et al., "Characterization and Modeling of Power Electronics Device," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol/issue: 5(2), pp. 135-141, Oct 2014.
[2] T. G. Sanchez, et al., "Electron transport in InP under high electric field conditions," *IOP science*, pp. 31-36, 1992.
[3] R. Singh and R. Mehra, "Qualitative Analysis of Darlington Feedback Amplifier at 45nm Technology," *Bulletin of Electrical Engineering and Informatics*, vol/issue: 7(1), pp. 21-27, 2018.
[4] A. A. Rezazadeh, et al., "Invited paper ―InP-based HBTs for Optical Telecommunications," *Int. J. Optoelec.*, vol. 10, pp. 489-493, 1995.
[5] S. Chowdhury and S. Basu, "Effect of Device Parameters on Current Voltage Characteristics and Current Gain of InP/InGaAs HBTs," *Journal of Electron Devices*, vol. 9, pp. 362-366, 2011.
[6] B. Yamina and G. Kherreddine, "Modelling Electronic Characteristic of InP/InGaAs Double Heterojunction Bipolar Transistor," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 5(3), pp. 525-530, 2015.
[7] D. Yu, et al., "Ultra-high-speed 0.25µm emitter InP-InGaAs SHBTs with fmax of 687 GHz," *in 2004 International Electron Devices Meeting*, 13-15 Dec. 2004, San Francisco, CA, USA, pp. 557-60, 2005.

[8] T. Tauqeer, et al., "Two-Dimensional Physical and Numerical Modelling of InP-based Heterojunction Bipolar Transistors," *in the* 7^{th} *International Conference on Advanced Semiconductor Devices and Microsystems*, pp. 271-274, Oct 2008.
[9] Song J. I., et al., "Carbon –doped base InP/InGaAs base HBTs with fT=200GHz," *in Proc. IEEE Device Research Conf.*, pp. 97-98, 1994.
[10] J. Sexton and M. Missous, "Annealing Experiments on INP/INGAAS Single and Double HBTs Grown by Molecular Beam Epitaxy," *in Electron Devices for Microwave and Optoelectronic Applications, 2002. EDMO 2002. The* 10^{th} *IEEE International Symposium on*, pp. 300-305, 2002.
[11] E. S. Julian, "Silicon Germanium Heterojunction Bipolar Transistor for Digital Application," *TELKOMNIKA Telecommunication Computing Electronics and Control*, vol/issue: 10(3), pp. 493-498, Sep 2012.
[12] M. Missous, "Optical and electrical properties of InO.48 (AlxGa (1-x)) 0.52P grown by Solid Source MBE using a GaP Decomposition Source," *EDMO 2001*, (Cat. No. 01TH8567). IEEE, pp. 1-8, 2001.
[13] J. Sexton, et al., "GHz Class Low-Power Flash ADC for Broadband Communications," *ASDAM 2008, The Seventh International Conference on Advanced Semiconductor Devices and Microsystems, Smolenice Castle, Slovakia*, pp. 235-238, Oct 2008.
[14] S. K. Dargar, et al., "Performance Evaluation of GaN Based Thin Film Transistor using TCAD Simulation," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 7(1), pp. 144-151, Feb 2017.
[15] www.silvaco.com
[16] C. K. Maiti and G. A. Armstrong, "Technology Computer Aided Design for Si, SiGe and GaAs Integrated Circuits," *IET*, 2007.
[17] ATLAS User's Manual, "Device Simulation Software, Silvaco International," Sep 2010.
[18] DevEdit User's Manual, "Silvaco International," 2006.
[19] ATHENA User's Manual, "2D Process Simulation Software, Silvaco International," Jul 2005.
[20] Deckbuild User's Manual, "Silvaco," Oct 2015.
[21] "2015 International Technology Roadmap for Semiconductors (ITRS) 2.0 Executive Report," 2015.
[22] W. M. Jubadi, et al., "Optimization of Empirical Modelling of Advanced Highly Strained In 0.7Ga 0.3As/In0.52Al0.48As pHEMTs for Low Noise Amplifier," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 7(6), pp. 3002-3009, 2017.
[23] Caughey D. M. and Thomas R E., *Proc IEEE*, vol. 52, pp. 2192, 1967.
[24] J. L. Polleux, et al., "Optimization of InP–InGaAs HPT Gain: Design of an Opto-Microwave Monolithic Amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol/issue: 52(3), pp. 871-881, Mar 2004.
[25] N. Saha, et al., "Comparative Study of IV-Characteristics of Pin Diode at Different Doping Concentrations for Different Semiconductor Materials Using TCAD," *International Journal of Electronics and Communication Engineering (IJECE)*, vol/issue: 4(6), pp. 1-8, 2015.
[26] J. Ouchrif, et al., "Investigation of the static current gain for InP/InGaAs single heterojunction bipolar transistor," *Indonesian Journal of Electrical Engineering and Computer Science*, vol/issue: 13(3), pp. 1345-1354, Mar 2019.
[27] E. S. Julian and R. S. Wahjudi, "Scaling Model for Silicon Germanium Heterojunction Bipolar Transistors," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol/issue: 14(1), pp. 103-109, Apr 2015.
[28] H. Jung, "Threshold voltage roll-off for sub-10 nm asymmetric double gate MOSFET," *International Journal of Electrical and Computer Engineering (IJECE)*, vol/issue: 9(1), pp. 163-169, Feb 2019.