International Journal of Electrical and Computer Engineering (IJECE)
Vol. 9, No. 4, August 2019, pp. 2902~2909
ISSN: 2088-8708, DOI: 10.11591/ijece.v9i4.pp2902-2909

Effects of downscaling channel dimensions on electrical characteristics of InAs-FinFET transistor

Ahmed Mahmood[1], Waheb A. Jabbar[2], Yasir Hashim[3], Hadi Bin Manap[4]
[1,2,4]Faculty of Engineering Technology, Universiti Malaysia Pahang, 26300 Gambang, Kuantan, Pahang, Malaysia
[3]Computer Engineering Department, Faculty of Engineering, Ishik University, Erbil-Kurdistan, Iraq

Article Info

Article history:

Received Sep 10, 2018
Revised Mar 22, 2019
Accepted Apr 3, 2019

Keywords:

Channel dimensions
InAs- FinFET,
I_{ON}/I_{OFF} ratio
MuGFET
Subthreshold swing,

ABSTRACT

In this paper, we present the impact of downscaling of nano-channel dimensions of Indium Arsenide Fin Feld Effect Transistor (InAs- FinFET) on electrical characteristics of the transistor, in particular; (i) ION/IOFF ratio, (ii) Subthreshold Swing (SS), Threshold voltage (VT), and Drain-induced barrier lowering (DIBL). MuGFET simulation tool was utilized to simulate and compare the considered characteristics based on variable channel dimensions: length, width and oxide thickness. The results demonstrate that the best performance of InAs- FinFET was achieved with channel length = 25 nm, width= 5 nm, and oxide thickness between 1.5 to 2.5 nm according to the selected scaling factor (K = 0.125).

Corresponding Author:

Waheb A. Jabbar,
Faculty of Engineering Technology,
Universiti Malaysia Pahang,
26300 Gambang, Kuantan, Pahang, Malaysia,
Email: waheb@ieee.org

1. INTRODUCTION

Nowadays, the application of nanoscience and its inherent technology has been extensively used in interdisciplinary research most especially for the past two decades. The concept of nanotechnology involves the use of low dimensional materials with different structural configurations which include the nanowires, Nano-rods, Nano photo laser production, nanotubes or Nano-crystalline films [1, 2]. Nanoelectronic applications have benefited enormously from the great advancement in the emerging Nano-technology industry and Internet of Things applications [3, 4]. The tremendous downscaling of the transistors' dimensions has enabled the placement of over 100 million transistors on a single chip, thus reduced cost, increased functionality, and enhanced performance of integrated circuits (ICs) [5, 6]. However, shrinking size of the conventional planar transistors would be exceptionally challenging due to leakages, ,electrostatics, energy consumption and other fabrication issues [7-9].

Many researchers and engineers have made lots of efforts on the discovery of different varieties of nanoscale materials such as the field-effect transistor (FET) devices. That application is largely due to the improved properties of these materials which include greater strength, lighter weight, and higher resistance to chemical reactions [10, 11]. In recent years, the uses of FET transistors are widely prevalent in many integrated circuits (ICs). Fin Field Effect Transistor (FinFET) shows a great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies [12-15]. The structure of FinFET provides superior electrical control over the channel conduction, thus, it has attracted widespread interest from researchers in both academia and industry [16-18]. However, aggressively scaling down of channel dimensions, mainly the channel length, will degrade the overall performance due to detrimental short channel effects (SCEs) [19, 20].

New FET structures are being explored on a large scale with one of the structures such as the FinFET, which are described as MOSFET built on a material where the gate is supported by two-to-four channels or configured by to form a dual gate structure [21]. The FinFET's structure is based on the presence of a fin that is perpendicular to the substrate superficies. The conduction occurs thus in two parallel channels that are in vertical plans the conduction remaining parallel to the substrate surface between drain and source area. The drain current is flowing on both sides of the fin is a way to increase the discharge source for the same area in the channel region [22, 23].

In this study, we simulate and analyze the impact of reducing channel dimensions [length (L), width (W), and oxide thickness (Tox)] on InAs-FinFET performance in terms of various electrical characteristics, namely; (i) I_{ON}/I_{OFF} ratio, (ii) Subthreshold Swing (SS), Threshold voltage (V_T), and Drain-induced barrier lowering (DIBL). Furthermore, we exploit a scaling factor, K to downscale all dimensions (L, W, and T_{ox}) together and identify the best performance based on the selected scaling factor. According to the highest I_{ON}/I_{OFF} ratio, and nearest SS to the ideal SS, we have designed the best channel dimensions of InAs-FinFET. The remaining part of this paper is structured as follows: The next section presents simulation modeling. Section 3 introduces results and discussions. Finally, a conclusions are drawn up in Section 4.

2. RESEARCH METHOD

2.1. Simulation tools

In this study, the well-known MuGFET [24, 25] which is developed and designed by Purdue University (USA) is used as the simulation tool. MuGFET can select either PADRE or PROPHET for simulation, in which both simulator are developed by Bell Laboratories. PROPHET is a partial differential equation profiler for one, two or three dimensions, whereas PADRE is a device-oriented simulator for 2D or 3D devices with arbitrary geometry. The software can generate useful characteristic FET curves for engineers, especially to fully explain the underlying physics of FETs. It can also provide self-consistent solutions to poison and drift-diffusion equations.

2.2. Simulation design

This simulation tool is utilized to investigate the characteristics of the InAs-FinFET transistor based on various channel's dimensions. The output characteristic curves of the transistor under different conditions and with different parameters are considered. The effects of variable channel dimensions, namely; channel length, width and oxide thickness in addition to scaling factor of the InAs-FinFET transistor, are determined based on the I–V characteristics that derived from the simulation. In this paper, the I_d–V_g characteristics of InAs-FinFET at the temperature of 300 K are simulated and evaluated with the simulation parameters that listed in Table 1.

Table 1. Simulation parameters

Parameters	value
Channel length (L)	(10, 15, 25, 35 and 45) nm
Channel width (W)	(5, 10, 12, 15 and 20) nm
Oxide thickness (T_{OX})	(1.5, 2.5, 5 and 7) nm
Scaling factor (K)	(0.125, 0.25, 0.5 and 1.00)
channel concentration p -type	10^{16} cm^{-3}
channel concentration N -type	10^{19} cm^{-3}

Four simulation experiments were designed to evaluate the performance of InAs-FinFET in terms of the considered metrics. In the first scenario, channel length was changed, whereas other dimensions (W and Tox) were kept constant. In the second scenario, the impact of changing channel width was investigated while both length and thickness of channel were kept constant. In the third scenario, oxide thickness was changed and length and width were fixed. Finally, the impact of changing scaling factor was studied by changing the three dimensions all at once based on a changeable scaling factor.

3. RESULTS AND DISCUSSION

This paper presents the obtained simulation results to evaluate characteristics of the InAs-FinFET transistor based on various channel's dimensions. The output characteristic curves of the transistor under different conditions and with different parameters are considered. The effects of variable channel dimensions, namely; channel length, width and oxide thickness in addition to scaling factor of the InAs-FinFET transistor,

are determined based on the I–V characteristics that derived from the simulation. In this paper, the I_d–V_g characteristics of InAs-FinFET at the temperature of 300 K are simulated and evaluated.

Four simulation experiments were designed to evaluate the performance of InAs-FinFET in terms of the considered metrics. In the first scenario, channel length was changed, whereas other dimensions (W and T_{OX}) were kept constant. In the second scenario, the impact of changing channel width was investigated while both the length and thickness of the channel were kept constant. In the third scenario, oxide thickness was changed and length and width were fixed. Finally, the impact of changing scaling factor was studied by changing the three dimensions all at once based on a changeable scaling factor. This section investigates the effect of channel dimensions on the I–V characteristics of InAs-FinFET. A simulation tool (MuGFET) was used to investigate the effect of channel dimensions on its electrical characteristics.

3.1. Impact of varying channel length

The scaling down of channel length L and its effect on the characteristics of InAs FinFET have been studied. The simulation of transfer characteristics (drain current I_d –gate voltage V_g) have been down with different channel lengths (L) channel width (W) and oxide thicknesses (T_{OX}). The limitation parameters were used to find the optimal channel dimensions were I_{ON}/I_{OFF} ratio (where I_{OFF} is an I_d at OFF state at V_g = 0 V and I_{ON} is an I_d at ON state at V_g = 1 V) and sub-threshold swing (SS) and the threshold voltage (V_T) and drain-induced barrier lowering (DIBL).

Figure 1(a) illustrates the relation between I_{ON}/I_{OFF} ratio with the channel length of 10 15 25 35 and 45 nm and at W = 5 nm and T_{OX} = 2.5 nm the I_{ON} /I_{OFF} ratio increased to 10^6 for increasing L from 10 to 40 nm for V_{DD} = 5 V. For V_{DD}= 5 V increased value for I_{ON}/I_{OFF} ratio were more than10^4 at L =40 nm. It is noticed that for L range from 10 to 30nm the highest I_{ON}/I_{OFF} ratio happen for V_{DD}= 5 V while for 30 to 45 nm, L range the highest I_{ON}/I_{OFF} ratio happen for V_{DD}= 5 V where the lowest leakage current I_{OFF}.

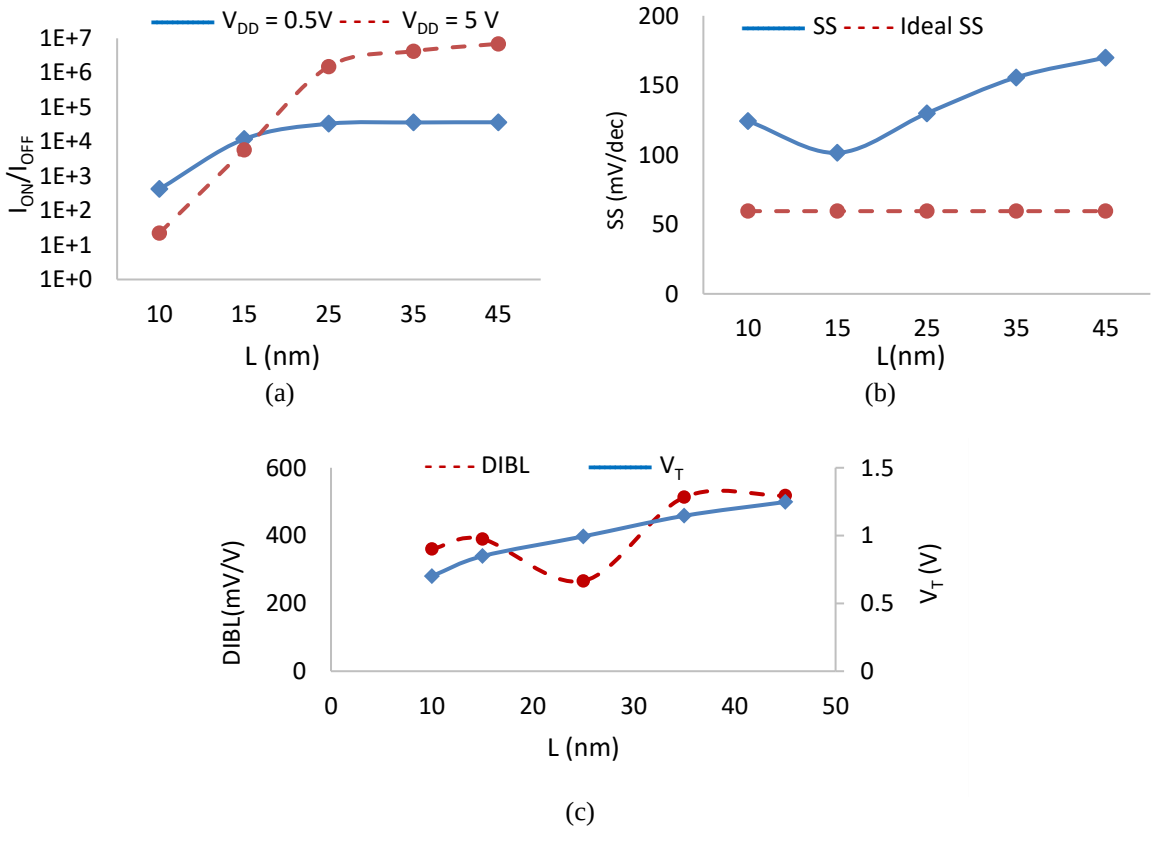

Figure 1. Impact of varying channel length of InAs-FinFET: I_{ON}/I_{OFF} ratio (a), SS value (b), V_T and DIBL (c)

Figure 1(b) presents the relation between channel length with (SS) of the IaAs-FinFET in this results the channel length was 10, 15, 25, 35 and 45 nm the W = 5 nm and T_{OX} = 2.5 nm. This figure illustrated that the value SS started with 124 mV/dec at L = 10 nm and at L = 15 nm this value to becomes the nearest value

to the ideal SS (101 mV/dec) were happen. The furthest value from the ideal SS (59.5 mV/dec) where the higher channel length at L = 45nm, SS = 169.9 mV/dec where the transistor is slower.

Figure 1(c) depicts the variation of both V_T and DIBL with different channel length value of V_T is proportional increases with channel length and reaches to 1.2 V at the longest channel. On the other hand, DIBL increases as channel length increased from 360 mV/V at L = 10 until it reached 517 mV/V at L = 45 nm leading to poor electrical conductivity due to the high DIBL value. According to the obtained characteristics in this scenario, the best performance in terms of both the I_{ON}/I_{OFF} ratio and SS value can be achieved in the case with 25 nm channel length. However, in the case with L = 45 nm, although I_{ON}/I_{OFF} ratio is the best, the SS value is too far from idle SS.

3.2. Impact of varying channel width

The scaling down of channel width W and its effect on the characteristics of InAs-FinFET have been studied in this scenario. The value of W was changed (5, 10, 15 and 20 nm) while L and T_{OX} were set to 40 nm and = 2.5 nm respectively. Figure 2 shows the electrical characteristics, I_{ON}/I_{OFF} ratio, SS, V_T, and DIBL correspondingly. The I_{ON}/I_{OFF} ratio for both voltages (V_{DD} = 5 V and V_{DD} = 5 V) in terms of the varying width of the channel are illustrated in Figure 2(a). Unlike the channel length scenario, the ratio is inversely proportional with channel width. Ratios for both voltages drop down to approximately 10^3 when W increases to 20 nm. In contrast, the highest I_{ON}/I_{OFF} ratio (more than 10^6) was achieved for V_{DD} = 5 V with the smallest channel width. Figure 2(b) depicts the variation of SS value with variable channel width. The closest SS to ideal value was achieved at W = 5 nm which is 124 mV/dec, then it was increased to 156 mV/dec at W = 20 nm.

Furthermore, the impacts of varying channel width on V_T and DIBL are illustrated in Figure 2(c). The voltage threshold is almost constant regardless channel width except in the first case with W = 5 nm, where V_T scores the highest value of 1.2 V. Finally, the DIBL decreased as channel width increased. InAs-FinFET achieved worst DIBL = 517 at W = 5 nm then DIBL characteristics improved and achieved the best value at W = 10 nm.

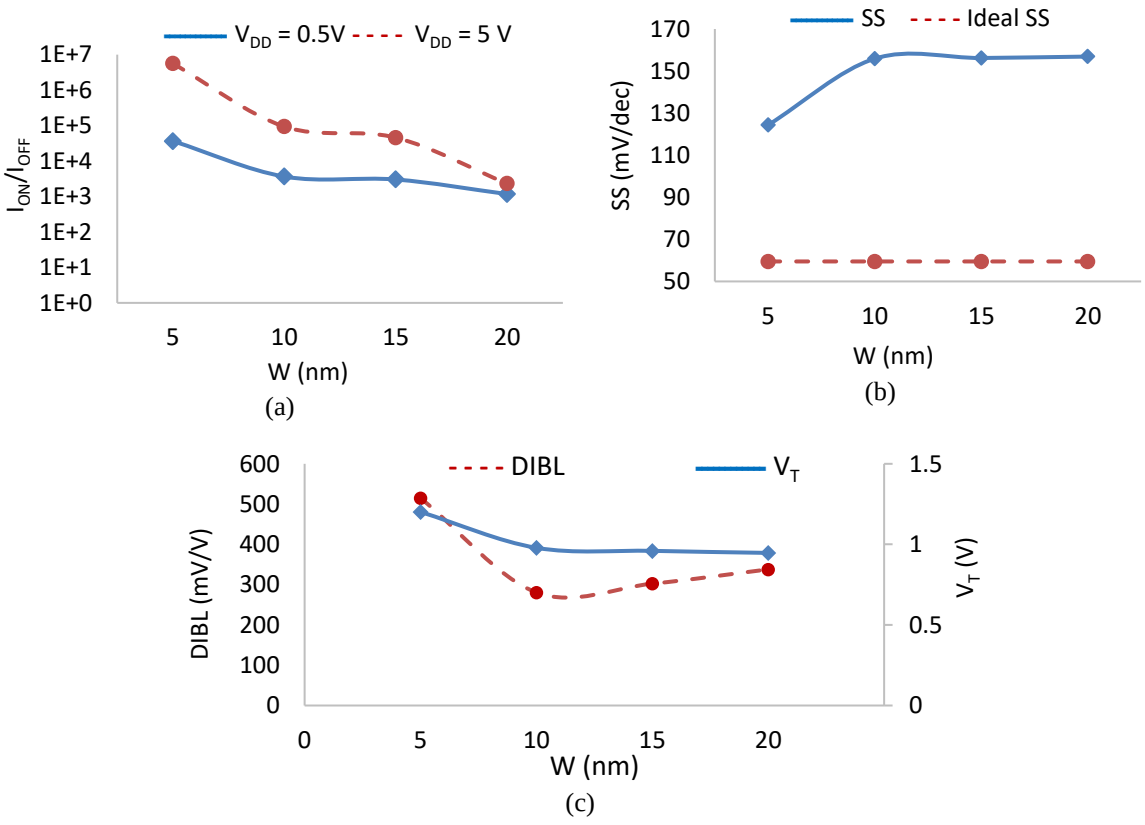

Figure 2. Impact of varying channel width of InAs-FinFET I_{ON}/I_{OFF} ratio (a), SS value (b), VT and DIBL (c)

3.3. Impact of varying channel oxide thickness

Figure 3 shows the channel oxide thickness variation in relation to the electrical characteristics of InAs-FinFET. For the simulation scenario carried out in Figure 4 channel oxide thickness, T_{OX} has been varied (1.5, 2.5, 5 and 7 nm), the channel length, L is kept constant at 40 nm, while as the channel width, W is kept fixed at 5 nm. Figure 3(a) illustrates the relation between the I_{ON}/I_{OFF} ratio with the channel oxide thickness which is consistent with previous channel width scenario. The maximum I_{ON}/I_{OFF} ratio (more than 10^6) with V_{DD} = 5 V was obtained at minimum T_{OX} = 1.5 nm and then decreased to 10^3 at T_{OX} = 7 nm. From the results shown in Figure 3(b), it is obvious that for a channel oxide thickness, T_{OX} = 7 nm the InAs-FinFET has shown better SS characteristics with the best SS value of 140 mV/dec compared to other T_{OX} values. Conversely, the farthest value from ideal SS occurred at T_{OX} = 5 nm where SS is 216 mV/dec. On the other hands, in Figure 3(c) displays channel oxide thickness versus both V_T and DIBL characteristics of InAs-FinFET. Both characteristics behave inconsistent manner with decreasing channel thickness, they decrease as T_{OX} decreased. The best V_T = 15.8 V at the highest T_{OX} value, whereas the best value of DIBL is 165 mV/V at oxide thickness of channel = 1.5 nm.

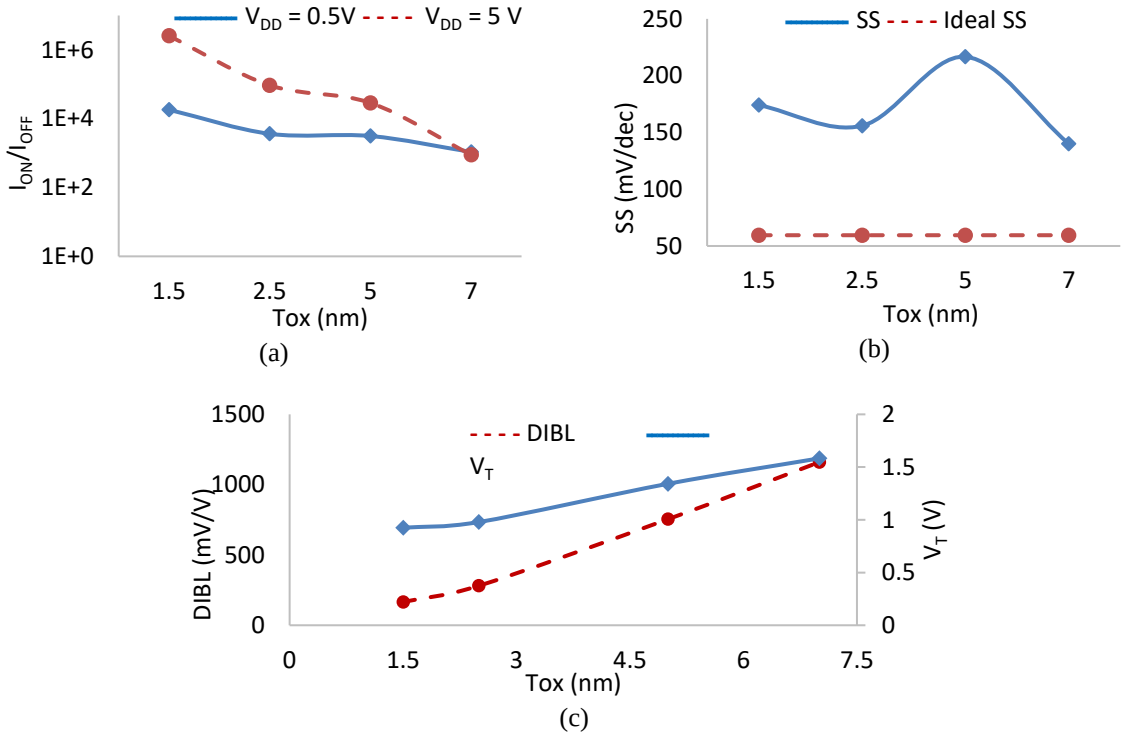

Figure 3. Impact of varying InAs-FinFET channel thickness: I_{ON}/I_{OFF} ratio (a), SS value (b), VT and DIBL (c)

3.4. Impact of varying scaling factor of channel dimensions

The scaling down of all channel dimensions at once can be achieved by applying scaling factor, K. All channel dimensions, length, width, and thickness will be scaling-down together by a factor (K). In order to study the electrical characteristics based on the scaling factor, the reference value of K is defined as "1" with its channel dimensions. All corresponding dimensions to the defend scaling factors are shown in Table 2.

Table 2 Channel dimensions based on scaling factor K

K	L (nm)	W (nm)	T_{OX} (nm)
1.00	40	20	6
0.5	20	10	3
0.25	10	5	1.5
0.125	5	2.5	0.75

Figure 4(a) shows the relation between the I_{ON}/I_{OFF} ratio with the scaling factor K from 0.125 to 1.00 The maximum value of I_{ON}/I_{OFF} ratio is higher than 10^4 which was attained at scaling factor K = 0.125 for both V_{DD} = 5 V and for V_{DD} = 5 V. The worst I_{ON}/I_{OFF} ratios, less than 10^2 occurred at the reference value of K = 1.00 for both V_{DD} values. Figure 4(b) shows the worst SS value (194 mV/dec) that obtained at K = 1.00 in contrast, the nearest value to the ideal SS (94 mV/dec) is obtained at K = 0.125. It can be noticed that, with increasing K, the SS value is increased significantly. The impact of changing Scaling Factor (K) on V_T and DIBL is illustrated in Figure 4(c). Where the highest value of V_T = 1.28 V is obtained at K = 1.00 compared to the lowest value, V_T = 0.7 V at K = 0.125 conversely, the DIBL value ranges from 376 mV/V at K = 0.125 to 934 mV/V at K = 1.00 and the best value is attained at K = 0.125 which is 195 mV/V. The summury of main finding for best L, W, T_{OX} and K were illustrated in Table 3, according to this table, in the first scenario, the best L was at 25nm, the best W in the second scenario was at 5nm, and the best T_{OX} in the third scenario was at range of 1.5 t0 2.5 nm, these dimentions represent the optimal channel dimensions for InAs-FinFET based on varying dimentions indevedually. In the last scenario, the propsed scalling factor achieved smaller limits with acceptable performance.

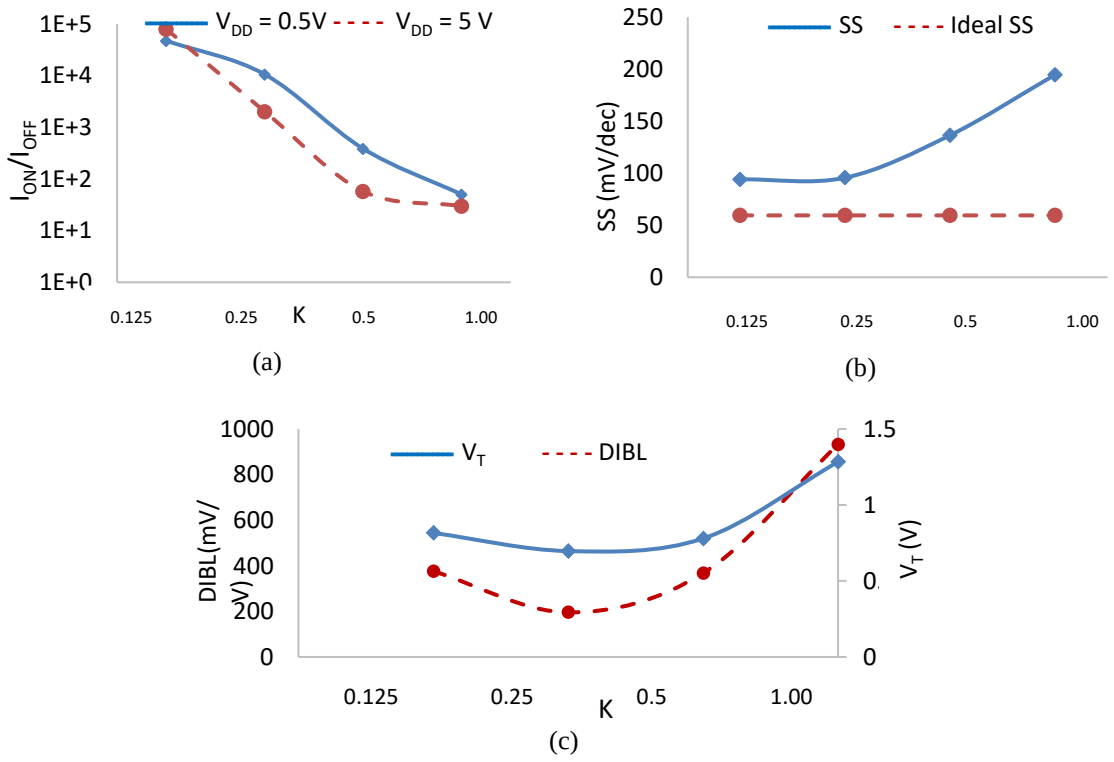

Figure 4. Impact of varying channel scaling factor of InAs-FinFET on I_{ON}/I_{OFF} ratio (a), SS value (b), V_T and DIBL (c)

Table 3. Channel summary of main findings for InAs-FinFET

Scenario	Characteristics	value
Scenario 1	I_{ON}/I_{OFF}	6.97×10^6
	SS(mV/dec)	101
L	Best L(nm)	25
Scenario 2	I_{ON}/I_{OFF}	5.58×10^7
	SS(mV/dec)	124
W	Best W(nm)	5
Scenario 3	I_{ON}/I_{OFF}	2.54×10^6
	SS(mV/dec)	155
T_{OX}	Best T_{OX} (nm)	1.5-2.5
Scenario 4	I_{ON}/I_{OFF}	**7.94×10^4**
	SS(mV/dec)	**94**
K	Best K	**0.125**

4. CONCLUSION

The effects of channel dimensions (length, width, and oxide thickness) on electric characteristics of InAs-FinFET were studied and analyzed using the MuGFET simulation tool. The highest I_{ON}/I_{OFF} ratio and the nearest SS to the ideal value were exploited to design the best nono-dimensions of InAs-FinFET. According to the obtained results from individual consideration scenarios, the highest L (= 32 to 40 nm), the lowest W (= 5 nm), and the lowest T_{OX} (= 1.5) nm, are the optimal channel dimensions for InAs-FinFET based on the considered parameters. Based on scaling factor (K), which shrinking all channel dimentions semoltenously, the optimal value was at K = 0.125, and it represents the lowest dimensions of the channel with the best performance in terms of the considered metrics.

ACKNOWLEDGEMENTS

The research was supported by the Ministry of Education Malaysia under Grant scheme No. FRGS/1/2018/TK04/UMP/02/11 (RDU190133).

REFERENCES

[1] R. Harikrishnan, "Amalgamating Nanoscience with Robotics Technology to Influence the Behaviour of Fractal Robots: A Focus on Future Applications," 2018.
[2] W. A. Jabbar, et al., "Energy and mobility conscious multipath routing scheme for route stability and load balancing in MANETs," *Simulation Modelling Practice and Theory*, vol. 77, pp. 245-271, 2017.
[3] A. Mahmood, et al., "Electrical characterization of Ge-FinFET transistor based on nanoscale channel dimensions," *Journal of Nano- and Electronic Physics*, vol. 11, 2019.
[4] W. A. Jabbar, et al., "MEQSA-OLSRv2: A Multicriteria-Based Hybrid Multipath Protocol for Energy-Efficient and QoS-Aware Data Routing in MANET-WSN Convergence Scenarios of IoT," *IEEE Access*, vol. 6, pp. 76546-76572, 2018.
[5] M. A. Riyadi, et al., "Influence of Gate Material and Process on Junctionless FET Subthreshold Performance," *International Journal of Electrical & Computer Engineering*, vol. 6, 2016.
[6] A. Rachakh, et al., "A Novel Configuration of A Microstrip Power Amplifier based on GaAs-FET for ISM Applications," *International Journal of Electrical and Computer Engineering*, vol. 8, pp. 3882, 2018.
[7] A. A. Almohammedi, et al., "An accurate performance analysis of hybrid efficient and reliable MAC protocol in VANET under non-saturated conditions," *International Journal of Electrical and Computer Engineering*, vol. 7, pp. 999, 2017.
[8] Y. Hashim, "A New Approach for Dimensional Optimization of Inverters in 6T-Static Random-Access Memory Cell Based on Silicon Nanowire Transistor," *Journal of Nanoscience and Nanotechnology*, vol. 17, pp. 1061-1067, 2017.
[9] A. Arjimand and M. Prashant, "An Analytical Modeling of Drain Current for Single Material Surrounded Gate Nanoscale SOI MOSFET," *Journal of Nano- and Electronic Physics*, vol. 10, pp. 04012-1-04017-5, 2018.
[10] A. F. Roslan, et al., "30nm DG-FinFET 3D Construction Impact Towards Short Channel Effects," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 12, pp. 1358-1365, 2018.
[11] W. A. Jabbar, et al., "Performance evaluation of MBA-OLSR routing protocol for MANETs," *Journal of computer networks and communications*, vol. 2014, 2014.
[12] A. A. Almohammedi, et al., "Evaluating the Impact of Transmission Range on the Performance of VANET," *International Journal of Electrical and Computer Engineering*, vol. 6, pp. 800, 2016.
[13] Z. R. Fatima and B. Bouazza, "Effects of High-k Dielectrics with Metal Gate for Electrical Characteristics of SOI TRI-GATE FinFET Transistor," *Journal of Nano- and Electronic Physics*, pp. 04037-1-04037-4, 2016.
[14] W. A. Jabbar, et al., "Design and Implementation of IoT-Based Automation System for Smart Home," *2018 International Symposium on Networks, Computers and Communications (ISNCC)*, pp. 1-6, 2018.
[15] M. S. Mobarakeh, et al., "Theoretical logic performance estimation of Silicon, Germanium and SiGe Nanowire Fin-field effect transistor," *Superlattices and Microstructures*, 2018.
[16] S. Rai, et al., "Modelling, Design, and Performance Comparison of Triple Gate Cylindrical and Partially Cylindrical FinFETs for Low-Power Applications," *ISRN Electronics*, vol. 2012, 2012.
[17] J. Alvarado, et al., "SOI FinFET compact model for RF circuits simulation," *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2013 IEEE 13th Topical Meeting on*, pp. 87-89, 2013.
[18] Y. Hashim, "Optimization of Resistance Load in 4T-Static Random-Access Memory Cell Based on Silicon Nanowire Transistor," *Journal of nanoscience and nanotechnology*, vol. 18, pp. 1199-1201, 2018.
[19] W. A. Jabbar, et al., "Framework for enhancing P2P communication protocol on mobile platform," *Proceedings of the ICIA*, vol. 12, 2012.
[20] T. A. Bhat, et al., "Study of Short Channel Effects in n-FinFET Structure for Si, GaAs, GaSb and GaN Channel Materials," *Journal of Nano- and Electronic Physics*, 2015.
[21] Y. Hashim, "A Review on Transistors in Nano Dimensions," *International Journal of Engineering Technology and Sciences (IJETS)*, vol. 4, pp. 8-18, 2015.
[22] G. Moore, "Moore's law," *Electronics Magazine*, vol. 38, pp. 114, 1965.

[23] T. Elayampalayam, "Design of a Reduced Carry Chain Propagation Adder Using FinFET," *Asian Journal of Information Technology*, vol. 15, pp. 1670-1677, 2016.
[24] S. Kim, et al., "MuGFET," 2008.
[25] M. Rahmani, et al., "Trilayer graphene nanoribbon field effect transistor analytical model," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol. 12, pp. 2530-2535, 2014.

BIOGRAPHIES OF AUTHORS

Ahmed Mahmood received his Bachelor of Science in Laser & Optoelectronics Engineering from University of Technology, Baghdad, Iraq, in 2005. Presently, the author is a Master candidate majoring in Advanced Electronics And Automation at Facylty of Engineering Technology, Universiti Malaysia Pahang (UMP). He is currently undertaking his research on Nano Electronics in particular FinFET transistors. His research interests include Nanotechnology, and advanced electronics.

Waheb A. Jabbar received the B.Sc. in Electrical Engineering from the University of Basrah, Iraq, in 2001, the M.Eng. in Communication & Computer and the Ph.D. in Electrical, Electronics, and System Engineering from Universiti Kebangsaan Malaysia (UKM), Bangi, Selangor, Malaysia, in 2011 and 2015 respectively. He is currently a Senior Lecturer in the Faculty of Engineering Technology, Universiti Malaysia Pahang (UMP), Gambang, Pahang, Malaysia. His research interests include Routing Protocols in Ad Hoc Networks, Mobile Communications and Wireless Networking. He also has a keen interest in Nano electronics, Internet of Things applications, and Smart City.

Yasir Hashim received the B.Sc. and Master of Engineering in Electronics and Communications Engineering from the University of Mosul, Mosul, Iraq, in 1991 and 1995 respectively. He completed the Ph.D. in Electronics Engineering-Micro and Nanoelectronics from Universiti Science Malaysia (USM), Penang, Malaysia, in 2013. He is currently a Senior Lecturer in the Faculty of Engineering, Ishik University, Erbil-Kurdstan, Iraq. His research interests include Microelectronics and Nanoelectronic: Nanowire transistors, FinFET transistor, Multistage Logic Nano-inverters.

Hadi Manap was born in Kuantan, Malaysia in 1973. He received his first degree in Mathematics and Physics from University of Malaya in 1998. Then he got his Masters degree in Process Plant Management from University of Technology, Malaysia in 2004 and appointed as a teaching staff at Faculty of Electrical & Electronic Engineering, University Malaysia Pahang (UMP). He was sponsored by UMP for Ph.D. studies in the University of Limerick under the supervision of Prof Elfed Lewis and he was awarded his Ph.D. in 2011. Currently he is a senior lecturer in the Faculty of Engineering Technolgy, UMP.