

## PID controller using rapid control prototyping techniques

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### ABSTRACT

To analyze the performance of the PID controller in a buck type converter implemented in real time. We begin by designing a continuous controller using the analytical method for calculating PIDs. Pulse width modulation is then used and bifurcation diagrams analyzed to reveal some problems of switching and sampling time. The model converter is then implemented with a PID controller in dSPACE. The experimental results provide detailed requirements of sampling frequency and switching speed, and show the performance of the PID controller. Converters are used in power generation solar systems and commuted power sources for feed telecommunication devices, smart grids, and other applications.

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## 1. INTRODUCTION

The buck converter is a switching power supply with two semiconductor devices [1], a transistor ( $Q$ ) and diode ( $D$ ), an inductor ( $L$ ), an output capacitor ( $C$ ), and its respective load as shown in Figure 1. This system converts an unregulated DC voltage to another regulated lower voltage. The transistor switches the input power  $E$  by pulse width modulation (PWM) to feed the filter  $LC$ . The diode conducts when the transistor is off if there is positive current in the coil. The inductor does not allow rapid changes in current and the capacitor does not support abrupt changes of voltage, creating between them a low pass filter. A MOSFET is used for switching, thus, the control technique must determine the OFF and ON switch times. This control form is known as pulse width modulation (PWM) [2]-[6].

Figure 2 shows a block diagram of the system under study. This system is divided into two major subgroups: the hardware that includes the physical and electronic components and the software implemented on a dSPACE, which performs the signal acquisition and implementation of PID control technique. The hardware consists of a sensors (high-impedance resistors connected in parallel) to measure the  $V_C$  state variable (capacitor voltage). The converter's switch is handled from the control and development card through the PWM and the pulse is opto-isolated through fast optocouplers. The digital part is developed in the control and development card dSPACE DS1104 [7], where the PID control technique is implemented. PID was used due to its easy availability and compatibility with some series of PLCs, DCS software, Advantech 6022, and popular software such as LabView and MATLAB [8], [9]. The card is programmed using the MATLAB/Simulink® platform and has a display interface called "ControlDesk." The controller is implemented in Simulink® and downloaded to the DSP to operate at a given frequency [10]. The state variable

comes to the controller through the 12-bit ADC input with a sampling rate set for the experiment at 10 kHz and then 30 kHz. The controller parameters are set through variable gain blocks because they were tuned in real time. At each sampling period, the controller calculates the duty cycle in real time and its equivalent in the PWM control switch.

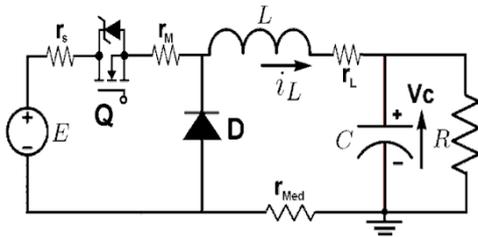


Figure 1. Schematic of buck converter model

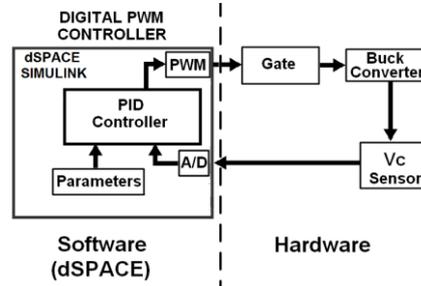


Figure 2. Block diagram of the proposed system

This article is intended for the digital PWM approach, which presents rich nonlinear dynamics and has the following advantages: immunity to analog component variations; faster process design; low sensitivity to changes in parameters; programmability; allows reduction or elimination of passive external components; allows calibration of protection algorithms; and supports digital system interfaces for implementing nonlinear control techniques [11]–[16]. However, the DPWM also has disadvantages as it is affected by two limitations: quantization effects [12], [13] and delays in the control loop [17], [18].

## 2. BUCK CONVERTER MODEL

$$E = (r_{int} + r_L)i_L + Li_L + V_C,$$

Where  $r_{int}$  is the internal resistance of the MOSFET ( $r_M$ ) plus the resistance source ( $r_s$ ) and the resistance coil ( $r_L$ ) plus the shunt resistor's resistance used for the current measure ( $r_{Med}$ ) as shown in Figure 1. By summation of currents in the capacitor's node we obtain

$$C\dot{V}_C = i_L - \frac{V_C}{R}.$$

Solving and simplifying gives

$$i_L = -\frac{r_{in} + r_L}{L}i_L - \frac{1}{L}V_C + \frac{E}{L},$$

$$\dot{V}_C = \frac{1}{C}i_L - \frac{1}{RC}V_C.$$

Converting to matrix form gives

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_C \end{bmatrix} = \begin{bmatrix} -\frac{r_{int} + r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{E}{L} \\ 0 \end{bmatrix},$$

$$y = [0 \quad 1] \begin{bmatrix} i_L \\ V_C \end{bmatrix}.$$

Converting to state variables and making  $a = \frac{r_{int}+r_L}{L}$ ,  $b = \frac{1}{L}$ ,  $c = \frac{1}{C}$ ,  $d = \frac{1}{RC}$ , and maintaining signs gives

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \end{bmatrix} = \begin{bmatrix} -a & -b \\ c & -d \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} + \begin{bmatrix} E \\ L \\ 0 \end{bmatrix}, \tag{1}$$

$$y = [0 \quad 1] \begin{bmatrix} X_1 \\ X_2 \end{bmatrix}.$$

If the switch stays OFF ( $u=0$ ), then the equation becomes  $\dot{X} = AX$  because it does not take into account the diode's voltage.

In the case where the switch is closed, we find the transfer function using

$$G(s) = \frac{Y(s)}{U(s)} = C(SI - A)^{-1}B,$$

which yields

$$G(s) = \frac{\frac{E}{L}}{s^2 + (a+d)s + (ad+bc)}, \tag{2}$$

In (2), the following values will be replaced to find the system's response:

$$\begin{aligned} E &= 40 \text{ V}, C = 46.27 \mu\text{F} \\ R &= 39.3 \Omega, r_{int} = 0.688 \Omega \\ L &= 2.47 \text{ mH}, r_L = 1.345 \Omega \end{aligned}$$

$$G(s) = \frac{8.739e06}{s^2 + 1372s + 9.192e06} \tag{3}$$

The poles for (3) are

$$-681 \pm j2953.$$

The root locus is shown Figure 3. Therefore, the system is stable with the values used for constants and it is underdamped. The response to stepped  $E$  volts can be seen in Figure 4, which shows an overshoot that must be reduced and a steady-state error of about 2 volts, indicating the system is underdamped. In low-power buck converters, such as computer sources, it is usual to find a zener diode and transistor-based regulation of the converter output. This technique has the advantage of avoiding the use of control; however, it has the disadvantage of increasing the probability of failure on points where it handles the power output. To obtain the desired voltage with proper MOSFET handling and without adding elements that may fail in the converter output is the goal of implementing a controller.

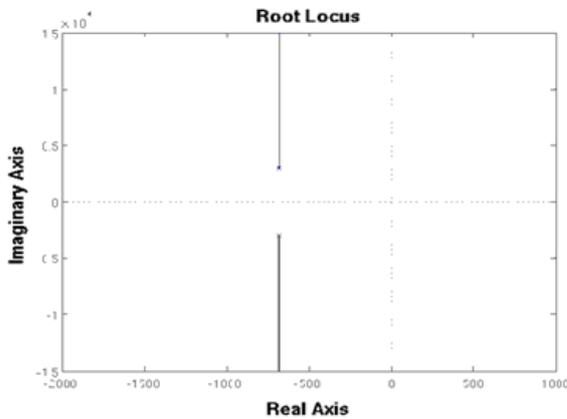


Figure 3. Root locus

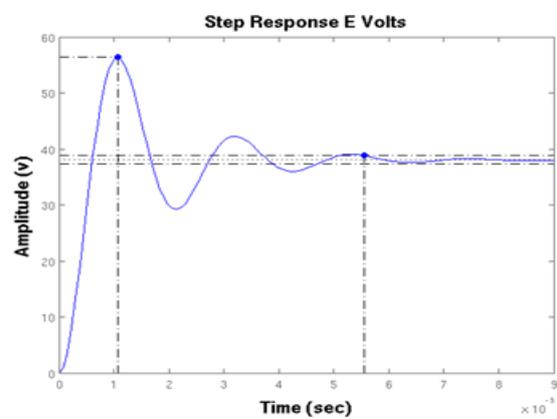


Figure 4. Step response

### 3. CONTINUOUS PID CONTROLLER

The method used is known as the “analytical method.” We start from the desired behavior as determined by the second-order canonical equation, which should match the characteristic equation of the closed-loop system with PID, to find the constants  $Kp$ ,  $Kd$ , and  $Ki$ .

#### 3.1. Desired response

$$ts = 2.5 \text{ ms}, Mp = 10\% = 0.1$$

$$\zeta = \sqrt{\frac{\ln(Mp)^2}{\pi^2 + \ln(Mp)^2}} = \sqrt{\frac{\ln(0.1)^2}{\pi^2 + \ln(0.1)^2}} = 0.591$$

$$\sigma = \frac{4}{ts} = \frac{4}{2.5 \text{ ms}} = 1600$$

$$\sigma = \zeta \cdot \omega_n \Rightarrow \omega_n = \frac{1600}{0.591} = 2707.27$$

Second-order canonical equation (*desired behavior*):

$$\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\frac{2707^2}{s^2 + 3200s + 2707^2}$$

Poles on:

$$-1.600 \pm j2.183$$

#### 3.2. Closed loop with unknown PID constants

Replacing the parameters in the transfer function and making a change of variables  $m = 8739229$ ,  $n = 1372$ , and  $p = 9191377$ , we must close the loop with unknown PID. Block diagram as shown in Figure 5.

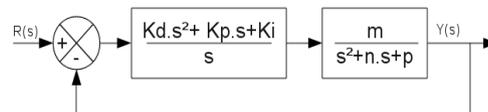


Figure 5. Block diagram

This gives the transfer function with the unknown constants of PID:

$$Glc(s) = \frac{mKds^2 + mKps + mKi}{s^3 + (n + mKd)s^2 + (p + mKp)s + mKi}$$

However, before matching the characteristic equations, we must first increase the degree of the second-order characteristic equation. This is achieved by adding a remnant pole to the characteristic equation so as to not affect the desired behavior; in this case, that is five times away from the dominant poles. This modification usually affects the amplitude, but the behavior of the canonical system is preserved:

$$(s + 8000)(s^2 + 3200s + 2707^2).$$

Thus, it is now possible to match the coefficients:

$$(n + mKd) = 11200 \Rightarrow Kd = 0.0011245,$$

$$(p + mKp) = 32929310 \Rightarrow Kp = 2.7162,$$

$$(mKi = 5) = 863448e10 \Rightarrow Ki = 6709.$$

Replacing these constants in the closed-loop transfer function, the simulation is then performed with a step value of  $E$  volts.

Figure 6 shows that the controlled system does not reach the desired overshoot; however, it is normal to do some tuning, preferably when the controller is already modulated by the PWM so as to avoid double tuning. The settling time and the steady-state error are the desired outcomes.

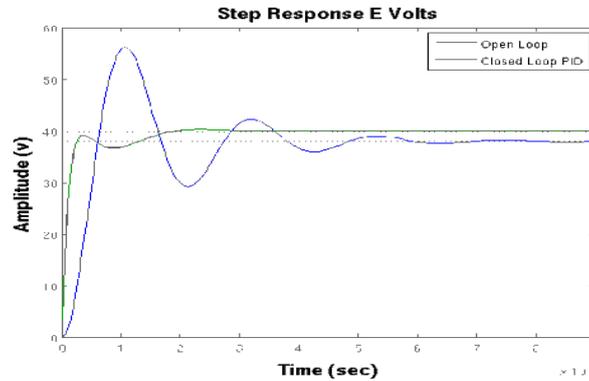


Figure 6. Comparison of step response in open-and closed-loop systems with PID

**4. DISCRETE TIME SYSTEM**

For a continuous time, system, the general solution is given by

$$X(t) = e^{A(t-t_0)}X(0) + \int_{t_0}^t e^{A(t-\tau)}Bu(\tau)d\tau.$$

Therefore, the solution in discrete time form is given by

$$X(k+1)T = e^{AT}X(kT) + \int_0^T e^{A(T-\tau)}Bu(kT)d\tau. \tag{4}$$

The solution of Equation (4) is obtained as

$$X(k+1)T = e^{AT}X(kT) + (e^{AT} - I)A^{-1}Bu(kT).$$

Making  $Ad = e^{AT}$  y  $Bd = (e^{AT} - I)A^{-1}B$ , the solution can be presented as

$$Ad.X(kT) + Bd.u(kT) \tag{5}$$

Then, the solution of  $e^{AT}$  is

$$C^{-1}(SI - A)^{-1} = \begin{pmatrix} \frac{s+d}{s^2+(a+d)s+(ad+bc)} & -\frac{b}{s^2+(a+d)s+(ad+bc)} \\ \frac{c}{s^2+(a+d)s+(ad+bc)} & \frac{s+a}{s^2+(a+d)s+(ad+bc)} \end{pmatrix} \tag{6}$$

From (6) and applying Laplace's anti-transformation, we obtain the matrix  $e^{AT}$ :

$$e^{AT} = \begin{pmatrix} Term2 + dTerm1 & -bTerm1 \\ cTerm1 & Term2 + aTerm1 \end{pmatrix} \tag{7}$$

where

$$Term1 = \frac{e^{-\zeta\omega_n t} \sin(\omega_d t)}{\omega_d}, \quad Term2 = -\frac{e^{-\zeta\omega_n t} \sin(\omega_d t) - \phi}{\sqrt{1-\zeta^2}},$$

and

$$\omega_d = \omega_n \sqrt{1-\zeta^2}; \quad \phi = \tan^{-1} \frac{\sqrt{1-\zeta^2}}{\zeta}.$$

At this point, we prove that  $e^{AT}$  evaluated at  $t = 0$  is equal to the identity matrix.

Knowing  $e^{AT}$ , an algorithm was implemented in MATLAB® to produce the discrete equivalent shown in Figure 7. The continuous time system has  $T_s = 5.9$  ms, so we can choose a sampling rate  $T = 50$   $\mu$ seg. Initializing the necessary variables, we obtain the output shown in Figure 7. Thus, we can see how the discrete equivalent is very close to the real equivalent.

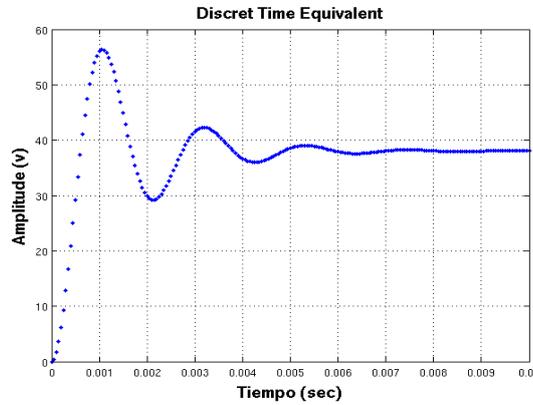


Figure 7. Discrete time equivalent

### 5. PID MODULATED BY PWM

The found constants will be used in this controller. Initializing variables and respective vectors to zero the output ( $V_C$ ) (load voltage) shown in Figure 8. We observe that the overshoot appears even higher than previously estimated; to reduce the overshoot, we follow Table 1 taken from [13], showing an online tuning form of PID, depending on the output characteristics required by the user. This table is valid as long as the constants to tune are calculated with a known method. Therefore, from the values that we have calculated, we reduce  $K_i = 2400$  to obtain an overshoot close to zero as shown in Figure 9, which is very convenient for such converters.

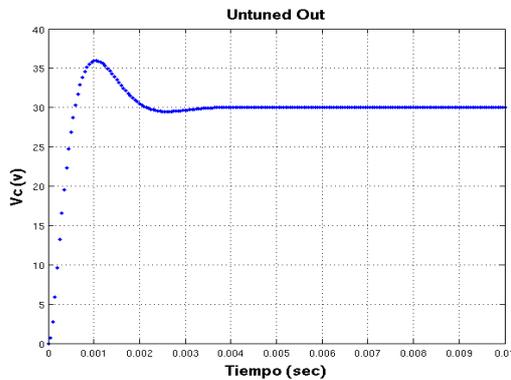


Figure 8. PID with PWM

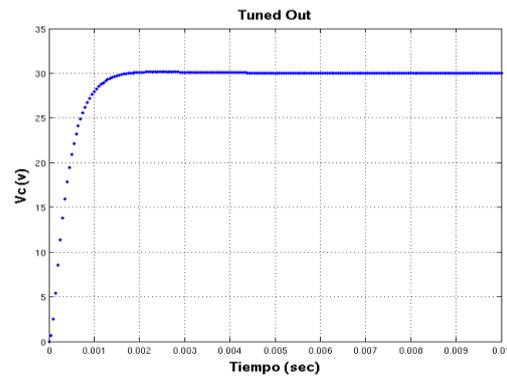


Figure 9. Tuned output ( $V_C$ ) using Table 1

Table 1. Effects of Independent  $P$ ,  $I$ , and  $D$  Tuning

PID	Rise Time	Overshoot	Settling Time	Steady Stage Error	Stability
$\uparrow K_p$	Decrease	Increase	Small increase	Decrease	Degrade
$\uparrow K_i$	Small decrease	Increase	Increase	Large decrease	Degrade
$\uparrow K_d$	Small decrease	Decrease	Decrease	Minor change	Improve

### 6. BIFURCATION DIAGRAMS

Bifurcation diagrams are defined as qualitative and quantitative variations of the system’s dynamics in front of the variation of parameters that can influence the stability of the system and characteristics of the output, among other issues.

The bifurcation diagram is a tool to analyze the dynamic system and provides information on its limits of stable operation. For this system, only the constant  $K_p$  has to be varied as this affects the others. This requires the industrial form of PID:

$$PID = k_p \left( 1 + \frac{\tau_i}{s} + \tau_d s \right).$$

**6.1.  $V_c$  and  $D$  bifurcation diagrams with  $K_p$  variations**

Figures 10 and 11 show that the operating range of  $K_p$  has an upper limit of 19 units apx before the system becomes chaotic.

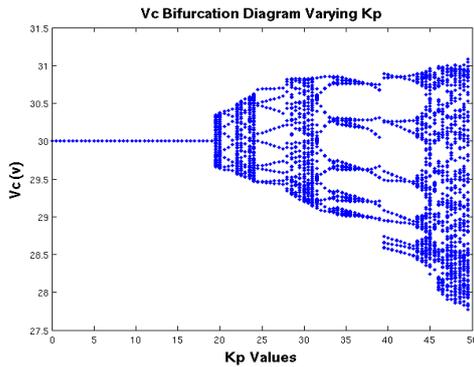


Figure 10.  $V_c$ 's bifurcations

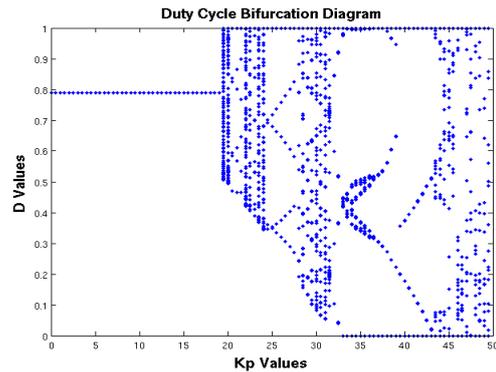


Figure 11.  $D$ 's bifurcations

**6.2.  $V_c$  and  $D$  bifurcation diagrams with varying  $T$**

Figure 12 shows that for small values of  $T$  (sampling period), the system has a one periodic wave for high frequencies; however, by increasing the sampling period equal to the switching period (around 110  $\mu$ sec), the systems begins to turn chaotic.

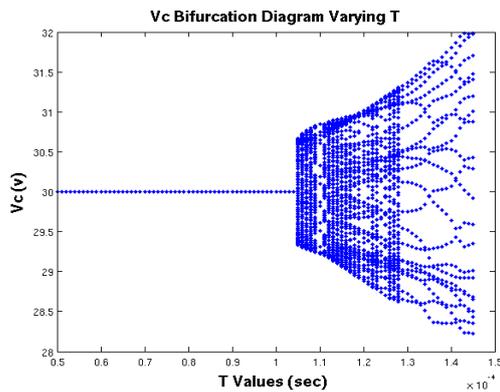


Figure 12.  $V_c$ 's bifurcation diagram with varying  $T$

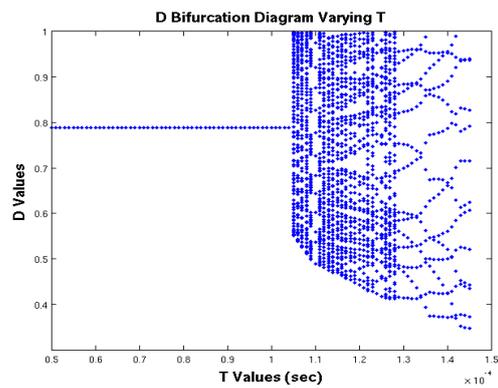


Figure 13.  $D$ 's bifurcation diagram with varying  $T$

**7. MATLAB/SIMULINK® SIMULATION**

The next simulation performed in simulink moves us closer to real-time implementation performed in dSPACE. Figures 14 and 15, respectively, show the circuit diagrams and elements used. Figure 16 displays the output in open- and closed-loop systems with PID. Reducing the sampling rate to half causes the signal to lose symmetry because it receives fewer sampling points and, therefore, the integration process struggles as it adds more than needed or rests more than needed, for the same reason. This explains the strong oscillations seen in Figure 17. This effect is accentuated in the implementation.

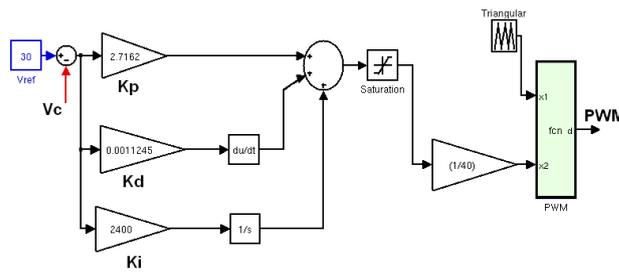


Figure 14. PID and PWM schema

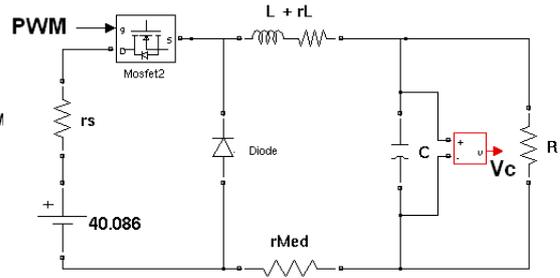


Figure 15. Buck converter

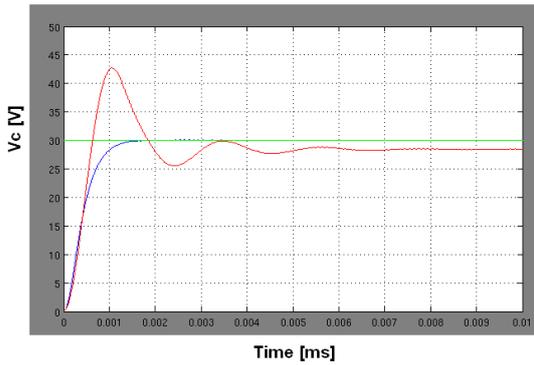


Figure 16.  $V_c$  output in open- and closed-loop

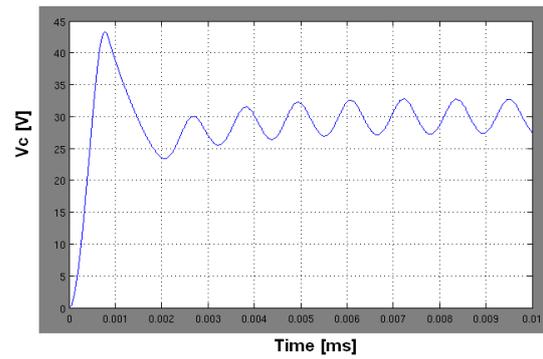


Figure 17.  $V_c$  output with a minor sample frequency systems with PID

### 8. EXPERIMENTAL RESULTS

For real-time implementation, the control and development card dSPACE was used. The converter's PID controller was implemented in simulink as diagrammed in Figure 18, where it controls the controller implemented on hardware through the PWM generation block.

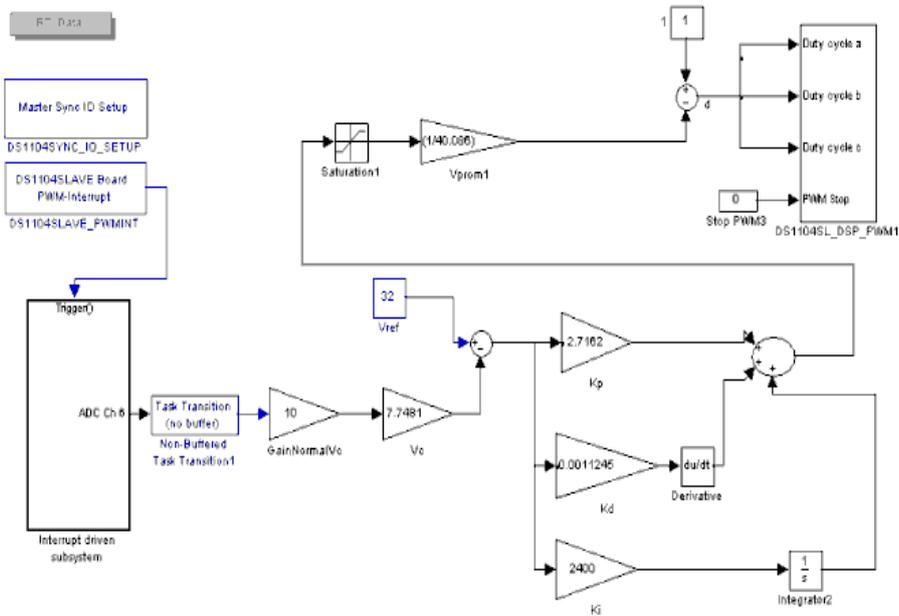


Figure 18: Rapid control prototyping to control the buck converter

The results presented in this section were obtained with the experimental prototype and the parameters defined in Table 2. By changing the reference voltage to 10 V, 20 V, and 30 V, and varying the sampling and switching frequency, we show that the real system is much more sensitive to a low sampling rate. Figure 19 corresponds to a sampling frequency of 10 kHz. Increasing the sampling frequency three times (30 kHz) in Figure 20 results in a little improvement in the regulated signal  $V_C$  and, especially, a reduction in the sound produced by the inductor due to the switching frequency growth of the transistor.

By increasing significantly the value of the capacitor to 376  $\mu\text{F}$  as shown in Figure 21, we improve the converter's filtering and find a better answer with a lower steady-state error, even for the design parameters shown in Table 2. The reason is that more capacity filters higher frequencies and, therefore, the regulation is better, thus reducing considerably the system's chaos. It can be seen in Figures 22 and 23 that if we make instant load changes going from 14.59  $\Omega$  to 39.3  $\Omega$  with a capacitor of 376  $\mu\text{F}$  and switching to 10 kHz, then the system regulates too well with errors less than 2%; hence, not only the good performance of the PID controller must be considered.

Table 2. Experimental Prototype Data

Parameter	Value
$R$ :	Load resistance 39.3 $\Omega$
$C$ :	Capacitance 46.27 and 376 $\mu\text{F}$
$L$ :	Inductance 2.473 mH
$r_{int}$ :	Internal resistance of the source 0.688 $\Omega$
$r_L$ :	Internal resistance of the inductor 1.345 $\Omega$
$E$ :	Input voltage 40.086 V
$f_c$ :	Switching frequency 10 kHz and 30 kHz
$f_s$ :	Sampling frequency 10 kHz and 30 kHz
$K_p$ :	Proportional gain 2.7162
$K_d$ :	Derivative gain 0.0011245
$K_i$ :	Integral gain 2400

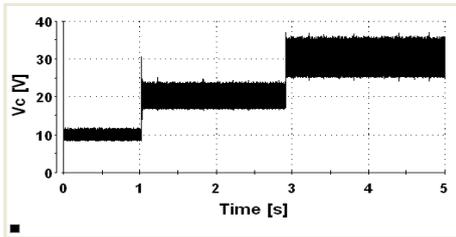


Figure 19.  $V_C$  output with  $C = 46 \mu\text{F}$ ,  $V_c$  at 10 kHz

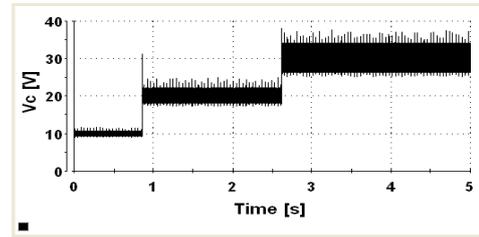


Figure 20.  $V_C$  output with  $C = 46 \mu\text{F}$ ,  $V_c$  at 30 kHz

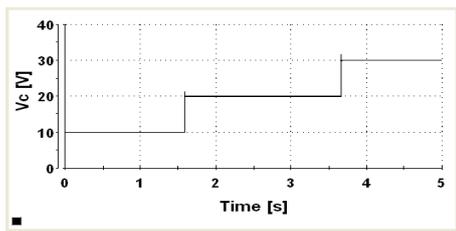


Figure 21.  $V_C$  output with  $C = 376 \mu\text{F}$  at 10 kHz

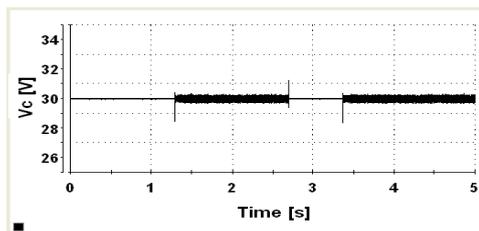


Figure 22.  $V_C$  output with load changes  $R$  with  $C = 376 \mu\text{F}$

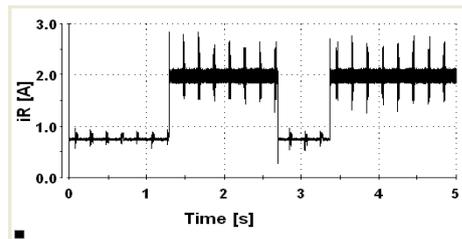


Figure 23.  $I$  load  $i_R$  with load changes  $R$  with  $C = 376 \mu\text{F}$

## 9. CONCLUSIONS

Because the increased value of the capacitor produced a substantial improvement in the system, it is necessary to propose a detailed study of the buck converters currently on the market in order to determine and compare which and what values of their elements are most appropriate to apply with different control techniques. It is likely that the implemented converter does not have the best features to adequately respond to PID control. The PID controller in the continuous case shows good performance in terms of regulating output voltage ( $V_C$ ). In some systems, a continuous PID control can react in a way and when is modulated by PWM change substantially; therefore, we should not assume that what is found in continuous time can be applied without restrictions in discrete time. The switching and sampling frequencies affect a major proportion of the integral because it needs to add the highest possible amount of points to successfully complete the integration process. Having hardware that supports high sampling and switching frequencies is a very important factor when implementing a system. For the implemented converter, the PID controller did not respond in the best way. It is necessary to filter or remove the derivative and select appropriate sampling and switching frequencies.

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