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Energy optimization of 6T SRAM cell using low-voltage and high-performance inverter structures

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ABSTRACT

The performance of the cell deteriorates, when static random access memory (SRAM) cell is operated below 1V supply voltage with continuous scale down of the complementary metal oxide semiconductor (CMOS) technology. The conventional 6T, 8T-SRAM cells suffer writeability and read static noise margins (SNM) at low-voltages leads to degradation of cell stability. To improve the cell stability and reduce the dynamic power dissipation at low- voltages of the SRAM cell, we proposed four SRAM cells based on inverter structures with less energy consumption using voltage divider bias current sink/source inverter and NOR/NAND gate using a pseudo-nMOS inverter. The design and implementation of SRAM cell using proposed inverter structures are compared with standard 6T, 8T and ST-11T SRAM cells for different supply voltages at 22-nm CMOS technology exhibit better performance of the cell. The read/write static noise margin of the cell significantly increases due to voltage divider bias network built with larger cell-ratio during read path. The load capacitance of the cell is reduced with minimized switching transitions of the devices during high-to-low and low-to-high of the pull-up and pull-down networks from VDD to ground leads to on an average 54% of dynamic power consumption. When compared with the existing ones, the read/write power of the proposed cells is reduced to 30%. The static power gets reduced by 24% due to stacking of transistors takes place in the proposed SRAM cells as compare to existing ones. The layout of the proposed cells is drawn at a 45-nm technology, and occupies an area of 1.5 times greater and 1.8 times greater as compared with 6T-SRAM cell.

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1. INTRODUCTION

SRAM technology is more suitable for high-speed and low-power applications like processors, computing units and other sophisticated devices, scientific and industrial subsystems, modern appliances, automotive electronics, mobile phones etc [1], [2]. Low-Power, Low-Voltage stability with high packaging density has represented the fundamental topics of the recent decade regarding SRAM outlines [3]. The reduction of the supply voltage offers the greatest energy efficiency since the dynamic power has been quadratic function of voltage [4]. As CMOS technology relies on scaling, both the supply voltage and the threshold voltage of the MOSFET usually needed to maintain normal performance. Therefore, for low energy applications, the leakage energy is invariably associated with the minimum threshold voltage, viz., VtnMOS = 0.31 V and Vtpmos = -0.29 V of the MOSFET. Thus, speed benefits little from innovation perspective of the size [5].

Lower supply voltage increments parametric (access, disturbance, and write) faults in the SRAM array, which are caused by fabrication and inherently different varieties of elements in a gadget. Thus, a higher bit error rate of memory with voltage scaling occurs. In the wake of other effects such as narrow width, Soft Error Rate (SER), temperature, process variation and resistance to parasitic transistors, the scaling of SRAMs turn out to be progressively troublesome [6]. The past industry evolved patterns to investigate the bigger cell and more colorful SRAM hardware styles are in the scaled environments [7]. Some of the existing architectures of SRAM cell are 6T, 7T, 8T, 9T, 10T [1], [3], 11T [5] and 13T [6]. The 6T- SRAM cell suffers from read/write access distribution, scaling, soft errors and stability of the cell diminishes at low-voltage. The disadvantages of the existing 8T, 9T, 10T and 13T SRAM memory cells are; i) It requires more than 1-word line (WL) and 2-bit lines (BLs) for an operation of the cell. More number of WLs and BLs required for read/write operations of the cell leads to the increased internal wiring capacitance and resistance. The performance of the cell is degraded with increased propagation delay. ii) Increased cell area. iii) Continuous switching transitions during high-to-low and low-to-high of the pull-up network (PUN) and the pull-down network (PDN) gives rise to charging and discharging of the load capacitance (CL) lead to dynamic power dissipation.

In this paper, we present four SRAM cells improving both read/write access distribution and cell stability at low-voltage based on high-performance inverters. The organization of the paper is as follows: Four SRAM cell configurations based on proposed inverter structures, aimed for less energy consumption using voltage divider bias current sink/source inverter and NOR/NAND gate using a Pseudo-nMOS inverter explained in section 2 require 1-word line and 2-bit-lines during read/write operations as 6T-SRAM cell. Simulation results and their comparison are presented in section 3, which determines the read/write access time, energy and stability of the cell at low-voltage. Section 4 ended up with a conclusion.

2. PROPOSED INVERTER STRUCTURES FOR 6T-SRAM CELL

2.1. SRAM cell using NOR gate with respect to a pseudo-nMOS inverter (NOR-8T)

The In conventional, SRAM cell is designed by two pass transistors and a flip-flop formed by two cross-coupled inverters [8]. A flip-flop is designed for as shown in Figure 1 using NOR gate with respect to pseudo- nMOS inverter require 8 transistors to build a 1-bit SRAM cell. Transistors M1, M5, M6 and M2, M7, M8 form two cross-coupled pseudo-nMOS inverters using NOR gate as a flip-flop. The PDN is implemented with NOR gate using nMOS logic. The PUN is a pMOS transistor. The gate terminal is always connected to the ground so that the pMOS transistor is always in ON [9] state. M1, M2 are the load transistors and M5, M6, M7, M8 are the storage transistors, respectively. M3, M4 are two access transistors controlled by the word-line signal. They are connected to the complementary bit-lines BL and $\overline{BL}$, and a flip-flop which acts as a transmission gate.

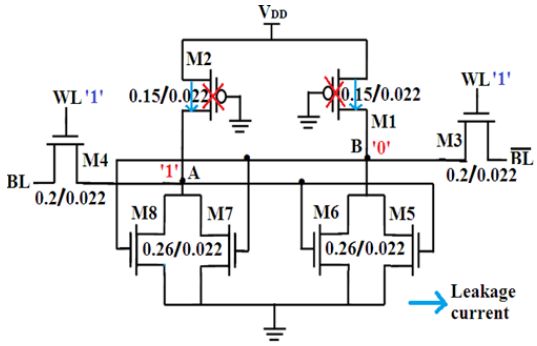


Figure 1. Schematic diagram of Proposed SRAM cell using a NOR gate with respect to a pseudo-nMOS inverter

The anticipated operation of the memory cell is as follows: A particular memory cell is selected by enabling the WL = 1 through transistors M3 and M4 to perform read/write operations. The information bit isto be composed and get exchanged to the BL, while its complement represents $\overline{BL}$. For example, if datalogic 1 is written to the BL = 1, its complement goes to the $\overline{BL}$=0. The data will be transferred and we get logic 1 at node A and logic 0 at node B, respectively. The data would be same and changes only with another write operation. The read operation takes place, whenever the memory cell is directed by enabling the WL = 1. Assume logic 1 is stored at node A, and its complement logic 0 is stored at node B. The current flows fromVDD, which in turns charges BL, via M2 and M4. At the same time, $\overline{BL}$ discharges to the ground

terminal, via M3 and M5. The stored content is read from the memory cell at the output. A small voltage differenceappears at the differential pair of bit-lines, where BL >$\overline{BL}$. The hold operation takes place, whenever the WL = 0 is disabled [8].

Instead of using nMOS inverter logic to build a NAND/NOR gate, preferred CMOS logic. Because the drawbacks of nMOS inverter are; i) when V_{in} = logic 1, the circuit dissipates more amount of power due to short-circuit from VDD to GND. ii) when V_{in} = logic 0, Vout cannot reach the VDD (logic 1) due to threshold voltage drop across the load transistor. iii) The load transistor is initially non-saturated and low resistance is present through the capacitive loads (charge) during switching of output from 1 to 0, require more propagation delay. The advantages of parallel connected devices are; i) Minimization of cell area takes place using Euler-path approach due to the parallel connection of storage devices in which the transistor's source and drain terminals are tied together. ii) Each and every transistor is connected parallel to the circuit gets the same amount of voltage. Hence, disconnecting or connecting the new devices without affecting the operation of other devices. iii) The current is enabled to pass through the circuit if any fault occurs in the circuit through any of the paths. If there is any fault occurred in the given circuit, the current is automatically passed through the circuit in different paths. iv) The width of a single transistor is increased, inversely proportional to the delay. By this parallel connection proposed delay of NOR-8T SRAM cell is reduced significantly expressed as eqn. 4. v) In detail, transistors (M5, M6, M7 and M8) have identical channel length connected in parallel, which is equivalent to a single transistor of channel width, equal to the sum of widths of the transistors (M5, M6, M7, and M8) [9].

If the size of the transistors is small, memory size would be reduced by a factor of 2, which helps to design the high packing density of SRAM array. The aspect ratio of MOSFET device plays a significant role in the design metrics of the SRAM cell. The power dissipation, access time, stability of the cell and area are interlinked with the width of the transistors along with the underlying scaling concerns. In the pseudo-nMOS inverter, the beta ratio affects the performance of the cell. We have to use a weak static load as PUN and a strong PDN as a compromise between noise margin and performance. Hence, 'ratioed circuits' influences transfer characteristics [10] and the strength of the PDN to the PUN ratios. To attain better performance of the cell, the aspect ratio of the transistors [11] is controlled by

$$1 \leq \frac{W_p}{W_n} \leq 2 \quad (1)$$

Where W_p and W_n are the widths of the pMOS and nMOS transistors. Implementation of any Boolean function with respect to Pseudo-nMOS inverter requires an N+1 number of transistors; whereas a 2N number of transistors are required for conventional CMOS logic (N denotes the number of inputs). Implementation of digital circuits using CMOS logic style would affect the output CL of the circuit. For settled VDD and frequency, reduction of dynamic power requires minimization of CL, which is evaluated by reducing [11] the area of the cell as

$$A = W_p L_p + W_n L_n \quad (2)$$

Where Lp and Ln are the lengths of the pMOS and nMOS transistors. The capacitance depends on the number of transistors required for implementation of a Boolean expression and the continuous switching of the transistors. For each of the transition, the dynamic power dissipation [12] is given by

$$P_{Dynamic} = \alpha C_L V_{DD}^2 f \quad (3)$$

Where α is the switching frequency, VDD is the supply voltage, CL is the load capacitance and f is the operating frequency. The transistors M1 and M2 of the PUN are as shown in Figure 1 always in ON state. The switching transition of the PUN is found to be reduced. Thus, the CL of the circuit is minimized, which in turn results for reduction of dynamic power.

2.2. SRAM cell using NAND gate with respect to a pseudo-nMOS inverter (NAND-8T)

The implementation (section 2.1) of SRAM cell's flip-flop using NOR gate is replaced with NAND gate. The design as shown in Figure 2 of a 1-bit SRAM cell by NAND gate using the Pseudo-nMOS inverter involves 8 transistors. In this circuit, M1, M5, M6 and M2, M7, M8 constitute two cross-coupled pseudo-nMOS inverters using NAND gate, act as a flip-flop. The PDN is the NAND gate implementation using the nMOS logic. The PUN is a pMOS transistor, in which the gate terminal is connected to the ground, such that

the pMOS transistor is always in ON [9] state. M1, M2 are the load transistors and M5, M6, M7, and M8 represent the storage transistors, respectively. M3, M4 are the two access transistors controlled by the WL signal, connected to the complementary bit-lines BL and $\overline{BL}$, and a flip-flop act as a transmission gate.

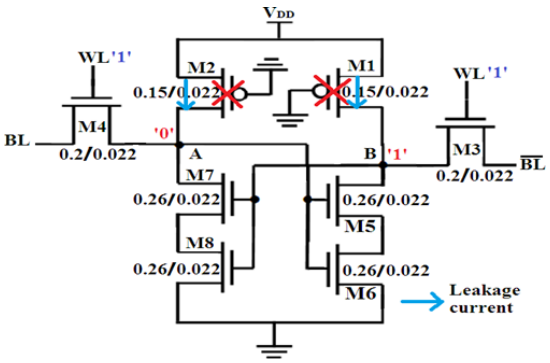


Figure 2. Schematic diagram of proposed SRAM cell using a NAND gate with respect to a pseudo-nMOS inverter

The read/write operation of the cell takes place whenever the WL = 1 is enabled. The operation of the memory cell is as follows: The data would be composed and get exchanged to the BL, as its complementwould be $\overline{BL}$. For example, if data logic 0 is written as BL = 0, its complement goes to the $\overline{BL}$= 1. A particular memory cell is selected by enabling the WL = 1, through transistors M3 and M4. The data would be transferred and logic 0 at node A and logic 1 at node B, respectively. The data would be same, while it changes with another write operation only. The read operation takes place whenever the memory cell is enabled by WL = 1. Thus, logic 0 is stored at node A, and its complement logic 1 is stored at node B. Thecurrent flows from VDD charges $\overline{BL}$ via M1 and M3. At the same time, BL discharges to the ground terminal via M4, M7 and M8. The stored content is read from the memory cell at the output. A small voltagedifference appears at the differential pair of bit-lines, where BL <$\overline{BL}$ .The hold operation takes place, whenever the WL = 0 is disabled.

The advantages of series connected devices are; i) Minimization of cell area take place using Euler-path approach by the series connection of storage devices, where transistor's source and drain terminals are tied together. ii) The width of the single transistor is decreased, which is directly proportional to the power dissipation of the NAND-8T SRAM cell as in eqn. 8. iii) The transistors M5, M6, M7 and M8 connected in series having identical channel length (L = 0.022µm) is equivalent to a single transistor of channel width equal to the reciprocal of the sum of the reciprocal of the widths of the transistors. iv) The same amount of current flows in a series connected transistors, which could not easily overheat the circuit.

In the existing SRAM cells i.e., 8T, 9T, 10T and 13T, the number of data and word lines required to design the cell are greater than or equal to 4. The number of lines (BLs + WLs) required as shown in Figure 2 to design the cell is 3. The performance of the cell would be increased with minimized data and word lines since internal wiring capacitance and resistance are reduced. In the conventional 6T-CMOS SRAM cell, the charging and discharging of a CL causes continuous switching transition for a flip-flop, i.e., VDD to ground during read/write operations. Hence, the dynamic power dissipation and delay of the cell is increased [8] by

$$\tau_{delay} = \frac{2 C_L V_{DD}}{\mu C_{ox}\left(\frac{W}{L}\right)\left((V_{DD}-V_{th})^2\right)} \quad (4)$$

Where CL represents the load capacitance, VDD is the supply voltage, µ denotes the electron mobility, Cox is the oxide capacitance, Vth is the threshold voltage and W/L denotes the width to length ratio of the MOSFET. To overcome the delay problem, NAND gate is designed for using a pseudo-nMOS inverter. The gate terminal of the PUN is connected to the ground, the pMOS transistors M1 and M2 are kept always in ON state. The switching transitions take place only from the PDN. The CL is reduced with minimized switching transitions; it leads to a reduction of dynamic power dissipation and delay of the cell. Whenever the size ofthe transistor is small, the area of the cell in the memory array would be reduced. Therefore, the CL is minimized, which in turn reduces the gate area. However, it would be difficult to drive

the data lines using small transistors. To overcome the drive on a problem, sensing is carried out by amplifiers viz., connected to the bit-lines.

2.3. SRAM cell using voltage divider bias current sink inverter (Current Sink-10T)

Typical circuit diagram of a current sink inverter is presented in Figure 3a. The input signal VIN is connected to the M1 transistor, to serve as a PUN. The transistor M2 acts as a current sink load in which the gate terminal of nMOS transistor is connected to the fixed bias supply voltage, which serves as a PDN. The nMOS transistor seems to sink towards the ground. By applying Kirchhoff Voltage Law to the transistor M2,

Therefore, $V_{GS} = V_{DD}$ (i.e. logic 1). The N-channel transistor would always be in ON state. Compare to active load inverters, higher voltage gain would be achieved by current sink inverter configuration. More amount of power would be dissipated due to fixed bias supply voltage connected to the nMOS. The voltage divider bias network M3, M4 connected as shown in Figure 3b by replacing the fixed bias supply voltage. Hence, the power dissipation would be reduced by dividing the network.

$$V_{DD}-V_{GS}+0=0 \quad (5)$$

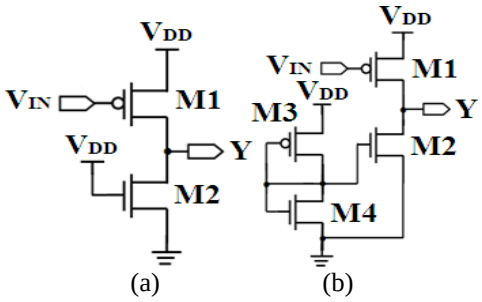


Figure 3. Schematic diagrams are (a) current sink inverter (b) a modified current sink inverter, using voltage divider bias

Design as shown in Figure 4 of a 1-bit SRAM cell is using voltage divider bias current sink inverter involves 10 transistors. M1, M2 are the load transistors and M5, M6, M7, M8, M9, M10 are the storage transistors respectively. M3 and M4 represent access transistors controlled by the WL signal. They are connected to thecomplementary bit lines BL and $\overline{BL}$, and a flip-flop, which in turn acts as a transmission gate. Here, transistors M1, M5, M6, M7 and M2, M8, M9, M10 constitute two cross-coupled inverter configurations to form a flip-flop, using a voltage divider bias current sink inverter. The read/write operation of the memory cell takes place by enabling the WL = 1, while WL = 0 being the hold operation. The complementary bitlines BL and$\overline{BL}$ act as input for a write operation and output for the read operations. The operation of the memory cell is as follows: The data to be composed would be exchanged to the BL. Its complement wouldgo to the$\overline{BL}$. For example, if data logic 1 is written to the BL = 1, its complement goes to the $\overline{BL}$ = 0. A particular memory cell is selected by enabling the WL = 1 through transistors M3 and M4. The data would be transferred. Thus, logic 1 would be received at node A and logic 0 at node B, respectively. The data would be same and changes with another write operation only. When WL = 1, the read operation takes place. The bit- lines get precharged to an equalized potential before the read operation. If logic 1 is stored at node A, and its complement logic 0 is stored at node B, the current flows from VDD charge BL via M2 and M4. At the sametime, $\overline{BL}$ discharges to the ground terminal via M3 and M5. The stored content is read from the memory cell at the output using bit-lines. A small voltage difference appears at the differential pair of bit-lines, where BL>$\overline{BL}$.

In the operation of the SRAM cell, the size of the transistor plays an important role. As the size of the transistors is maintained in a similar manner, the fabrication cost would be reduced. Along with wafer cost gate area Ag, the gate capacitance per unit area Co and gate capacitance Cg would be reduced with minimum sized transistors. Whenever the read/write operations take place, the switching transitions, (0→1, 1→0) of the load transistors would occur. The storage transistors would be always in ON state as they are connected to the VDD. The switching transitions are not required in the PDN. The energy consumption of the proposed SRAM cell using voltage divider bias current sink inverter would be decreased with reduced switching transitions from VDD to ground.

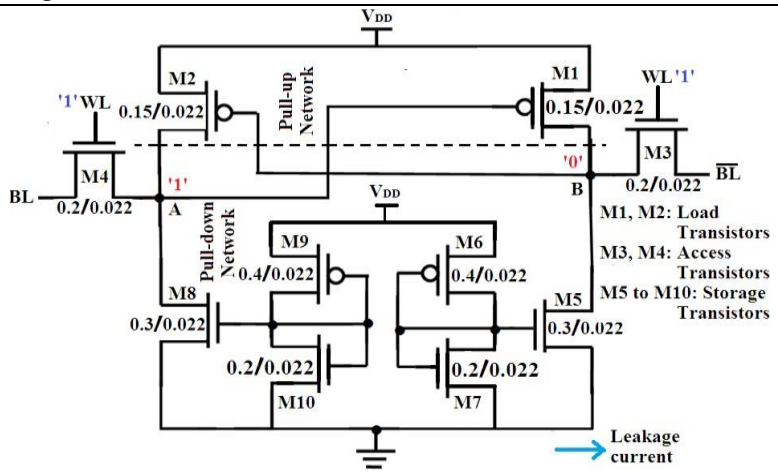


Figure 4. Schematic diagram of proposed SRAM cell using voltage divider bias current sinkinverter

2.4. SRAMcell using voltage divider bias current source inverter (CurrentSource-10T)

In the circuit diagram as shown in Figure 5a of a current source inverter, the PUN represents current source load in which the gate terminal of a pMOS transistor is connected to the source terminal. The input signal VIN is connected to the nMOS transistor, which serves as PDN. The pMOS transistor would sink towards the source terminal. By applying Kirchhoff Voltage Law to the transistor M1,

$$V_{DD}\text{-}V_{GS}\text{-}V_{DD}=0 \quad (6)$$

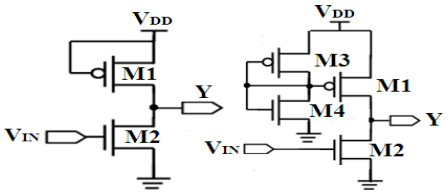


Figure 5. Schematic diagrams are (a) current source inverter (b) a modified current source inverter, using voltage divider bias

Therefore, VGS = 0 i.e. logic 0. The pMOS transistor would always be in ON state. Compared to active load inverters, higher voltage gain is achieved by current source inverter. More amount of power would be dissipated due to fixed bias supply voltage connected to the pMOS. The voltage divider bias network is connected by replacing the fixed bias supply voltage. Thus, the power dissipation would be reduced by dividing as shown in Figure 5b the network.

To design as shown in Figure 6 a 1-bit SRAM cell, with a voltage divider bias current source inverter configuration, 10 transistors are required. M1, M2, M7, M8, M9, M10 represents load transistors and M5, M6 represents storage transistors, respectively. M3 and M4 are two access transistors controlled by the WL signal. They are connected to the complementary bit lines (BL and $\overline{BL}$) and a flip-flop acts as a transmission gate. Here, transistors M1, M5, M7, M8 and M2, M6, M9, M10 are two cross-coupled inverters to generate a flip-flop using a voltage divider bias current source inverter configuration. The read/write operation of the memory cell occurs by enabling the WL = 1. WL = 0, hold operation takes place. The complementary bit-lines BL and $\overline{BL}$act as input for a write operation and output for the read operation, respectively.

The operation of a memory cell is as follows: The data to be composed would get exchanged to the BL and its complement to the $\overline{BL}$. For example, if data logic 0 is written to the BL = 0, its complement goes to the $\overline{BL}$ = 1. A particular memory cell is selected by enabling the WL = 1, through transistors M3 and M4. The data would be transferred, occurs logic 0 at node A; and logic 1 at node B, respectively. The data would be same and changes with another write operation only. When WL = 1, the read operation takes place. The bit-lines get precharged to an equalized potential before the read operation. If logic 0 is stored at node A, and complement logic 1 at node B, the current flows from V_{DD} to $\overline{BL}$by charging through M1 and M3.

Simultaneously, BL discharges to the ground terminal via M4 and M6. The stored content would be read out from the memory cell at the output using bit-lines. A small voltage difference appears at the differential pair of bit-lines, where BL <$\overline{BL}$

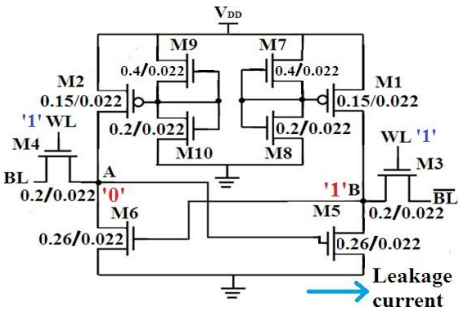


Figure 6. Schematic diagram of proposed SRAM cell using voltage divider bias current sourceinverter

Need of current source/sink inverter structures are; i) the current sink and current source inverters are used to control the flow of direct current in the load. It allows high noise margin with fast switching. ii) In 6T-SRAM cell, current source pull-up load is replaced instead of pMOS device acts as a load as shown in Figure 5(a). iii) Compared to active load inverters, high voltage gain is achieved by current source/sink inverters. iv) Similar to active-resistor load inverter, a large signal voltage transfer characteristics (VTC) curve is obtained. As the size of the transistors is small, the gate area and gate capacitance would be minimized since they are directly proportional to transistor's aspect ratio. MOSFETs, with similar sizes, would reduce the silicon wafer cost during the fabrication. As the current source load is always in the ON state, the switching activity of the PUN is reduced. The major advantage is that during switching through CL, transitions would be reduced due to the reduced switching transitions of the PUN. Hence, the minimization of energy consumption is achieved.

3. SIMULATION RESULTS ANDCOMPARISONS

The proposed SRAM cells based on inverter structures and the standard 6T, Conv. 8T and ST-11T are simulated using the mentor graphics with 22-nm technology. The simulations involve the timing waveform using the proposed as shown in Figure 7 inverter structures of 1-bit SRAM cell. The X-axis represents time (nanosec) and Y-axis as voltage (millivolts). The performance of the SRAM memory cell is further improved by the CMOS scaling technologies. As the technology shrinks down, the distance traveled by the electron between the source and drain of the MOSFET is reduced. The length of the MOSFET is directly proportional to the delay, and power can be expressed [12] as

$$t_p = \frac{L^2 V_{DD}}{\mu (V_{DD} - V_t)^2} \tag{7}$$

$$p = \alpha C_L V_{DD}^2 f = \alpha W L C_{ox} V_{DD}^2 f \tag{8}$$

Where V_{DD} is the supply voltage, α is the switching factor, V_t is the threshold voltage, f is the operating frequency, W is the width of the transistor and L is the channel length of the transistor. For different CMOS technologies, the estimated $P_{dynamic}$ and energy consumption seem to be minimized using proposed SRAM cells as shown in Table 1.

The switching or dynamic power dissipation of a CMOS logic circuit is defined as the charging and discharging of the output node capacitance expressed as (8). The switching factor (α) depends on the number of inputs. If the number of inputs increases, the output transition probability decreases, leads to dynamic power consumption. Comparison of dynamic circuit families (α = 1), with static CMOS logic styles (α is closer to 0.1) invariably requires less switching factor. The 1-bit SRAM cell designed for usingproposed inverter structures require 2-inputs to form a single inverter whereas the standard 6T-CMOS SRAM cell require 1-input. The Nand/Nor-8T and Current sink/source-10T SRAM cells require low switching factor of α = 0.1875 in comparison with 6T, 8T-SRAM cells, with α = 0.25.

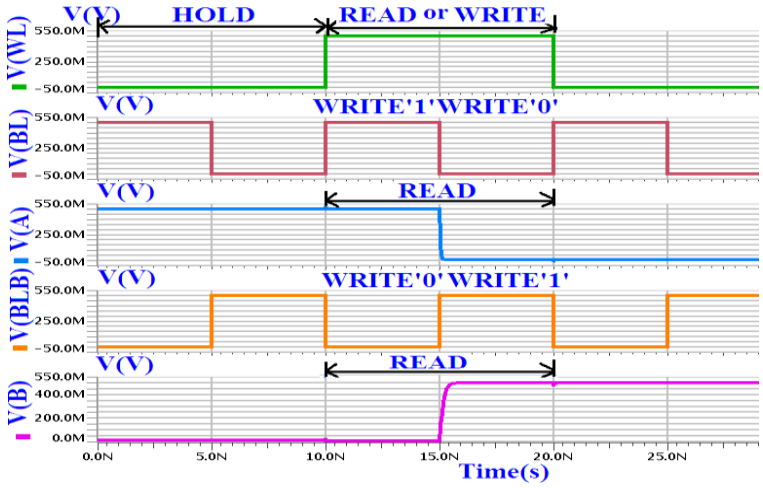


Figure 7. Stimulated timing waveform of the 1-bit SRAM cell using proposed inverter structures

Table1. Power and energy of different CM OS scaling technologies for various SRAM cells

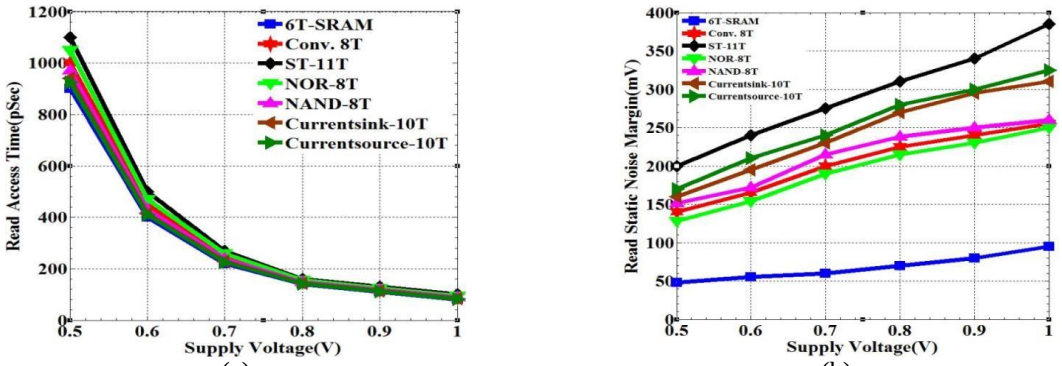
Comparison of different SRAM cells	Dynamic power consumption (µW) at V_{DD} = 1V					
	130 nm	90 nm	60 nm	45 nm	32 nm	22 nm
6T	6.12	3.08	0.74	8.02	5.90	03.8
Conv. 8T	6.12	3.05	1.79	7.62	3.09	09.8
ST-11T	4.35	7.19	4.09	9.85	5.42	11.0
NAND-8T	3.79	9.75	7.31	4.49	0.94	07.7
NOR-8T	3.78	9.32	6.27	4.10	0.24	07.1
Current Sink-10T	7.38	4.52	2.46	8.61	5.39	03.1
Current Source-10T	6.72	4.63	2.06	8.00	5.20	03.0

Comparison of different SRAM cells	Energy Consumption (fJ) of the cell at V_{DD} = 1V					
	13 nm	90 nm	60 nm	45 nm	32 nm	22 nm
6T	0.76	0.34	0.19	0.14	0.08	0.03
Conv. 8T	0.92	0.55	0.31	0.18	0.09	0.05
ST-11T	1.51	0.83	0.52	0.39	0.25	0.16
NAND-8T	0.53	0.35	0.20	0.1	0.07	0.03
NOR-8T	0.51	0.27	0.15	0.09	0.05	0.02
Current Sink- 10T	0.35	0.26	0.13	0.09	0.06	0.03
Current Source-10T	0.34	0.21	0.1	0.07	0.05	0.02

Due to the requirement of the supply voltage (V_{DD}), a major portion of the dynamic power occurs. In the proposed SRAM cells, more number of transistors is operating in the saturation region. The performance of the proposed SRAM cells does not get reduced due to low V_{DD}. To verify the functionality, the simulation of the proposed SRAM cells is carried out from minimum V_{DD} (i.e. 0.5 V) to the 1V. It is noticed that significant reduction occurs for the dynamic power results. The load capacitance C_L of the cell is reduced with minimized switching transitions of the device during high-to-low and low-to-high of the pull-up and pull-down networks (i.e., from V_{DD} to ground), leads to dynamic power consumption. But, a small amount of power is utilized by using voltage divider bias circuit in current sink/source-10T SRAM cell. The proposed current source-10T SRAM cell achieve 21%, 69% and 72% lower dynamic power dissipation than the 6T, Conv. 8T and ST-11T SRAM cells. For 1V supply voltage at 22-nm technology; the $P_{dynamic}$ and energy consumption is found to be 3.0 µW and 0.02 fJ. Thus, it is found to be extremely low for the current source-10T SRAM cell. Hence, the new SRAM cells are compared with the existing cells by varying the supply voltage in the range of 0.5-1V at 22-nm, which gives a better performance of the cell related to design metrics. The performance of the proposed cells is plotted without any loss of information in terms of output voltage levels. For this purpose BSIM3 LEVEL 53 nMOS.1model and pMOS.1model transistors with V_{Tn} = 0.31 V and V_{Tp} = -0.29 V are used.

3.1. Read access time (T_{RA}) and stability

The TRA is considered [5] as the time duration from the point when WL is activated to which a 50- mV difference is built across the complementary bit-lines BL and $\overline{BL}$. The comparison of T_{RA} for various SRAM cells is shown in Figure 8(a). It is observed that the Conv. 8T and ST-11T are associated with more than three BLs, plus WLs to result in higher TRA than for proposed cells.



(a) (b)

Figure 8. (a) Read access time (b) Comparison of Read Static Noise Margin (RSNM) of various SRAM cells

The comparisons of cell-ratio and pull-up ratios of different SRAM cells are presented in Table 2. For a read/write stability balance, cell-ratio (pull-down to access ratio) and pull-up ratio (pull-up to access ratio) need to be considered larger than 1 and smaller than 1. The read and write SNMs is found to depend on the cell-ratio and pull-up ratios. The read SNM seems to be required the pull-down transistors are stronger than the access transistors. The write margin requires (9) that the access transistors should be stronger than the pull-up transistors. As observed from the practical observations, given by

$$\left(\frac{W}{L}\right)_{pull-down} >> \left(\frac{W}{L}\right)_{access} > \left(\frac{W}{L}\right)_{pull-up} \quad (9)$$

The noise immunity [11] of a digital circuit would represent the ability of a logic gate to tolerate noise. Using DC transfer characteristics noise margins i.e. NM_H and NM_L of the proposed SRAM cells are calculated as shown in Table 2 at unity gain point. The proposed SRAM cells are using a voltage divider bias current sink and current source inverter structures seemingly allow high noise margin. As it provides a large signal VTC, it would allow fast switching with large voltage gain. In proposed cells, the PUNs represent the load transistors built with pseudo-nMOS inverter as showjn in Figure 1 and Figure 2 configuration. A weak pMOS device is required in which the pull-up ratio of the cell is less than existing ones. The read stability of the memory cells at low-voltage is determined in terms of SNM. The read SNM (RSNM) of an SRAM cell depends on the transistor width modulation. The cell ratio increases the RSNM, result in increased stability of the cell, as tuned by an underlying increase in an area of the cell.

Table 2. Comparison of Cell-ratio, Pull-up Ratio and Noise Immunity for Different SRAM Cells

Different SRAM cells	Cell-Ratio	Pull-up Ratio	Noise Immunity(V) at VDD = 1V	
			NMH	NML
6T	1.04	0.94	0.68	0.37
Conv. 8T	1.04	0.88	0.69	0.40
ST-11T	1.26	0.96	0.67	0.35
NAND-8T	1.3	0.75	0.69	0.42
NOR-8T	1.3	0.75	0.66	0.38
Current Sink-10T	1.5	0.75	0.63	0.32
Current Source-10T	1.3	0.75	0.67	0.36

To keep the cell area within the reasonable value, the width of the cell ratio is kept in the range given by (1). The stability of the write SNM depends on the pull-up ratio. If pull-up ratio is increased, the driving capability of the data bit will be written or flip the state of the cell would become difficult. By varying the supply voltage in the range of 0.5-1V, RSNM is measured as shown in Figure 8b using in the suggested [13, 14] method for various SRAM cells. It is observed that the current sink/source-10T SRAM cells are accompanied with 73% and 47% greater RSNM than that of 6T and Conv. 8T SRAM cells; it is achieved by voltage divider bias network built with larger cell-ratio during reading path resulted for large RSNM.

3.2. Write access time (T_{WA}) and ability

The write-access time (T_{WA}) represents the time duration from the point when WL is activated to that of the time where the storage node (to start with a low level) reaches to 90% of V_{DD} value for writing thelogic 1. Else, the time taken for writing logic 0, T_{WA} is defined as the time duration from the point when WL is activated [5, 15] to which the storage node (to start with a high level) reaches to 10% of V_{DD} value. The T_{WA} at various supply voltages of SRAM cells are presented in Figure 9. Due to the single-ended write operation, viz., in ST-11T, a very high T_{WA} for write 1 outlines. However other cells are using differential-pair of bit-lines for writing. The T_{WA} of the proposed SRAM cells are found to be lower than that for 6T, Conv. 8T and ST-11T. It is an argued due to the reduced critical path for writing the data (into the cell), which minimizes the switching transitions for the pull-up and pull-down networks. Thus, the delay time or T_{WA} is found to be directly proportional to the $C_{L.}$

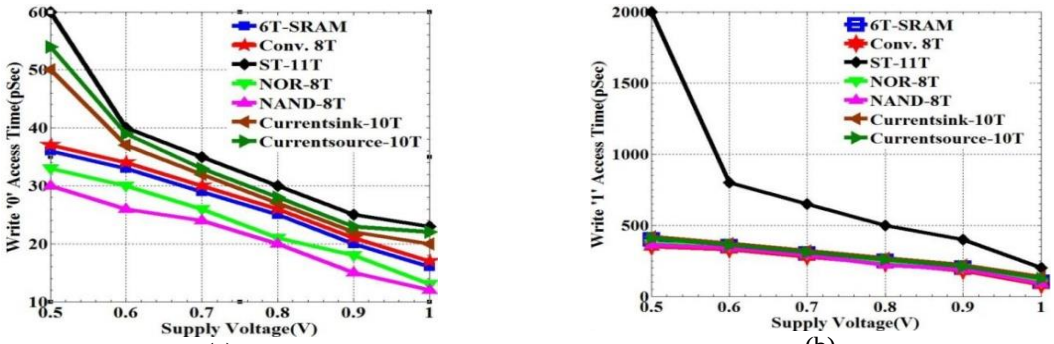


Figure 9. Write access time (T_{WA}) at various supply voltages of SRAM cells (a) Write 0 (b) Write 1

3.3. Read/write power and energy consumption

The power dissipation is directly proportional to the supply voltage and load capacitance. Delay is reduced by increasing the supply voltage and width of the transistor. Thus, it leads to the increase of area and power dissipation for the cell. Therefore, for better performance of the cell, minimize switching transitions and scale down the technology by maintaining the optimized supply voltage and width of the transistor. The maximum read/write power and energy consumed by 6T, Conv. 8T, ST-11T due to CL i.e. continuous switching transitions of PUN and PDN, Conv. 8T and ST-11T are found to be associated with more than three (BLs + WLs) during read/write operations. Larger aspect ratios appear to be required to design the cell when compared to the proposed cells. The proposed current sink-10T SRAM cell achieve 39%, 17% and 19% lower read power than the 6T, Conv. 8T and ST-11T SRAM cells as shown in Figure 10(a). It is absorved from the graph (Figure 10(b)) that the proposed current sink-10T SRAM cell achieve 41%, 23% and 42% lower read energy than the 6T, Conv. 8T and ST-11T SRAM cells. The proposed current sink-10T SRAM cell achieve 37%, 41% and 22% lower write '0' power than the 6T, Conv. 8T and ST-11T SRAM cells as shown in Figure 11(a). It is absorved from the graph (Figure 11(b)) that the proposed current source-10T SRAM cell achieve 68% and 70% lower write '1' power than the 6T and Conv. 8T SRAM cells. The proposed current sink/source-10T SRAM cells achieve lower average write energy than the existing ones at all considered supply voltages as shown in Figure 12

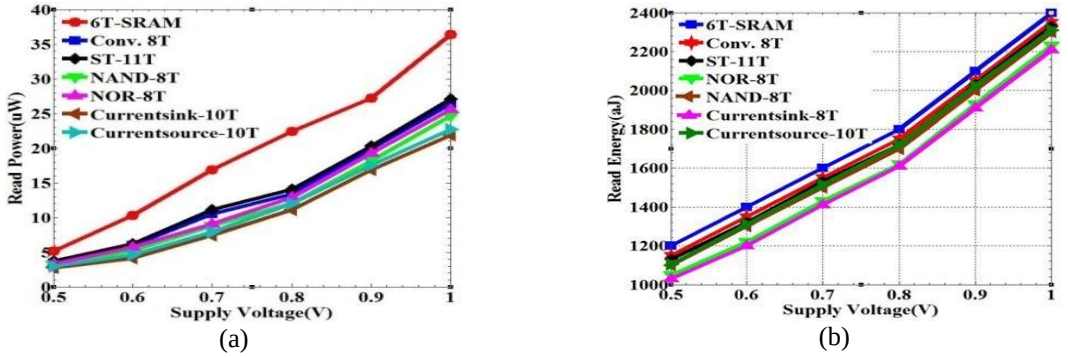


Figure 10. (a) Read power (b) Read energy at various supply voltages of different SRAM cells

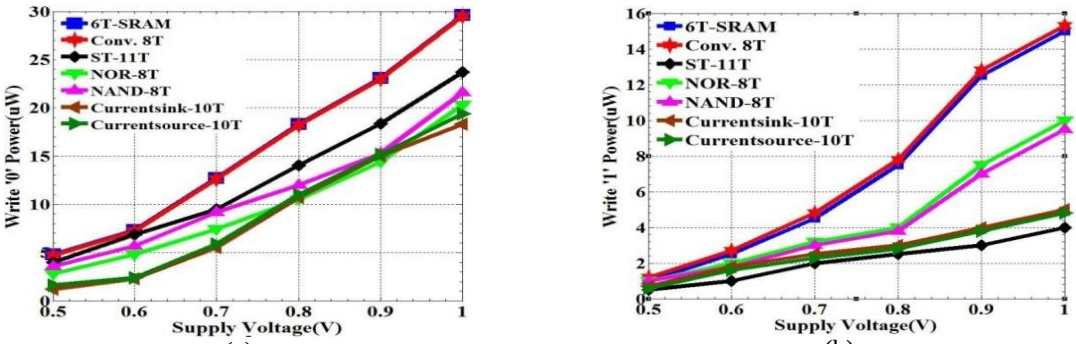


Figure 11. Write power at various supply voltages of SRAM cells (a) Write 0 (b) Write 1

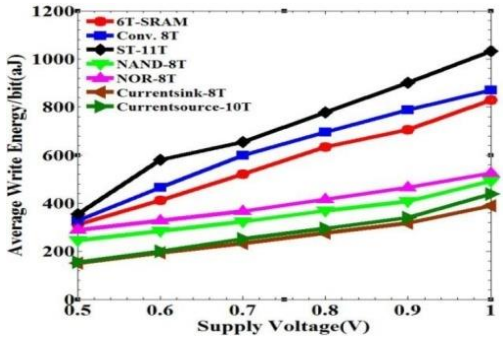


Figure 12. Write energy at various supply voltages of different SRAM cells

3.4. Static power consumption

As the CMOS technology shrinks down < 90 nm, the static power dissipation becomes comparable to dynamic power consumption. Whenever it enters into the deep sub-micron process, static power dominates the dynamic power. As the source-to-drain channel length decreases, short channel effects introduce potential problems in device characteristics leads to static power dissipation in standby mode. For memory circuits, static power would be a major contributor to total power consumption since most of the transistors in the cell are in standby mode [16]. The transistors crossed with red color indicate (Figure 1, 2, 4 and 6) that the transistor is in OFF state during the hold 1 state. The leakage current is found to occur due to cross-coupled inverters during the hold 0 and hold 1 state.

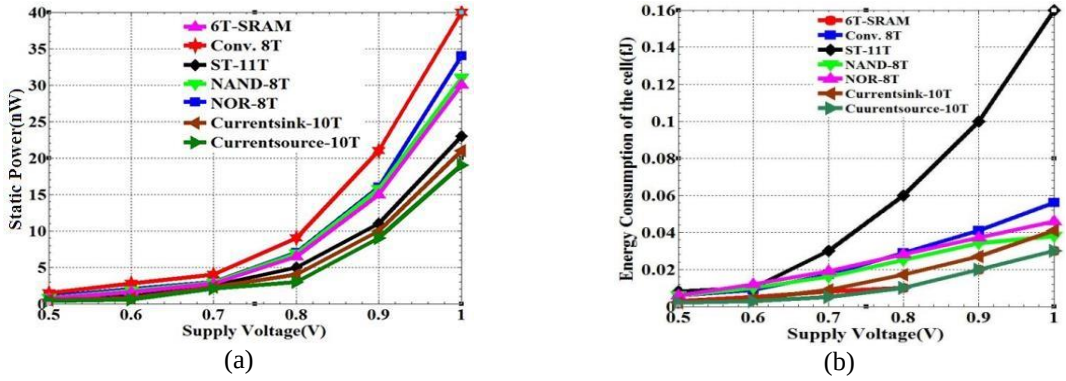


Figure 13. (a) Static power (b) Energy consumption of different SRAM cells at various supply voltages

The blue and light green colors indicates the static power dissipation of NOR and NAND-8T SRAM cells shown in Figure 13. As compare to 6T-CMOS and ST-11T SRAM cells, the NOR/NAND-8T SRAM cells using pseudo-nMOS inverter consume more amount of static power due to pMOS device i.e., always connected to the ground. For a series of stacked transistors the leakage current decreases. When the number of stacked devices is more than three the leakage current becomes negligible [17]. The leakage current for parallel connection of transistors equals to the sum of currents through each transistor. As shown in Figure 1, Figure 2, Figure 4 and Figure 6, the number of stacked transistors for each inverter section is ≥ 2, accomplishment of stack effect. It helps in reduction of leakage power or static power in proposed SRAM cells.

In order to minimize the static power, the cross-coupled inverters of proposed SRAM cells are built with minimum size along with combined stacking of transistors. The proposed current sink/source-10T SRAM cells are observed to result in reduced static power dissipation at all specified supply voltages as shown in Figure 13(a). The proposed current source-10T SRAM cell achieve 23%, 39% and 12% lower static power at various supply voltages in the range of 0.5-1V than the 6T, Conv. 8T and ST-11SRAM cells. It is absorved from the graph (Figure 13(b)) that the proposed current source-10T SRAM cell achieve 33%, 60% and 87% lower energy consumption of the cell than the 6T, Conv. 8T and ST-11T SRAM cells.

3.5. Comporison of area

The layouts of the proposed SRAM cells are presented in Figure 14; it is prepared by relying on mentor graphics IC layout 45-nm CMOS technology design rules. The proposed cells (NOR-8T/NAND-8T and current sink-10T/current source-10T) are found to occupy an area about 1.5 times greater and 1.8 times greater (Current Sink-10T/Current Source-10T) as compare to 6T-SRAM cell. Further, ST-11T is found to require a huge amount of area about 2.02 times greater than that for 6T-SRAM cell. It is observed that the dimensions of the proposed SRAM cells MOSFETs are of smaller geometry. Hence, they reduce the overall cell area, although more number of transistors is invoked. To increase the packing density of SRAM array, reduction of cell size poses a major concern. The specifications required for different SRAM cells are presented in Table 3. Diff.-Differential, SE-Single Ended, BL-Bit line, WL-Word-Line, RBL-Read bit line, WBL-Word bit line, VGND-Virtual Ground control for floating node

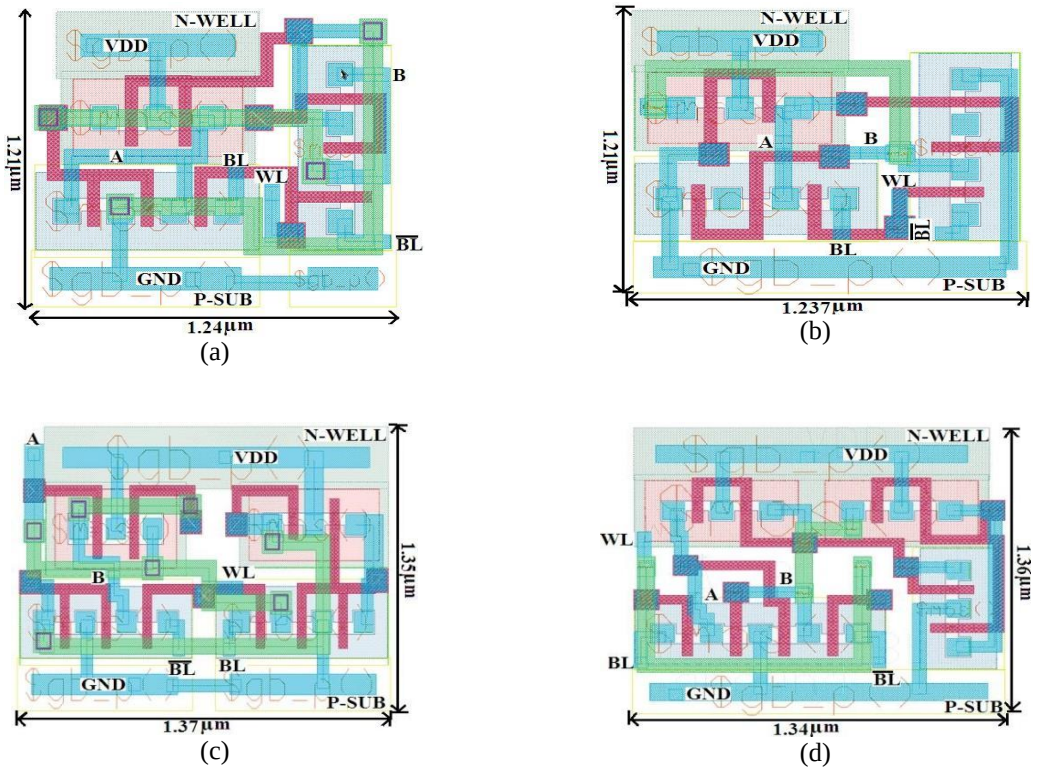


Figure 14. layout of Proposed SRAM cells are using (a) NOR-8T (b) NAND-8T (c) Current Sink-10T (d) Current Source-10T

Table 3. Comparison of Various SRAM Cells

Memory cell specifications	Conv. 6T [1]	Conv. 8T [1]	ST-11T [4]	Proposedwork	
				Nand/Nor-8T	Current sink/source-10T
Writing/Reading	Diff./Diff.	SE/Diff.	SE/SE	Diff./Diff.	Diff./Diff.
Control signals	1-WL	1-WL, 1-RWL	1-WL, 1-RWL, 1 VGND	1-WL	1-WL
Bit lines	2-BL	2-WBL, 1RBL	1-WBL, 1-RBL	2-BL	2-BL
Area (μm^2)	1	1.44	2.02	1.49/1.50	1.84/1.82
Minimum V_{DD}	0.33	0.33	0.36	0.47	0.34

3.6. Advantages of proposed SRAM cells

In summary, the advantages of the proposed SRAM cells are i) it operates in deep submicron at 22-nm technology, where the performance of the cells are examined and high robustness is observed. ii) In the pseudo-nMOS inverter, the beta ratios will affect the performance and power dissipation of the cell. Usage of a weak pull-up device, a static load, and a strong pull-down network leads to a negotiation between the noise margin and transfer function. iii) The design of cross-coupled inverters using NAND/NOR gate with respect to pseudo-nMOS inverter gives support to built an SRAM cell. The major advantage of using pseudo-nMOS would be the reduced input capacitance and area. iv) By using pseudo-nMOS inverter the switching transitions of the pull-up network gets reduced. Thus, the load capacitance of the circuit is minimized to result in dynamic power optimization.v) Even though high voltage gain is achieved by using current sink and current source inverters, a huge amount of power is dissipated due to fixed bias supply voltage. Usage of voltage divider bias current sink/current source inverters (by replacing fixed V_{DD}) reduces the power dissipation by dividing the network. vi) The transistors present in the cross-coupled inverters are connected in series. Thus, create an output voltage drop in the cells. To overcome this, the substrate terminals of all nMOS transistors are connected to the ground and the substrate terminals of all pMOS transistors are connected to the V_{DD}. Thus, the output voltage drops probably annuled. vii) The leakage current is minimized due to Stacking of MOSFETs in proposed cells. Using Euler path approach, optimization of layout area would be carried out.

4. CONCLUSIONS

This paper presents four cross-coupled inverter structures based SRAM cells are using NAND-8T, NOR-8T, Current sink-10T and Current source-10T.The performance of the proposed cells are a) significantly improved SNM and less energy consumption for applied voltages of considered SRAM cells. b) The dynamic power of the proposed cells are reduced due to the scaling of the supply voltage i.e. VDD = 0.5V. c) Device geometries and the switching transitions of the cell are decreased by using either PUN or PDN leads to the reduction of CL. d) The maximum Power-Delay Product is obtained by ST-11T and minimum energy consumption is achieved by current source-10T SRAM cell. e) The proposed current sink/current source-10T SRAM cells consume 49%, 37% and 9% low static power at various supply voltages in the range of 0.5-1V in comparison with Conv. 8T, 6T-SRAM, and ST-11T. f) For high performance, low-power and high-density SRAM architectures for mobile and storage applications, the essential benefits of the proposed SRAM cell structures could be fully utilized.

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