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Geometric and process design of ultra-thin junctionless double gate vertical MOSFETs

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ABSTRACT

The junctionless MOSFET architectures appear to be attractive in realizing the Moore's law prediction. In this paper, a comprehensive 2-D simulation on junctionless vertical double-gate MOSFET (JLDGVM) under geometric and process consideration was introduced in order to obtain excellent electrical characteristics. Geometrical designs such as channel length (L_{ch}) and pillar thickness (T_p) were considered and the impact on the electrical performance was analyzed. The influence of doping concentration and metal gate work function (WF) were further investigated for achieving better performance. The results show that the shorter L_{ch} can boost the drain current (I_D) of n-JLDGVM and p-JLDGVM by approximately 68% and 70% respectively. The I_D of the n-JLVDGM and p-JLVDGM could possibly boost up to 42% and 78% respectively as the T_p is scaled down from 11nm to 8nm. The channel doping (N_{ch}) is also a critical parameter, affecting the electrical performance of both n-JLDGVM and p-JLDGVM in which 15% and 39% improvements are observed in their respective I_D as the concentration level is increased from 1E18 to 9E18 atom/cm^3. In addition, the adjustment of threshold voltage can be realized by varying the metal WF.

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1. INTRODUCTION

For more than a decade, Moore's law has been an ultimate guideline for MOSFET minituarization. The main obstacle of shrinking the dimension of MOSFET is the decrease in gate controllability over the channel due to high electric field [1-4]. An alternative solution to improve the gate control over the channel is by adding an extra gate [5-10]. Multi-gate MOSFETs have been recognized promising candidates for future scaling of MOSFET technologies. These multi-gate devices, apart from providing better immunity of short channel effects (SCE), are still not really perfect and suffered from similar challenges encountered with conventional bulk MOSFET. The most crucial challenge is to form an ultra-shallow source/drain (S/D) junctions with high doping concentration gradient, which needs an advanced S/D and channel engineering [11]. Recently, a lot of junctionless MOSFET structures [12-19] have been introduced to overcome the difficulties in forming ultra-shallow junctions. The main design criteria of junctionless MOSFET is that the channel and S/D region are doped with the same dopant type (n- or p-type) and are normally employed in the range of 10^{18} to 10^{20} cm^{-3} [20]. There is no junction formed between the channel and S/D regions, thereby simplifying the fabrication process. Junctionless MOSFETs work in depletion mode, which significantly rely on the ultra-thin body architecture.

Initial work reported in [21] revealed that the physics of junctionless MOSFET is different from the conventional MOSFET. Current conduction in Junctionless MOSFETs is based on bulk phenomena in which the gate voltage would induce the depleted region in the ultra-thin channel in order to turn off the transistor. Meanwhile, the channel region (ultra-thin body) should be highly doped in order to turn on the transistor instantly. The simulation comparison between Junctionless nanowires transistor (JNT) and the inversion mode multi-gate FET (MuGFET) was reported in [21] and it was conducted using ATLAS module of Silvaco. The results revealed that the subthreshold swing (SS) of the JNT was 21% lower than MuGFET, implying that the JNT has faster switching capability than MuGFET. This happens due to the utilization of high doping and ultra-thin body in JNT structure that allows a higher electron mobility in the channel. A novel design analysis for a junctionless double gate vertical MOSFET (JLDGVM) using Silvaco TCAD (ATLAS) was previously reported in [22]. The results found that the drain barrier lowering (DIBL), subthreshold swing (SS) and leakage current (I_{OFF}) of the junctionless device are much lower than the junction device. This might happen due to the absence of the junction in which the depeletion layer width at drain and source was totally eliminated. Furthermore, the application of metal-gate and hafnium dioxide (HfO_2) to the JLDGVM structure did contribute a significant improvement of the on-current (I_{ON}). The metal-gate work function (WF) was tuned to obtain a higher I_{ON} magnitude for much better performance of the device. Although, the that junctionless vertical configuration has contributed a significant boost on the electrostatic performance, it still requires in-depth investigation on the impact of geometrical and process parameter variation (i.e. channel length, pillar thickness, channel doping, source/drain doping and metal-gate workfunction) on the electrostatic performance of the device. Thus, this recent study will provide a detailed approach of designing, studying, analyzing and improving transistor performance using Silvaco TCAD simulation tools. It will also provide a significant in sight on the design consideration of the JLDGVM in regard with the electrostatic behaviours such as drain current, current density and subthreshold swing.

2. ULTRA-THIN JLDGVM's DESIGN

A 2-D simulation for ultra-thin JLDGVMs were investigated, and the process flow of the device is depicted in Figure 1. The device process includes the ultra-thin pillar formation, the high-*k* metal-gate (HKMG) deposition, source/drain implantation and metallization.

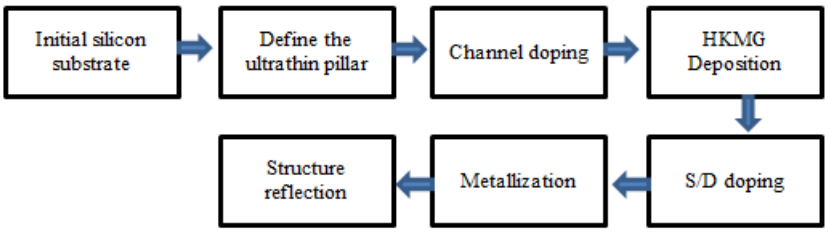

Figure 1. Simulated process flow for ultra-thin JLDGVM's design

2.1. JLDGVM's structure

The ultra-thin JLDGVMs utilized hafnium dioxide (HfO_2) as a dielectric combined with metal-gate, tungsten silicide (WSi_x). The simulated n-JLDGVM is a heavily n-type doped ($1x10^{18}$ cm^{-3} of Arsenic) channel with 10-7nm range of silicon pillar's thickness (T_p) and 15-12nm range of channel length (L_{ch}). In contrast, the simulated p-JLDGVM is heavily doped with $1x10^{18}$ cm^{-3} of boron dose. Double-gate structure was used to provide better controllability over the channel. The source and drain region for both n and p-type device were also heavily doped with the similar type as channel doping in order to form N^+ N^+ N^+ and P^+ P^+ P. Table 1 shows the geometrical and process parameter values used in the simulated n-channel and p-channel devices. The simulation was conducted by varying one parameter at a time while keeping the other parameters constant in order to study the effect of a specific design parameter on the device performance. The 2-D cross-section of the device which define the physical parameters like silicon pillar's thickness (T_p) and channel length (L_{ch}) is depicted in Figure 2.

Table 1. Parameters used in the simulated JLDGVMs

Variables	Units	Fixed value	Manipulated range
Channel Length, L_{ch}	nm	11	9 to 12
Pillar Thickness, L_p	nm	9	11 to 8
Channel doping, N_{ch}	Atom/cm^3	1.0E18	1.0E18 to 9.0E18
S/D doping, N_{sd}	Atom/cm^3	1.0E18	1.0E18 to 9.0E18
Metal work-function, WF	eV	4.5	4.5 to 4.7

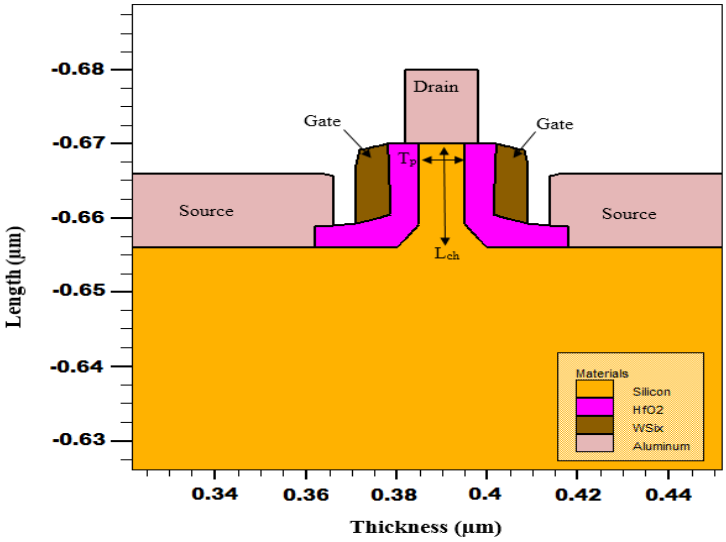

Figure 2. Cross section of the JLDGVM device

2.2. Device simulation

The TCAD Silvaco, Athena and Atlas were employed in this work to simulate the electrical characteristics of the JLDGVM devices. The devices were set up for simulation in both linear and saturation mode. For the purpose of simulating I-V curves of the devices, the Silvaco TCAD utilizes the following set of physical model: 1) drift diffusion (DD) model with simplified Boltzmann carrier statistics; 2). The inversion layer mobility model combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models. This recombination model was selected to consider the phonon transitions effect due to the presence of a trap (or defect) within the forbidden gap of the devices. Critical electrical characteristics like threshold voltage (V_{TH}) ON-state current (I_{ON}), OFF-state current (I_{OFF}) and subthreshold swing (SS) could be extracted from the I_D vs. V_G characteristic. The device simulation condition is set up as listed in Table 2 [23]. The I_{ON}, I_{OFF} and SS values can be extracted from the curve.

Table 2. Device simulation conditions [23]

Electrical Characteristics	Drain Voltage, V_D (V)	Gate Voltage, V_G (V)		
		$V_{Initial}$	V_{Step}	V_{Final}
Threshold Voltage (V_{TH})	1.0	0	0.1	2.0
On-state Current (I_{ON})	1.0	0	0.1	2.0
Off-state Current (I_{OFF})	1.0	0	0.1	2.0
Subthreshold Swing (SS)	1.0	0	0.1	2.0

3. GEOMETRIC DESIGN CONSIDERATION

Figure 3 depicts the impact of L_{ch} and T_p on I_D vs. V_G characteristics of the JLDGVM devices. Figure 3(a) shows the impact of channel length (L_{ch}) scaling on the I_D-V_G characteristic of both n-JLVDGM and p-JLVDGM devices. The drain current (I_D) of the n-JLVDGM and p-JLVDGM can boost up to 68% and 70% respectively as the L_{ch} is scaled down from 12nm to 9nm, shifting the I_D-V_G characteristic to the positive x-axis for n-JLVDGM and to the negative x-axis for p-JLVDGM. In this work, the smaller L_{ch} enhances the current flow due to less resistance resulted from shorter path between source and drain region. As a result, the V_{TH} decreases, allowing the I_D to significantly increase. Both n- and p-type devices show that the variation of L_{ch} do contribute a significant impact on the I_D as the maximum I_D is increased over

the reduction of L_{ch}. Meanwhile, the drain current (I_D) of the n-JLVDGM and p-JLVDGM could boost up to 42% and 78% respectively as the T_p is scaled down from 11nm to 8nm, shifting the I_D-V_G characteristic to the positive x-axis for n-JLVDGM and to the negative x-axis for p-JLVDGM. The thiner pillar would speed up the device as the channel is rapidly transformed to fully-depleted mode.

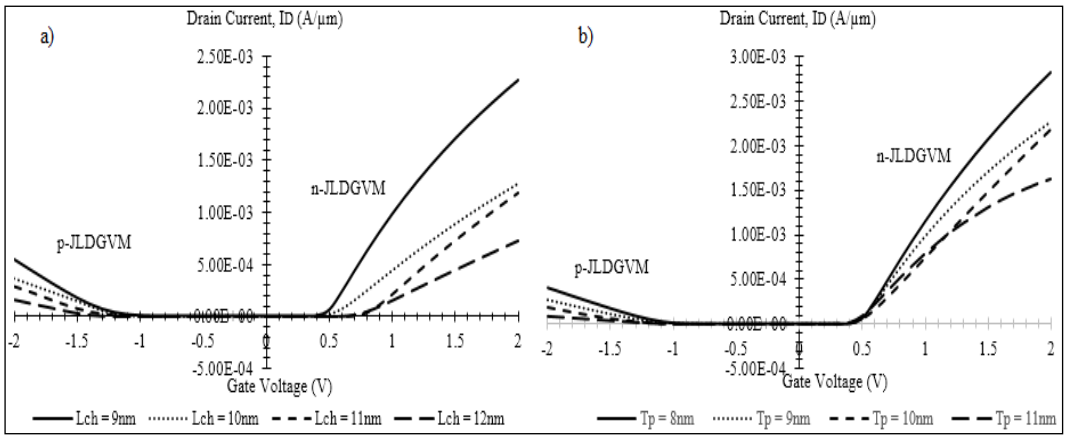

Figure 3. Graph of the drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different (a) L_{ch} and b) T_p

The subthreshold swing (SS) is an important characteristic of MOSFETs that measure how fast the transition could be triggered from 'ON' to 'OFF' condition or vice versa. It also determines the scalability limits of the devices by indicating how effectively the flow of drain current could be halted as the gate voltage is decreased below threshold limit [24]. The subthreshold swing (SS) was extracted from the inverse slope of $\log_{10} I_D$ vs V_{GS} characteristic shown in (1) [24]:

$$SS = \left[\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right]^{-1} \quad (1)$$

Figure 4 depicts the impact of the channel length variation on the SS characteristic of the devices. The SS is slightly decreased as the channel length of the devices are deliberately decreased, implying a directly proportional relationship between SS and L_c for both n- and p-channel JLDGVM. The shorter L_c of the device emulates the behavior of a fully-depleted devices in which the majority carrier (electron for n-JLDGVM and holes for p-JLDGVM) concentration were depleted as a sufficient gate voltage is applied. This subsequently reduces the parasitic capacitance which offers a near ideal SS characteristic (60mV/decade).

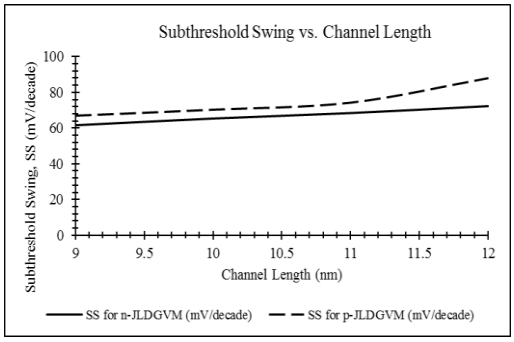

Figure 4. Subthreshold swing vs. channel length

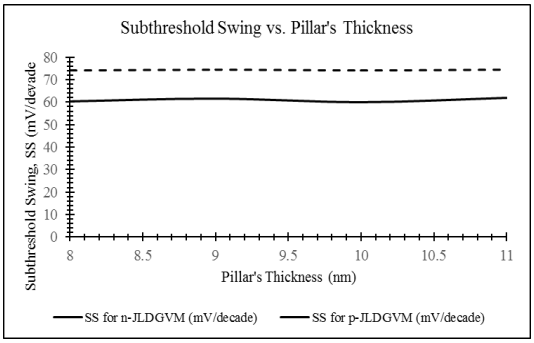

Figure 5. Subthreshold swing vs. pillar thickness

Figure 5 depicts the impact of the pillar thickness variation on the SS characteristic of the devices. It is observed that the variation in the pillar thickness variation do not contribute much effect on the SS characteristic. This is mainly due to the presence of high-*k*/metal-gate stack in forming the conducting channel of the device. The utilization of tungsten silicide (WSi_x) and hafnium dioxide (HfO_2) as the substitute materials for polysilicon and SiO_2 accordingly do reduce the amount of the required gate voltage to increase the drain current per decade. Since there are no poly depletion effects in high-*k*/metal-gate configuration, the variation in the pillar thickness is almost insignificant.

4. PROCESS DESIGN CONSIDERATION

For further understanding of the behavior of JLDGVMs, the impact of process design variation on I_D-V_G is presented in this section. Section A, B, and C will describe the impact of channel doping (N_{ch}), source/drain doping and work function (WF) upon the drain current (I_D), leakage current (I_{OFF}) and subthreshold swing respectively.

4.1. Channel doping (N_{ch})

Channel doping is a common approach to tune the V_{TH} of MOSFET devices [16],[25]. For short channel devices, the doping concentration in the channel region play a crucial part in determining the maximum I_D, I_{OFF} and also the SS characteristics. For that reason, multiple I_D-V_G curves with respect to different N_{ch} concentration are investigated, as depicted in Figure 6. Based on the curves, it can be observed that the higher concentration of N_{ch} reduces the V_{TH} value in both n-channel and p-channel JLDGVM devices. This is mainly due to mobility enhancement resulted from the increase of majority carriers in the channel region. As a results, the maximum I_D is observed to be improved by approximately 15% and 39% in both n-channel and p-channel JLDGVM devices respectively as a higher concentration of N_{ch} is applied. In other word, the higher concentration of N_{ch} allows much lower gate voltage to invert the channel. Nevertheless, such low V_{TH} causes deterioration in leakage current (I_{OFF}) as depicted in Figure 7. From the graph, it can be observed that the higher concentration of N_{ch} do increase the I_{OFF} value of both devices. Such occurrence mainly happens due to higher subthreshold slope that slow down the variation of I_D that occurs below the V_{TH}. Figure 8 depicts the impact of channel doping concentration upon SS variation.

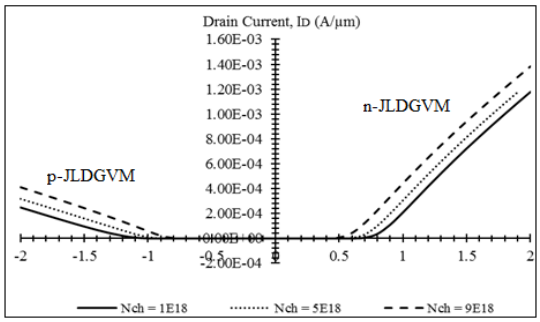

Figure 6. Graph of the drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different concentration of channel doping

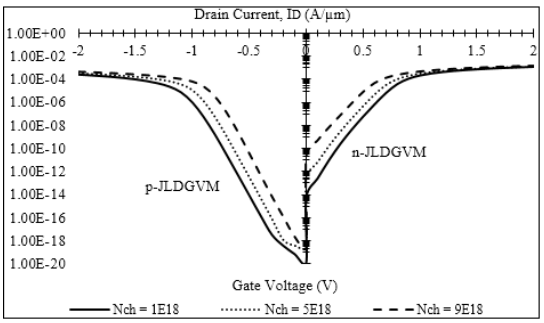

Figure 7. Graph of the subthreshold drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different concentration of channel doping

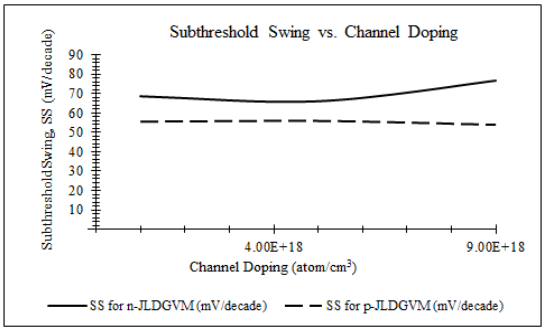

Figure 8. Subthreshold swing vs. channel doping

Based on the plot, the SS variation of n-JLDGVM is more prone to roll up along with an increased N_{ch} compared to p-JLDGVM. This is fundamentally due to the electrons in n-channel have twice mobility acceleration compared to holes in p-channel. The SS of n-JLDGVM is observed to be approximately 19% higher than the SS of p-JLDGVM. This indicates that the p-JLDGVM could switch from its off-state to on-state much faster than the n-JLDGVM.

4.2. Source/drain (S/D) doping (Nsd)

In junctionless configuration, the material used for the source/drain doping is similar with the material used in previous channel doping process [11]. For instance, the n-JLDGVM and p-JLDGVM fabrication requires arsenic and boron respectively as dopants for source/drain doping (N_{sd}). Figure 9 presents the variation effects of N_{sd} on the I_D-V_G characteristic for both JLDGVM and p-JLDGVM devices. In short channel devices, the diffusion of the S/D doping play an important role in V_{TH} changes. However, the variation of N_{sd} in JLDGVM devices do not give any significant impact on the I_D-V_G characteristic. This obviously shows that the concentration of N_{sd} in both devices is too low to change the V_{TH}. The values of N_{sd} are chosen below 10^{20} cm^{-3} in order to limit band-to-band-tunneling (BTBT) current due to heavy N_{ch} of 10^{18} cm^{-3}. The higher doping concentration in the silicon channel triggers larger effect of BTBT which eventually leads to a significant leakage current in the OFF state [3]. As a results, the maximum I_D is enhanced by approximately 10.6% and 2.3% in both n-channel and p-channel JLDGVM devices respectively as a higher concentration of N_{sd} is applied.

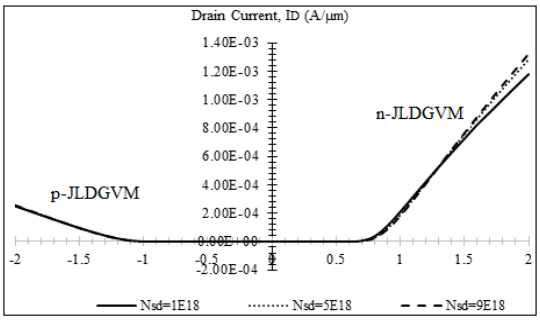

Figure 9. Graph of the drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different concentration of S/D doping

Further observation shows that further leakage occurs when N_{sd} is increased due to V_{TH} reduction, as depicted in Figure 10. The reduction in leakage current (I_{OFF}) for p-JLDGVM as the N_{sd} is increased is extremely minimal. The changes in I_{OFF} values for p-JLDGVM is almost unnoticable where the percentage difference is only 28%. Whereas the I_{OFF} value of n-JLDGVM is increased by approximately 98% as the N_{sd} is increased. This indicates that higher concentration of N_{sd} (>10^{18} cm^{13}) is required to significantly change both I_{ON} and I_{OFF} characteristic for p-JLDGVM. Figure 11 shows the impact of S/D doping upon the SS characteristic. It is observed that the SS values for n-JLDGVM are linearly increased as the N_{sd} is increased. However, the SS values for p-JLDGVM remains constant as the N_{sd} is increased. Similar to N_{ch}, N_{sd} do not contribute a significant impact on the SS characteristic for p-JLDGVM. The SS value of p-JLDGVM is more steep than the n-JLDGVM due to an extremely lower I_{OFF} value in which the amount of I_D increased per decade below the V_{TH} in the p-JLDGVM is higher than the n-JLDGVM. As a result, the ON/OFF ratio of p-JLDGVM is observed to be much better than the n-JLDGVM.

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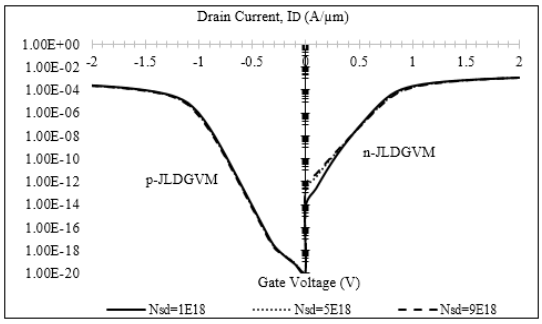

Figure 10. Graph of the subthreshold drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different concentration of source/drain doping

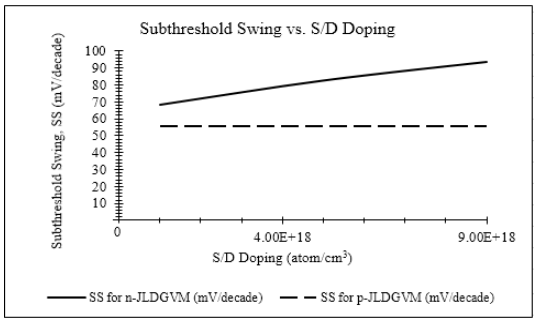

Figure 11. Subthreshold swing vs. s/d doping

4.3. Metal-gate work function (WF)

Apart from doping concentration, the work function (WF) also plays an important role to tune the V_{TH} value in junctionless MOSFETs [13, 26-28]. The WF significantly depends on the distribution of atoms at the surface of channel material, where a specific material has a fixed WF value [29]. Previously, the application of different metal-gate work functions in JLDGVM has been reported [22], stating that the I_D of n-JLDGVM was increased as the WF was decreased. This statement supports the current study about the variation effects of WF on the I_D-V_G characteristic for both n-JLDGVM and p-JLDGVM devices, as depicted in Figure 12. It is observed that the I_D for n-JLDGVM is increased by 15% as the WF is reduced from 4.7 eV to 4.5 eV. Such occurrence is mainly due to the early depletion of the channel surface between the two metal-gates that increases the I_D without enhancing the channel concentration. However, reverse trend of I_D variation has been observed in p-JLDGVM, where the value of I_D is increased by 20% as the WF is increased from 4.5 ev to 4.7 eV. Hence, it can be concluded that the WF value is inversely proportional to the I_D variation in n-JLDGVM, while the WF value is directly proportional to I_D variation in p-JLDGVM.

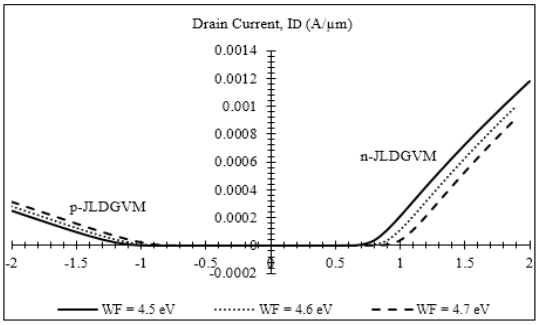

Figure 12. Graph of the drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different work functions

The combination of tungsten silicide and hafnium dioxide as a metal-gate and dielectric material respectively has improved the performance of JLDGVM in term of I_D, as well as I_{OFF}, as presented in Figure 13. It is observed that the I_{OFF} value for n-JLDGVM is tremendously reduced by 99% as the WF is increased from 4.5 eV to 4.7 eV. Similar to I_D variation, the opposite trend is observed in the p-JLDGVM as I_{OFF} value for p-JLDGVM is enormously reduced by approximately 97% as the WF is decreased from 4.7 eV to 4.5 eV. From sub-I_D-V_G characteristic, it can be concluded that the WF value is inversely proportional to the I_{OFF} variation in n-JLDGVM, while the WF value is directly proportional to I_{OFF} variation in p-JLDGVM. Thus, the performance of JLDGVM should be reasonably controlled with a proper tuning of the metal-gate WF. Figure 14 shows the impact of WF upon the SS variation in both n-JLDGVM and p-JLDGVM. It is observed that any changes in WF value do not contribute a significant impact on the SS value of both devices, since the SS values are almost constant as the WF is varied from 4.5 to 4.7 eV. This result further signifies that the elimination of poly depletion effect due to the introduction of high-*k*/metal-gate stack in the JLDGVM architecture do provide better short channel effects (SCE) suppresion.

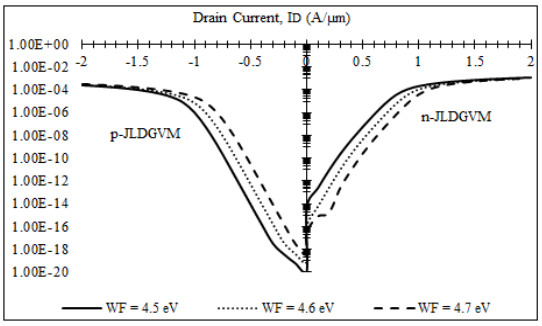

Figure 13. Graph of the the subthreshold drain current (I_D)-gate voltage (V_G) at V_D = 1.0 V with different work functions

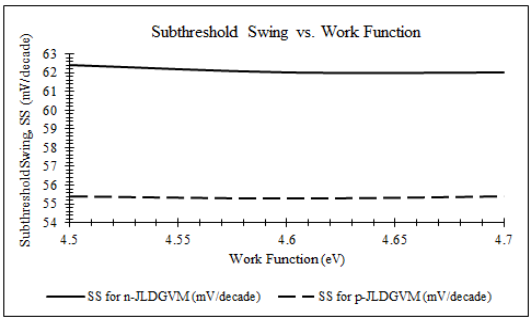

Figure 14. Subthreshold Swing vs. Work Function

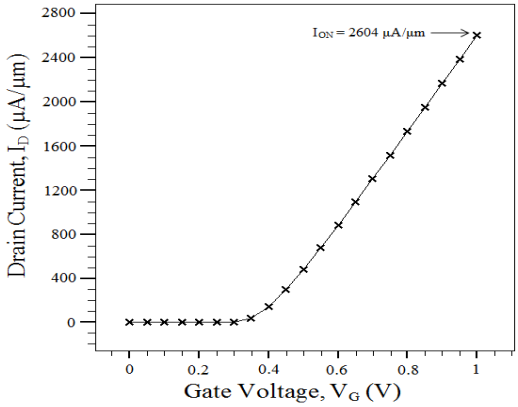

Figure 15. I-V curve at V_D = 0.5 V for n-JLDGVM device with WF = 4.5 eV

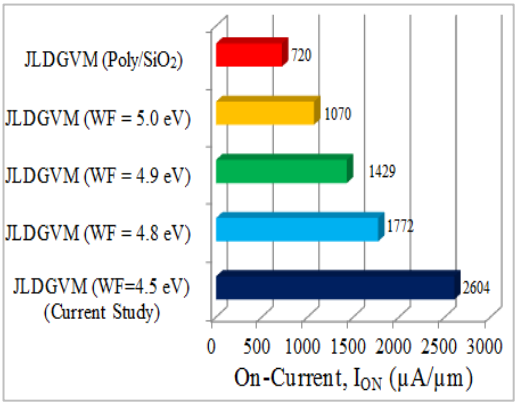

Figure 16. Benchmark of n-JLDGVM device with other junctionless vertical devices with multiple WF magnitude [18]

From the overall results, it can be concluded that the investigated geometrical and process parameter adjustments are very sensitive to the JLDGVM behavior. Although, the process parameter adjustment can boost the carrier mobility, its current improvement would be marginal when compared with geometrical parameter. For comparative purpose, the n-type device with WF = 4.5 eV was re-simulated at a constant V_D = 0.5 V as the V_G is shifted from 0 V to 1 V. The I_{ON} magnitude of the n-JLDGVM device with WF = 4.5 eV can be measured at V_G = 1V as depicted in Figure 15. Figure 16 summarizes the comparison of the I_{ON} magnitude of this current study with vertical double-gate transistors with multiple WF magnitude from previous studies [22]. Based on the comparison, it is observed that the n-JLDGVM device (current study) has demonstrated the highest I_{ON} magnitude compared to other devices. The trend of I_{ON} magnitude is in agreement with the previous studies as the lower WF do contribute a higher I_{ON} magnitude. Tuning the metal-gate WF in the range of 4.5-4.7 eV seems to be an effective method in attaining much better ON and OFF state current as well as ON/OFF ratio. In addition, doping concentration can be also adjusted to tune JLDGVM performance, yet the trend of its impact upon I_D-V_G characteristic has to be well considered. Thus, controlling the geometrical and process design is very crucial in order to obtain better device performance. For future work, several optimization approaches [30-33] could be employed to control and optimize the geometrical and process variation for improved JLDGVM performance.

5. CONCLUSION

Multiple electrical characteristics of the JLDGVMs are highly dependent on the JLDGVM design considerations. Considering the scaling of JLDGVM, it is concluded that L_{ch} scaling plays a crucial role in tuning the electrical characteristics such as I_{ON}, I_{OFF} and V_{TH}. Pillar design is also important and most preferable if the silicon pillar has a vertically ultra-thin shape so that the gate controllability can be fully

maximized. Despite of having high performance due to the fully-depleted channel, JLDGVM also suffers undesired degradation effect such as SCEs. Therefore, with process design consideration, these effects can be well monitored and excellent gate controllability could be gained, thus enabling JLDGVM design to be further optimized for better performance, especially from driveability and leakage perspective. Application of doping tuning approach and WF engineering are crucial for attaining desired threshold and lower leakage design. For future work, the JLDGVM design can be further optimized via appropriate optimization methods in order to improve the electrical characteristics. Thus, it is suggested that all of the parameters dependencies on JLDGVM performance should be carefully considered since the junctionless configuration is significantly associated with the geometrical and process parameters.

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