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Simple Three-Input Single-Output Current-Mode Universal Filter Using Single VDCC

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ABSTRACT

This paper presents a second-order current-mode filter with three-inputs and single-output current using single voltage differencing current conveyors (VDCC) along with one resistor and two grounded capacitors. The design of presented filter emphasizes on the use of a single active element without the multiple terminals VDCC which is convenient to implement the VDCC using commercially available IC for the practical test. Also, it can reduce the current tracking error at current output port and can reduce the number of transistors in the VDCC. The proposed filter can realize all the five generic filter responses, namely, band-pass (BP), band-reject (BR), low-pass (LP), high-pass (HP), and all-pass (AP) functions from the same configuration under various conditions in terms of three input current signals. Furthermore, the natural frequency and quality factor are electronically controlled. The output current node exhibits high impedance. Besides, the non-ideal case is also investigated. The simulation and experimental results using VDCC constructed from commercially available IC can validate the theoretical analyses.

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1. INTRODUCTION

Analog filters are an important building blocks for analog signal processing that have a variety of applications in the fields of communication, sound system, instrumentation, control system, etc [1]. The filter which provides several filter responses in the same topology is well-known as the universal filter or multifunction filter. The multifunction filter with multiple inputs and single output is one of the universal filters which have attracted significant research attention [2]. In addition to these, a current-mode (CM) signal processing circuits in which some parameters can be controlled by external currents have low power consumption, greater linearity, a smaller number of components and larger dynamic range, wider bandwidth when compared to voltage-mode counterparts such as operational amplifiers [3]-[4].

The design of an electronic circuit in analog signal processing has gone in the use of the active building block [5]-[9]. Especially, the electronically tunable active building blocks have attracted significant research attention since analog circuits using electronically tunable active building block give more fine-tuning than adjusting the value of passive device. The voltage differencing current conveyors (VDCC) [10] is a recently reported versatile active building block used in the realization of analog signal processing circuits. A very significant advantage of using VDCCs in analog circuit design is that it is able electronic controllability.

Analog circuits using the VDCC as the active element have been found in the literature for examples, the first order allpass filter [11], the ladder filter [12], the passive element simulator [10], [13]-

[16], the square and triangular wave generator [17], sinusoidal oscillator [18]-[21], etc. The VDCC based universal filters have been proposed in [22]-[25]. The three-input single-output (TISO) voltage-mode filter and single-input dual-output (SIDO) voltage-mode filters were presented in [22]. The TISO filter with five filter responses consists of single VDCC, one resistor and two capacitors. The SIDO filters with three filter responses (HP, BP and LP) consist of single VDCC, two resistors and two capacitors. The natural frequency and quality factor for both TISO and SIDO are electronically tuned. Moreover, the tune of quality factor for SIDO filter can be done without affecting the natural frequency. However, the output voltage node doesn't exhibit low impedance, so the voltage buffer is required for cascading. The single-input four-output voltage-mode filter was proposed in [23]. It consists of single VDCC, two resistors and two capacitors. The natural frequency and quality factor are electronically tuned. Moreover, the tune of quality factor can be done without affecting the natural frequency. However, the output voltage nodes don't exhibit low impedance, so the voltage buffer is required for cascading. The current-mode reconnection-less reconfigurable filter was proposed in [24]. It consists of single VDCC, a single dual output current amplifier, a single resister and two grounded capacitors. The natural frequency and quality factor are electronically tuned. The impedance at input current node exhibits low and the impedance at output current node exhibits high which is convenient to cascade in the current-mode circuit without the use of any current buffer. However, this filter can provide only three filter responses (LP, HP and BP). Also, it requires the multiple output terminal active devices. The three-input single-output current-mode universal filter with five filter responses was proposed in [25]. It consists of single VDCC, a single grounded resister and two grounded capacitors. The natural frequency and quality factor are electronically tuned. The impedance at the output current node exhibits high which is convenient to cascade in the current-mode circuit without the use of any current buffer. However, this filter requires the multiple output terminals of VDCC.

The three-input single-output current-mode biquad filter emphasizing on the use of the VDCC is present in this paper. The proposed filter consists of single VDCC, one resistor and two grounded capacitors which are suitable for the chip and off-the-shelf implementation. The natural frequency and quality factor can be electronically adjusted. The simulation results of the proposed filter agree well with the theoretical expectation.

2. THE PRINCIPLE OF OPERATION

2.1. Voltage differencing current conveyor (VDCC)

In this design, the active building block (ABB) called the voltage differencing current conveyor (VDCC) is used as the main active device. The international construction of CMOS VDCC was proposed by Firat et al [10] in 2014. It is five port device namely P, N, Z, X and W port. The high impedance voltage input ports are P and N. The high impedance current output ports are Z and W port. The low impedance voltage output port is X port. In the original version of VDCC, the output current at W port provides the output current both positive and negative direction called Wn and Wp ports. For this purpose, a single W port is required. This can reduce the current tracking error at W port and can reduce the number of transistor in the VDCC. The electrical symbol and the equivalent circuit of the VDCC are shown in Figure 1 (a) and (b). The ideal electrical properties of the VDCC are shown in equation (1).

$$\begin{pmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_W \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{pmatrix} \quad (1)$$

where g_m is the transconductance gain. The VDCC can be constructed from commercially available ICs as shown in Figure 1(c). It consists of LM13700 [26] and AD844 [27]. This construction contains only the single w terminal. The g_m for this construction is given as

$$g_m = \frac{I_B}{2V_T} \quad (2)$$

where I_B is DC bias current and V_T is thermal voltage.

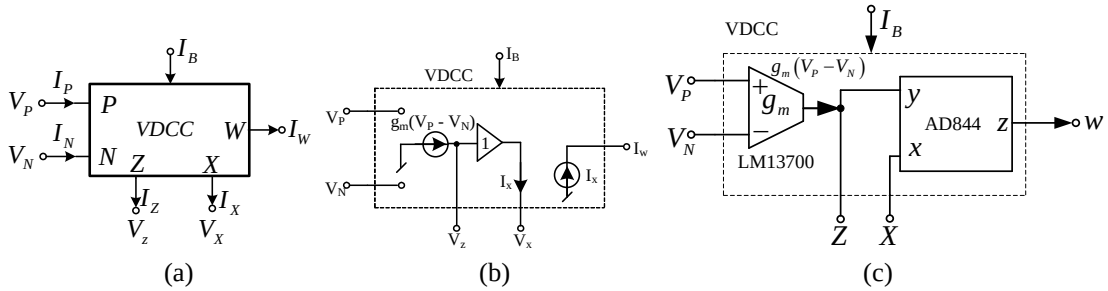

Figure 1. VDCC (a) Circuit symbol of VDCC (b) Equivalent circuit (c) VDCC (without the dual W terminal) constructed from commercially available ICs

2.2. Proposed filter

The proposed filter is shown in Figure 2. It consists of single VDCC, one resistor and two grounded capacitors. There are three input currents, i_{i1}, i_{i2} and i_{i3}. The single output current is i_{out} which exhibits high impedance at the current output node. It is found that the proposed filter doesn't require VDCC with multiple W terminals unlike the current-mode filter using VDCC as the active element presented in [24]-[25]. This makes the VDCC used in the proposed filter is more convenient to construct by using commercially available ICs. Routine analysis of the proposed filter using equation (1) yields the following output current equation

$$i_{out} = \frac{i_{i1} s \frac{1}{C_1 R} - i_{i2}\left(s\frac{1}{C_2 R} + \frac{g_m}{C_1 C_2 R}\right) + i_{i3}\left(s^2 + s\frac{1}{C_2 R} + \frac{g_m}{C_1 C_2 R}\right)}{s^2 + s\frac{1}{C_2 R} + \frac{g_m}{C_1 C_2 R}} \quad (3)$$

From equation (3), the natural frequency and qualigy factor are given as

$$\omega_0 = \sqrt{\frac{g_m}{C_1 C_2 R}} \text{ and } Q = \sqrt{\frac{C_2 g_m R}{C_1}} \quad (4)$$

It is evident from equation (4) that the natural frequency and quality factor can be electronically tuned via g_m.

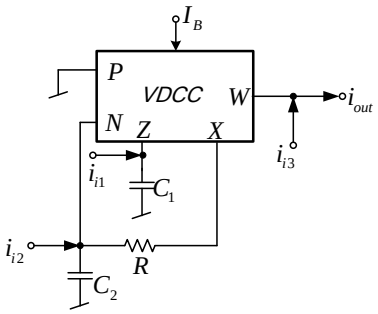

Figure 2. Proposed filter

From equation (3), the derivation of five filter responses can be done as follows:

- The non-inverting band-pass filter response can be obtained by applying the input current to i_{i1} while i_{i2} and i_{i3} being zero (no the input current applying).
- The non-inverting low-pass filter response can be obtained by applying the input current to i_{i1} and i_{i2} while i_{i3} being zero and $C_1=C_2$.
- The non-inverting high-pass filter response can be obtained by applying the input current to i_{i2} and i_{i3}

while i_{i1} being zero.

- The non-inverting band-reject filter response can be obtained by applying the input current to i_{i3} and applying the inverting input current to i_{i1} while i_{i2} being zero.
- The non-inverting all-pass filter response can be obtained by applying the input current to i_{i3} and applying the double inverting input current to i_{i1} while i_{i2} being zero.

3. NON-IDEAL ANALYSIS

In practically, the influent of current/voltage tracking errors and parasitic elements in the VDCC will affect the performances of the proposed filter. For the non-ideal case, the relationship of the terminal voltages and currents of the VDCC can be rewritten as:

$$\begin{pmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_W \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \alpha \end{pmatrix} \begin{pmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{pmatrix} \tag{5}$$

where β is the voltage tracking error from X to Z terminal and α is the current tracking error from X to W terminal. The various ports of VDCC are characterized by parasitic resistances (R_P, R_N, R_Z, R_X and R_W) and parasitic capacitances (C_P, C_N, C_Z, and C_W) as shown in Figure 3(a). Taking parasitic elements in VDCC into account, the proposed circuit in Figure 2 is re-drawn as shown in Figure 3(b). Taking the non-ideal parameters into account, the output current of the circuit in Figure 2 is obtained as

$$i_{out} = \left(\frac{1}{Y_3 R_L + 1} \right) \left[\frac{i_{i1}\alpha\beta Y_2 - i_{i2}\left(\alpha Y_1 + \alpha\beta g_m\right) + i_{i3}\left(Y_1 Y_2 R' + Y_1 + \beta g_m\right)}{Y_1 Y_2 R' + Y_1 + \beta g_m} \right] \tag{6}$$

where $Y_1 = s(C_1+C_z)+G_z$, $Y_2 = s(C_1+C_N)+G_N$, $Y_3 = sC_W + G_W$, $R' = R+R_x$, and R_L is the load resistance. If R_L is low and the operational frequency $f_{op} << 1/C_W R_W$, the output current in equation (6) becomes

$$i_{out} = \frac{\left\{ \begin{array}{l} i_{i1}\left(s\dfrac{\alpha\beta}{C_1' R'} + \dfrac{\alpha\beta G_N}{C_1' C_2' R'} \right) - i_{i2}\left(s\dfrac{\alpha}{C_2' R'} + \dfrac{\alpha G_z}{C_1' C_2' R'} + \dfrac{\alpha\beta g_m}{C_1' C_2' R'} \right) + \\ i_{i3}\left[s^2 + s\left(\dfrac{G_z}{C_1' C_2'} + \dfrac{G_N}{C_2'} + \dfrac{1}{C_2' R'} \right) + \dfrac{G_N G_z + G_z + \beta g_m}{C_1' C_2' R'} \right] \end{array} \right\}}{s^2 + s\left(\dfrac{G_z}{C_1' C_2'} + \dfrac{G_N}{C_2'} + \dfrac{1}{C_2' R'} \right) + \dfrac{G_N G_z + G_z + \beta g_m}{C_1' C_2' R'}} \tag{7}$$

From equation (7), the natural frequency is given as

$$\omega_0 = \sqrt{\frac{G_N G_z + G_z + \beta g_m}{\left(C_1 + C_z\right)\left(C_2 + C_N\right)\left(R + R_X\right)}} \tag{8}$$

Subsequently, the quality factor is given as

$$Q = \left[\frac{\left(C_1 + C_z\right)}{G_z\left(R + R_X\right) + \left(C_1 + C_z\right)\left(R + R_X\right) G_N + \left(C_1 + C_z\right)} \times \sqrt{\frac{\left(C_2 + C_N\right)\left(R + R_X\right)\left(G_N G_z + G_z + \beta g_m\right)}{\left(C_1 + C_z\right)}} \right] \tag{9}$$

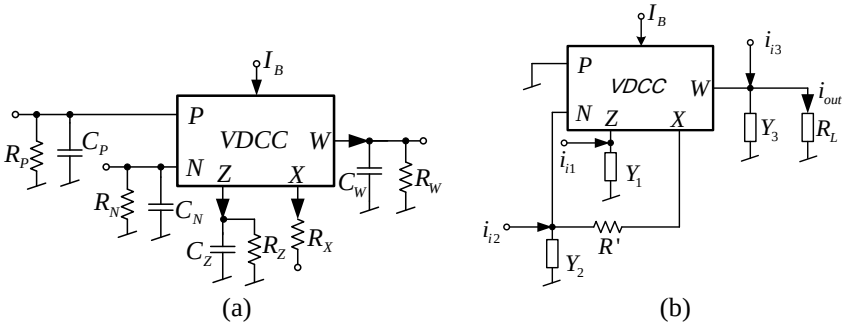

Figure 3. (a) Parasitic elements appeared in VDCC terminals (b) The proposed filter with parasitic elements

4. SIMULATION RESULTS

The simulation was done by using the LM13700 and AD844 PSPICE macro model parameters to confirm the functionality of the proposed filter. The internal construction of the VDCC was constructed as shown in Figure 2(c). The proposed circuit was supplied with symmetrical ±5 VDC, the DC bias current was set as I_B = 52 μA and the passive component values were chosen as R = 1 kΩ and C_1 = C_2 = 1 nF. With mentioned active and passive component values, the theoretical natural frequency and quality factor from equation (4) are respectively obtained as f_0 = 159.23 kHz, Q = 1.

The simulated gain for LP, HP, BP and BR versus frequency response of the proposed filter with mentioned active and passive component values is shown in Figure 4. The simulated natural frequency is 154.88 kHz. The deviation of theoretical and simulated natural frequency is 2.73%. This deviation suffers from the voltage/current tracking error and parasitic elements as analyzed in equation (8). The simulated gain and phase of AP versus frequency response is shown in Figure 5. It is found that phase response changes from 0° to -360° while the magnitude frequency response is constant for all frequencies. The results in Figure 4 and 5 confirm that the proposed circuit can provide five filter responses with the same circuit topology.

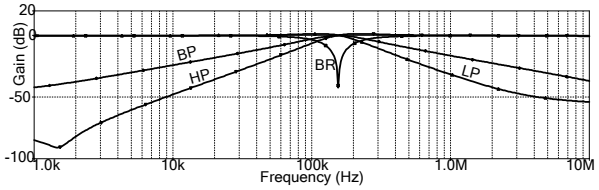

Figure 4. Simulated gain response of the proposed filer

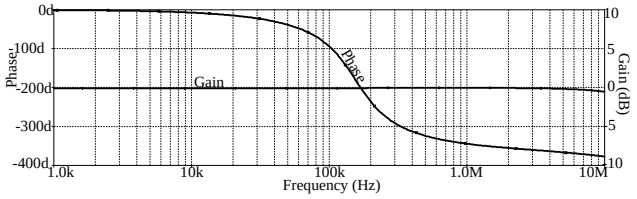

Figure 5. Simulated phase and gain response of all-pass function

The simulated input and output waveform in the time domain for the BP functions is illustrated in Figure 6 when three frequencies, 10 kHz, 154.88 kHz and 1 MHz with 20 μA_{p-p} were applied as input current. It is found that the magnitude of output current has the highest amplitude at f=154.88 kHz. The tuning of phase response for the AP function was tested as shown in Figure 7 by applying the input current as the sinusoidal signal with 20 μA_{p-p} and f=154.88 kHz while the DC bias current was adjusted for three values, 52 μA, 90 μA and 208 μA. It is found that the phase response of AP function can be controllable with constant

amplitude. THD analysis of the proposed current-mode universal filter given in Figure 8 was performed at 154.88 kHz for various sinusoidal peak input.

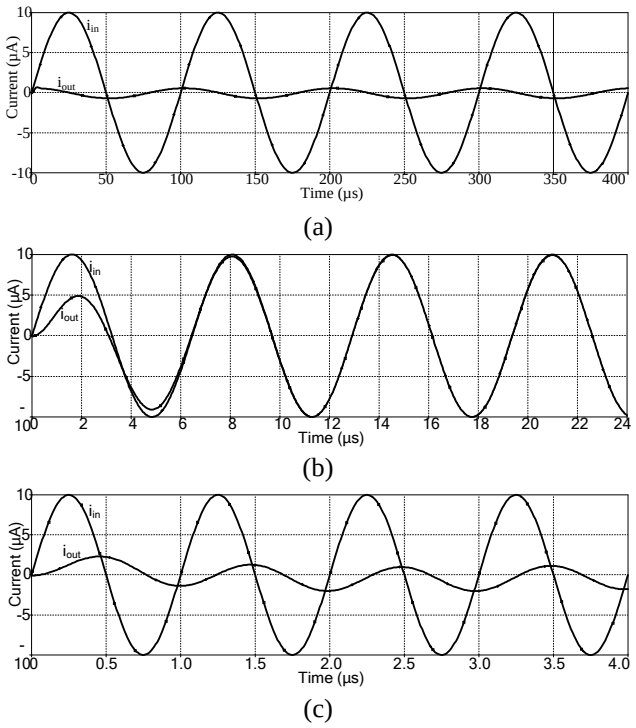

Figure 6. The simulated waveforms of the BP filter at (a) 10 kHz (b) 154.88 kHz and (c) 1 MHz

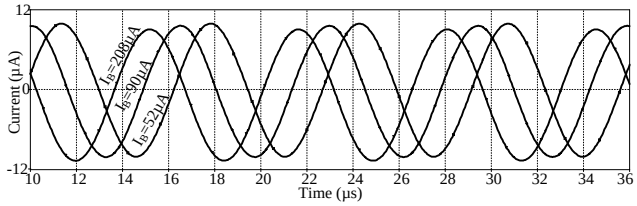

Figure 7. The measured output waveforms of the all-pass filter for different I_B values

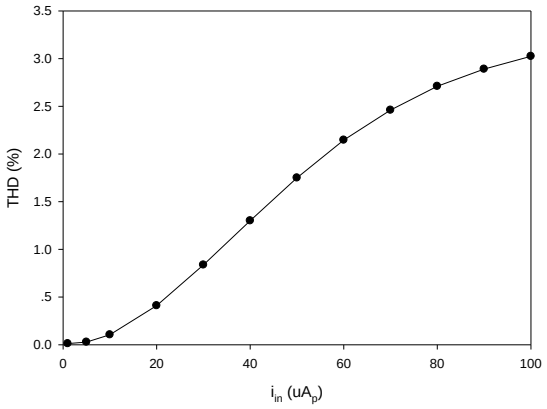

Figure 8. THD variation with respect to applied sinusoidal input current

5. EXPERIMENTAL RESULTS

The proposed filter in Figure 2 was experimentally tested using VDCC construced from the LM13700 and AD844 commercially available ICs as inlustrated in Figure 1(c). The input currents were converted from the input voltage signal by using the AD844 IC and one resistor as shown in Figure 9. The 1kΩ resistor was used as the output load to convert the output current to be the output voltage. The LM13700 and AD844 were biased with a DC supply voltage of ±5V and bias current of I_B = 52µA. All capacitances and resistance were given by 1 nF and 1 kΩ, respectively. The amplitude of input voltage for this test was 50 mV_{p-p}. The experimentally observed frequency response of the LP, HP, BP and BR filter is shown in Figure 10. The measured f_0 was obtained around 160 kHz. The measurement of the input voltage and output voltage dropped at the output resistance load for the BP response is shown in Figure 11. The experimentally measured gain and phase response of the AP filter is illustrated in Figure 12. It is found that experimental results are in well accordance to the theoretical analyses.

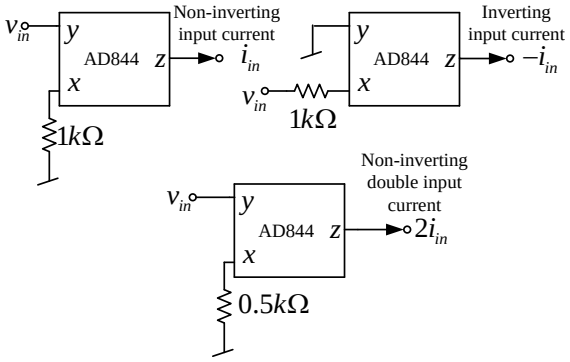

Figure 9. Implementation of input currents using AD844

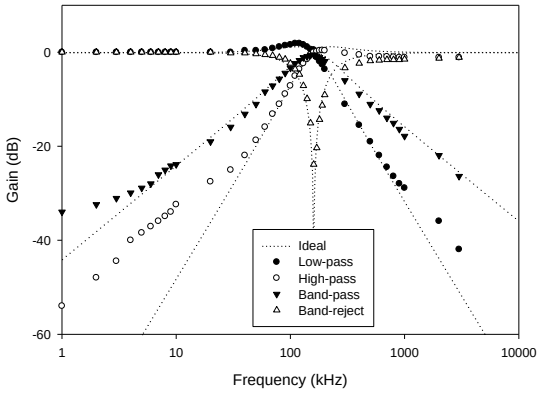

Figure 10. Experimental gain response of the proposed filer

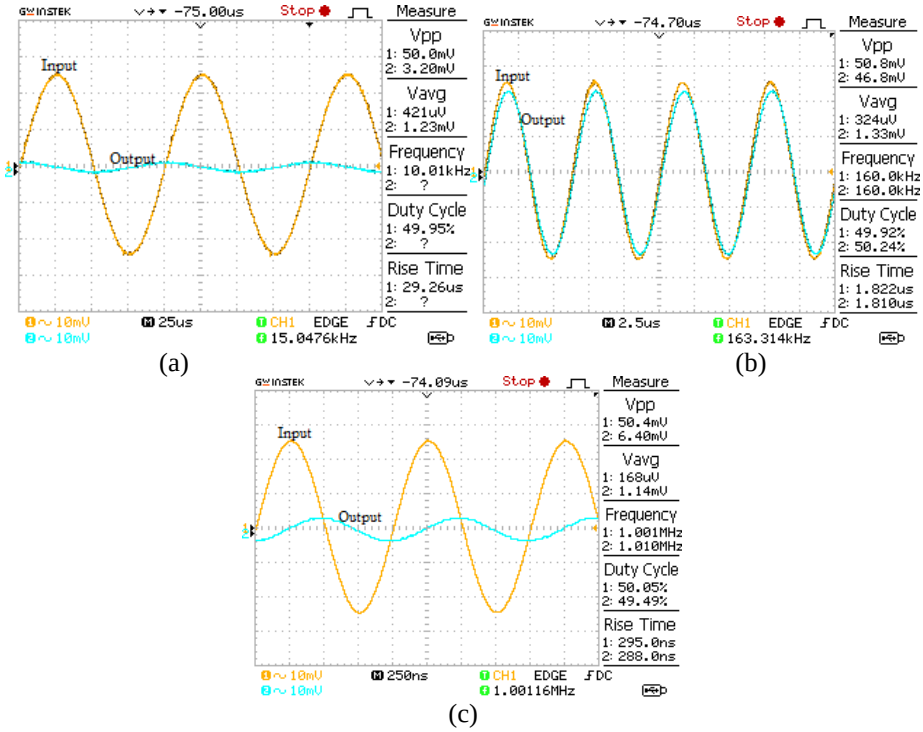

Figure 11. The input and output waveforms of BP filter at (a) 10 kHz (b) 160 kHz and (c) 1 MHz.

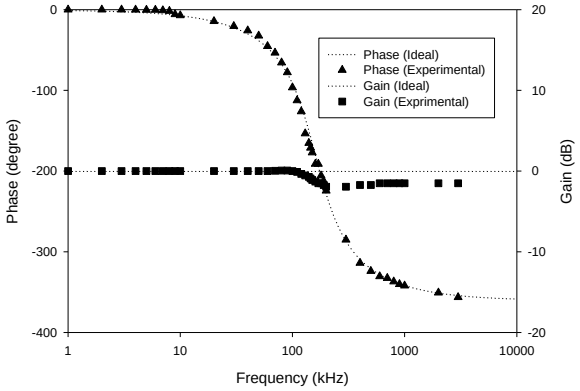

Figure 12. Experimental phase and gain response of the all-pass function

6. CONCLUSION

In this contribution, the three-input single-output current-mode filter is presented. The proposed filter uses only single VDCC as active element. The natural frequency and quality factor can be tuned electronically by changing the bias current of VDCC. Using only VDCC constructed from commercially available ICs, the proposed filter is suitable for off-the-shelf implementation. The workability of the proposed filter is demonstrated by simulation and experimental results.

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