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A Two Channel Analog Front end Design AFE Design with Continuous Time ∑-Δ Modulator for ECG Signal

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ABSTRACT

In this context, the AFE with 2-channels is described, which has high impedance for low power application of bio-medical electrical activity. The challenge in obtaining accurate recordings of biomedical signals such as EEG/ECG to study the human body in research work. This paper is to propose Multi-Vt in AFE circuit design cascaded with CT modulator. The new architecture is anticipated with two dissimilar input signals filtered from 2-channel to one modulator. In this methodology, the amplifier is low powered multi-VT Analog Front-End which consumes less power by applying dual threshold voltage. Type -I category 2 channel signals of the first mode: 50 and 150 Hz amplified from AFE are given to 2nd CT sigma-delta ADC. Depict the SNR and SNDR as 63dB and 60dB respectively, consuming the power of 11mW. The design was simulated in a 0.18 um standard UMC CMOS process at 1.8V supply. The AFE measured frequency response from 50 Hz to 360 Hz, depict the SNR and SNDR as 63dB and 60dB respectively, consuming the power of 11mW. The design was simulated in 0.18 m standard UMC CMOS process at 1.8V supply. The AFE measured frequency response from 50 Hz to 360 Hz, programmable gains from 52.6 dB to 72 dB, input referred noise of 3.5 μV in the amplifier bandwidth, NEF of 3.

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1. INTRODUCTION

ADVANCES in Complementary MOSFET technologies and low powered integrated circuits have stimulated considerable interests in wearable gadgets, anoccurrence which can potentially transfigure the healthcare devices. Sensor interface is the main part in the wearable gadgets, design of which should meet many uncompromising requirements both in digital block and in analog block. In designing AFE circuits, the corporal signals' nature is of much concern. The amplitude of these signals ranges from volts to mV and the frequencies vary from DC to a few kilo Hz, as described in figure 1 [1]. The signals, the AFE should possess lowest input referred noise, reconfigurable bandwidth, and programmable gain to accommodate the weak signals and giant dynamic range. Furthermore, the skin-electrode interface instigates a high DC potential in an input signal that should be minimized by high pass filtration, cutting-off frequencies below 1Hz. While, such a high-pass filter with external capacitors and resistors can be easily implemented [2], it is further cost-effective to integrate the filter on-chip. Switched-capacitor [3] are two possible approaches that could give good trade-offs between performance, power, and area as demonstrated in [4], [5]. It is noteworthy that an approach of pseudo-resistor not only diminishes the area but also ease reconfigurable design of band-pass filters [6]-[9]. A very high variation of resistances could be the drawback in existing pseudo-resistors which

are tunable under negative and positive biased conditions. While working on low-voltage, it leads to a critical DC. In this, recognizing the programmable BE with reconfiguring amplifier the switch in four modes.

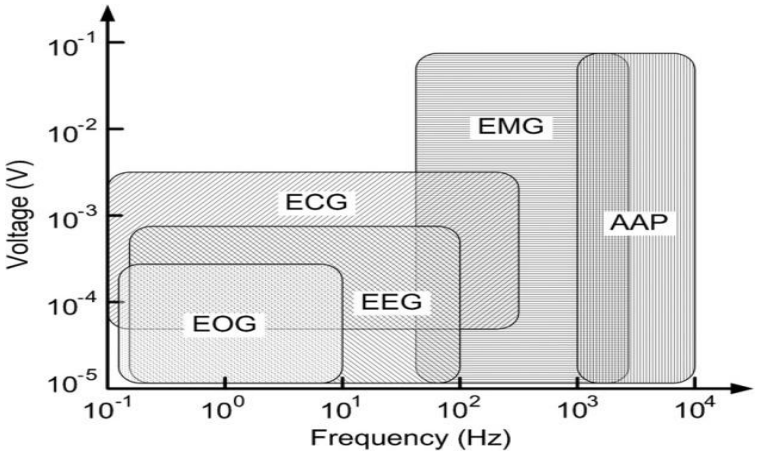

Figure 1. Voltage and frequency ranges of familiar physiological signals

Table 1. Medical Characteristics of the Familiar Physiology

Parameter	Signal Frequency	Standard Sensor
Electroretinography (ERG)	DC ~ 50 Hz	Contact electrode
Electroencephalography (EEG)	DC ~ 150 Hz	Scalp electrode
Electrocardiography (ECG)	0.01 Hz ~ 250 Hz	Skin electrode
Electroneurography (ENG)	250 Hz ~ 5000 Hz	Surface/needle electrode

This paper is sectioned as described hereafter. Section-II depicts a Proposed System level architecture of AFE with Programmable Procedure. An AFE with sigma-delta modulator is delineated in Section III. Results from simulation and related thoughts are furnished in Section IV. Hence, the conclusions are derived under Section V.

2. THE PROPOSED ARCHITECTURE 2- CHANNEL AFE FOR ECG SIGNAL MODULATOR

This paper addresses a chip that comprises a low noise (TB-FEA), a programmable gain amplifier (PGA) and a 10-bitΣΔ (SDM-ADC). The overall gain is programmed through the flip-over-capacitor feedback and proposed reconfiguring in the PGA. This allows the chip to offer FOUR operational modes, ERG, EEG, ECG, and ENG.

The microsystem for acquisition of bio-potential is as shown in figure 2. Bio-signals are amplified by AFE circuits and then they are converted into digital codes by ADCs [3]. In addition, analog multiplexers with large output current are designed to select the corresponding signals to ADCs. A trade-off in the microsystem exists between power and the area. The ratio between count of AFEs and ADCs affects the inclusivefunctioning.

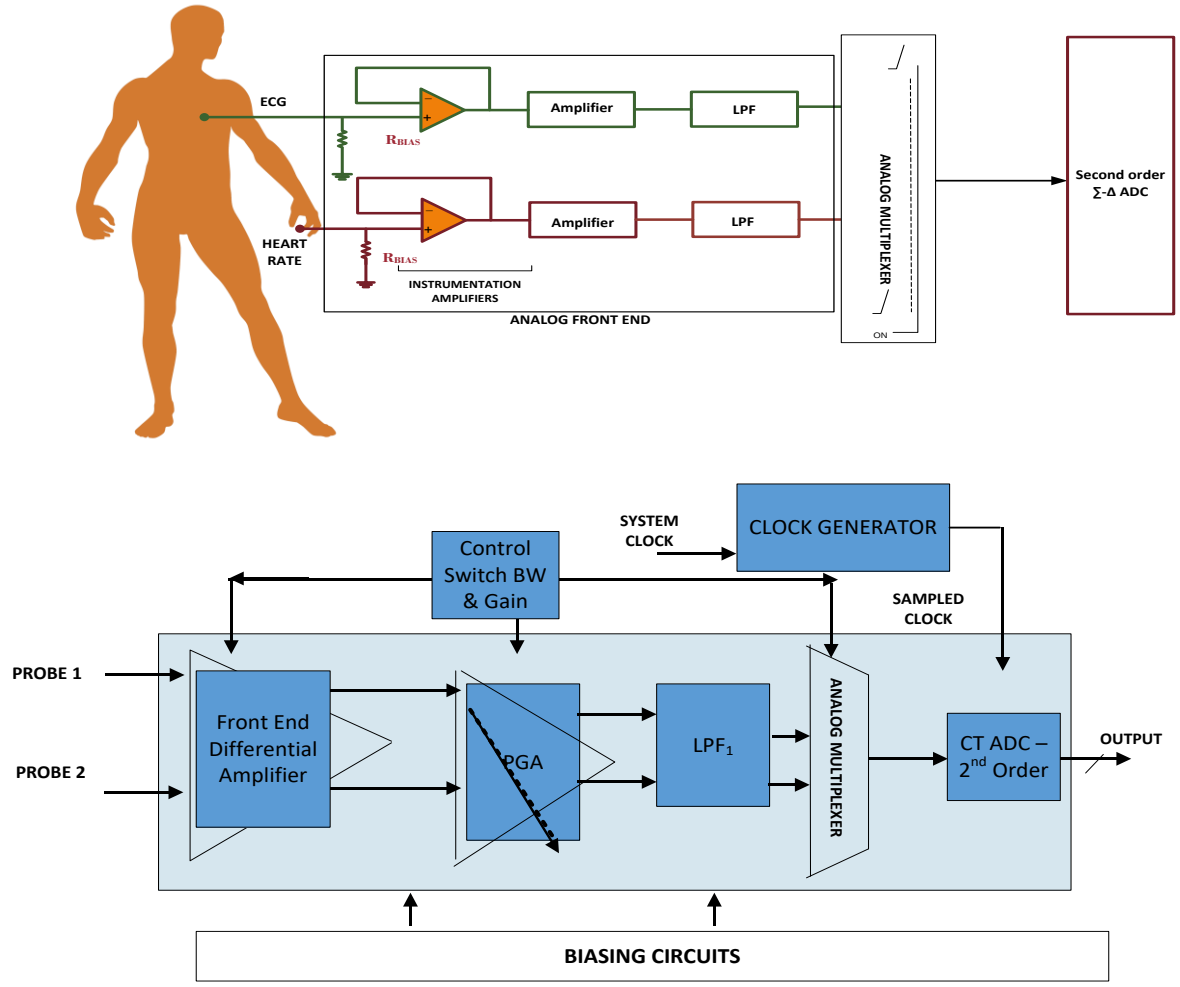

Figure 2. Proposed architecture of 2 channel

2.1. Noise Contribution at AFE design

The Flicker Noise 1/f reduction always remains a challenge in the bio-signal acquisition. This problem cannot be avoided completely 1/f noise exist in all the devices of MOSFET due to their surface conduction mechanism. For a MOS working in saturation region the total flicker noise power spectrum could be calculated as

$$g_m = \sqrt{2.m_{eff}.Cox.\frac{W}{L}.I_{ds}} \quad (1)$$

$$i_f^2 = a_l.\frac{q.m_{f.}(Vgs-Vt).Ids}{L^2.f} \quad (2)$$

The spectral density for a MOSFET is given from [9] as:

$$v_f^2 = \underbrace{4kT\frac{2}{3}\frac{1}{g_m}}_{\text{Thermal}} + \underbrace{\frac{K_f}{WLC_{ox}f}}_{\text{Flicker}} \quad (3)$$

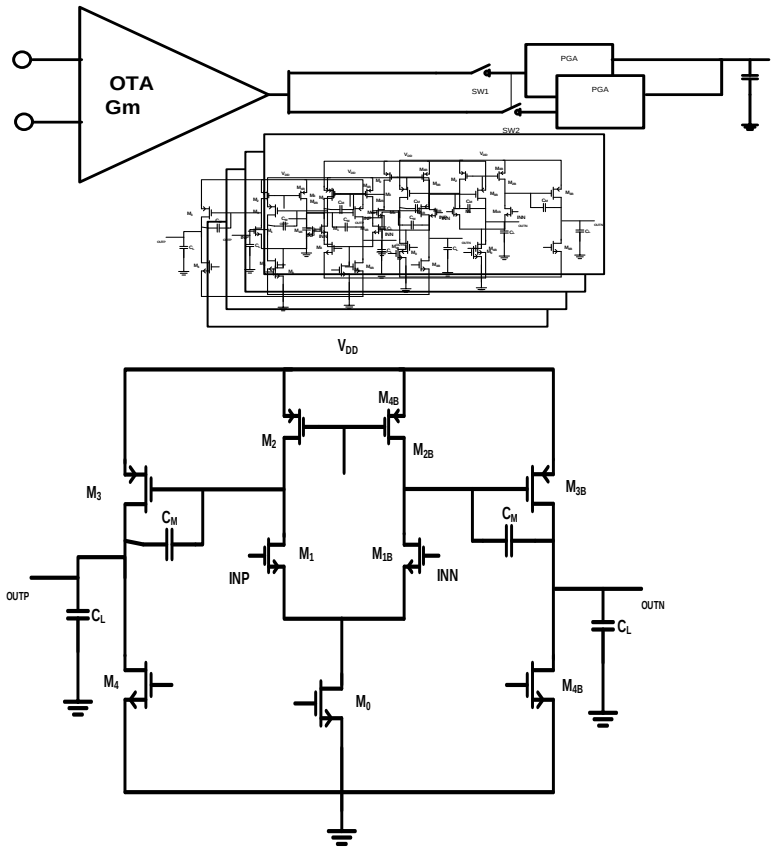

Figure 3. (a) Proposed Block diagram of Programmable two 2 control switches (b) Two-stage load compensated OTA

2.2. A Tunable Bandwidth Low Noise Amplifier in AFE

In the above Figure 2 the entire AFE design for biomedical LNA. The load-compensated amplifier of two-stage was chosen amongst the, OTA due to its power-efficiency, minimum load capacitance and rail to rail output swing for an optimum phase margin and GBW. Figure 3 depicts the two-stage amplifier along with load-compensation.

$$A_0 = g_{m1} R_{out1} \times g_{m5} R_{out2} \quad (6)$$

$$GBW = \frac{g_{m1} \cdot g_{m5} \cdot R_{out1}}{2\pi C_L} \quad (7)$$

Where g_{mi} is the transconductance of the i^{th} transistor, R_{outi} is the output resistance of tenth stage of the OTA. Furthermore it is assumed, all the transistors would work under the saturation region. From Eq. (3), we observe, thermal noise contribution is proportional inversely to transconductance gm. From the EKV model the transconductance normalized with respect to drain current.

$$\frac{g_{m,Strong}}{I_{Ds}} = \frac{12}{V_{eff}} \quad (5)$$

Hence by increasing the drain current I_{ds} and biasing the MOSFET in the weak inversion region of operation the thermal noise suppression is maximized. The most of noise contribution will come from the input signal of the first stage of the amplifier.

Control Switch	Parameter
0	ECG Signal (Heart)
1	Heart Rate (Index Finger)

2.3. Modulator Circuit

The device sizing W/L of input pair should be large to optimize the noise level at input. The OTA which acts as the key component in the modulator is used by the integrator and must possess high gain for smooth integration. The general two-stage amplifier consists of the single-ended differential amplifier having high gain, biasing circuit, compensation circuit and the second gain stage, as shown in the Figure 4. The basic OTA architecture includes a differential amplifier which has high gain with dominant pole. The second stage employs a common source amplifier. A unity follower with high frequency is used in the third stage. The differential amplifier is usually used as the first stage in amplifier with differential input and single ended output. The second stage is the most desirable stage for a high output swing and it also increases the gain. Although the gain increases, the bandwidth reduces and hence the designers would have to decide in this trade-off. To maintain the stability of the amplifier when negative feedback is given, the Compensation Circuit is employed.

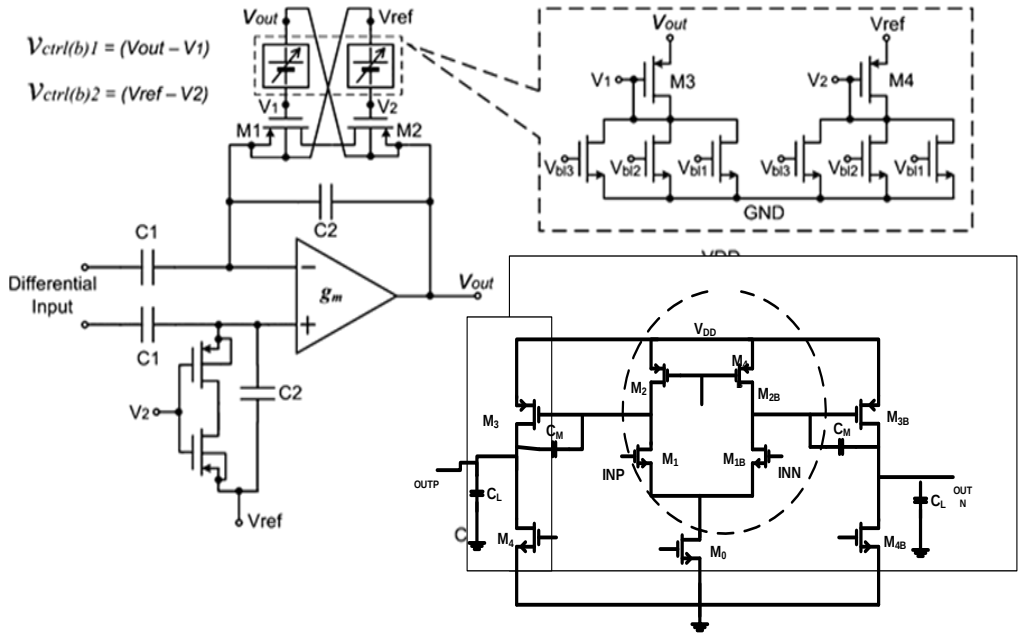

Figure 4. Schematic of Tunable Bandwidth with balanced pseudo-resistor replicas

In this circuit, the load-compensation technique is second-hand which is distinct as the compensation in which the compensator act on the output signal after it had generated feedback signals. The load-compensation is conceded using a Cc and Common-mode Feedback (CMFB) system. Preliminary transients in the output occur due to the time is taken by the CMFB circuit to be effective and to bring the common mode DC output to the desired voltage, halfway sandwiched between the supply rails in this case. The gain of the OTA was originated to be 72 dB and the UGB for this configuration was 25 KHz. The phase margin measured is 73°. In the schematic of OTA, as shown in Figure 4, the bottom circuit that consists of transmission-gate switches is CMFB circuit, whereas; the two-stage OTA is the CMOS circuitry above feedback system.

3. DISCUSSION OF RESULTS

The proposed architecture is Instrumental analysis with practical simulation on 0.18μm UMC CMOS technology the results are observed as shown in the above respective figures. The input impedance has great value (>100GΩ) ECG lies on (3 Hz - 10 Hz). The input voltage is 10 m to 100 mV is amplified with chopping technique, further amplified with multi-VT technique, the power consumption of this AFE Instrumental amplifier is depicted in the Pie chart.

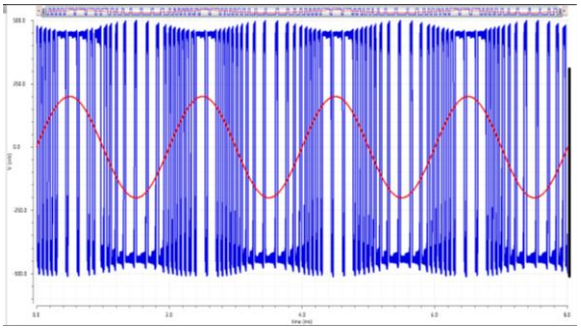

Figure 8. Transient Analysis of signal of 0.2 V and frequency of 500 Hz modulator

Table II. Performance of two different Modulators

Parameter	Mode A	Mode B
Technology	0.18µm CMOS	
Supply Voltage	1 V	
Sampling Frequency	64 kHz	32 kHz
Signal Bandwidth	250 Hz	50 Hz
Oversampling ratio	128	320
Peak SNR	63 dB	85 dB
Dynamic Range	58.5 dB	73 dB
Power Consumption	990 nW	685 nW
FOM pJ/step	.175	0.878
FOM_S	137.43	129.20

The gain is 52.6 dB and 72 dB. An output noise of Low Noise AFE is simulated with QPSS is shown in Figure 6. The SNR measured SNR, SNDR, and ENOB of whole design with four different modes of 2nd order CT Σ-Δ modulator) ADC resolution and dynamic range requirements are shown in the Figure 7 and Figure 5. Table III compares the achieved design performance with recent prior art. Conventionally, NEF is used for comparison.

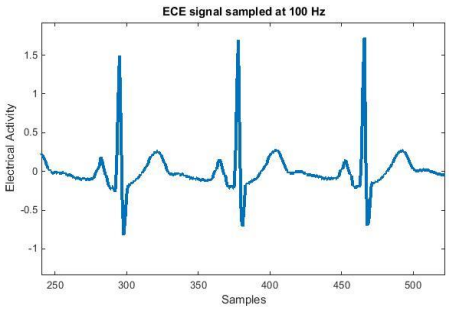

Figure 5. The ECG signal sample at 100Hz

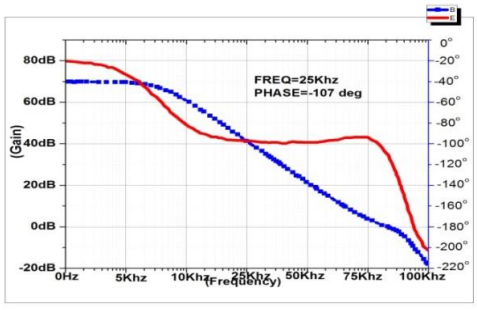

Figure 6. Gain and Phase Margin of an amplifier

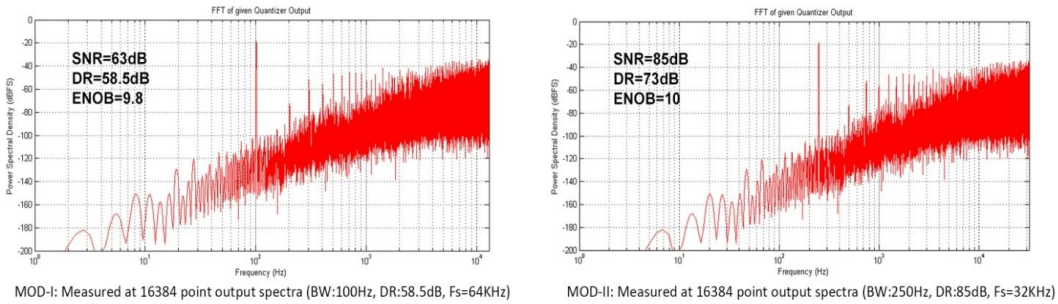

Figure 7. SNR Plots

$$NEF = Vrms, in\sqrt{\frac{2\,I\,total}{\pi V_t.4kT.Bandwidth}} \quad (8)$$

where $Vrms_{in}$ is the input-referred noise, $I_{total}$is the total current, is the thermal voltage, and BWis the bandwidth of the AFE with chopping technique.Usually AFE circuits attain a NEF of 2.5 to 10. The complete layout design with IO pad of the 2 channel AFE with modulator is shown in Figure 8. The Area occupied by the filter is 209.41 µm × 80.21 µm = 0.0167 mm^2.

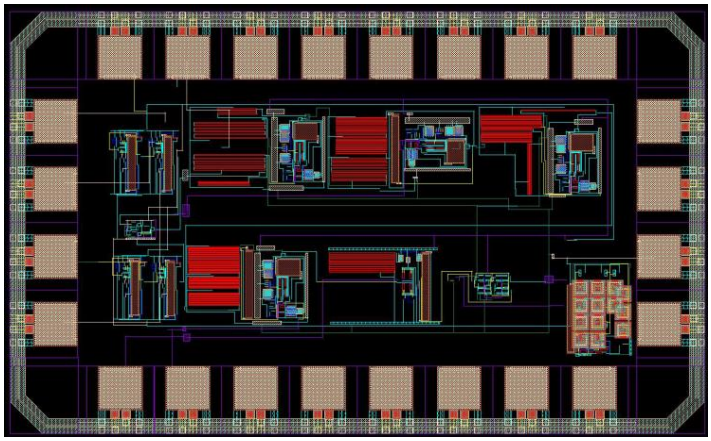

Figure 8. Final Layout of AFE with Dual Sigma-Delta Modulator

Power role of the different blocks is shown in Figure 9. As seen in Figure, more than half of the power budget is dedicated to the different mode of 2nd order CT Σ-Δ modulator. The chopping switch and clock generator are consumed more power when compared to amplifier due to noise considerations.

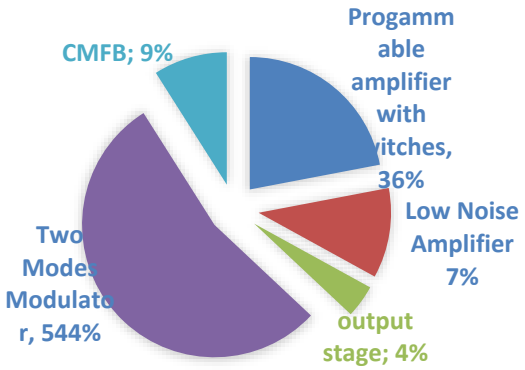

Figure 9. Power Consumption and distribution in Pie chart of whole design

Table III. Comparison of PRIOR ART

Parameter	[7]	[8]	[9]	[11]	This Work
Tech.(µm)	0.5	0.18	0.8	0.13	0.18
Supply (V)	2.8	1.5	1.8	1.2	1
Bias (nA)	743	5000	1050	580[a]/902[b]	500
Gain (dB)	40.9	40.8	41-50.5	40-83	52.8-72
Input Ref.Noise(µVrms)	1.66	1.27	0.98	2.06	3.5
HPF (Hz)	0.4	0.5	0.05- 0.4	0.17	0.1
LPF (KHz)	0.045-5.3	0.1-0.4	0.120	0.34-7.5	7.0
NEF	3.21	6.1	4.6 – 5.4	3.28[a]/4.1[b]	3.04

4. CONCLUSION

In this paper, a 2-channel ECG amplifier with appropriate features for dry and non-contact biopotential applications is presented. Unable to compare the complete design with other design this paper proposed the architectural system level design which is suitable for biomedical application targeted to ECG for 10 mV to 100 mV. Especially, in this paper the multi-VT concept is implemented in the circuit level which reduces the power consumption and the gain achieved by amplifier 52.9dB and 72 dB with an NEF 3.0, noise performance is satisfactory. Furthermore, another important approach the two different 2nd order CT Σ-Δ modulator to improve the performance.

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