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Threshold voltage roll-off for sub-10 nm asymmetric double gate MOSFET

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ABSTRACT

Threshold voltage roll-off is analyzed for sub-10 nm asymmetric double gate (DG) MOSFET. Even asymmetric DGMOSFET will increase threshold voltage roll-off in sub-10 nm channel length because of short channel effects due to the increase of tunneling current, and this is an obstacle against the miniaturization of asymmetric DGMOSFET. Since asymmetric DGMOSFET can be produced differently in top and bottom oxide thickness, top and bottom oxide thicknesses will affect the threshold voltage roll-off. To analyze this, thermal emission current and tunneling current have been calculated, and threshold voltage roll-off by the reduction of channel length has been analyzed by using channel thickness and top/bottom oxide thickness as parameters. As a result, it is found that, in short channel asymmetric double gate MOSFET, threshold voltage roll-off is changed greatly according to top/bottom gate oxide thickness, and that threshold voltage roll-off is more influenced by silicon thickness. In addition, it is found that top and bottom oxide thickness have a relation of inverse proportion mutually for maintaining identical threshold voltage. Therefore, it is possible to reduce the leakage current of the top gate related with threshold voltage by increasing the thickness of the top gate oxide while maintaining the same threshold voltage.

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1. INTRODUCTION

The study on the reduction of transistor size is the biggest issue in the semiconductor industry. The reduction of transistor size doesn't only have advantages in the economical aspect such as productiveness improvement by the increase of packing density and competitiveness increase by reduction of the unit cost, but also plays a large part of performance increase such as the increase of operation speed and improvement of the device reliability by low power consumption in the technological aspect.

Therefore, major transistor businesses are accelerating the invention of ultrafine transistor to be applied to system semiconductor integrated circuits, as well as to memories. However, in the transistors of the existing CMOSFET structure, there are difficulties in producing sub-10nm transistors, because of problems such as threshold voltage roll-off, subthreshold swing degradation, and the intensification of drain induced barrier lowering. To solve these problems, not only new devices using GNR (Graphene Nanoribbon) [1], but also multiple gate MOSFETs using silicon have been studied [2, 3].

Multiple gate MOSFET is the structure that is able to reduce the above-mentioned short channel effects by improving the control ability of the carrier through positioning more than 2 gate terminals around the channel which can control the flow of carrier within the channel [4]. It is divided into tri-gate structure such as FinFET structure [5], double gate structure [6], and cylindrical structure [7], according to the methods of positioning the gate terminals around the channel. It is known that the structures are different but

the basic operations are same. The study will be done about double gate (DG) MOSFET, the simplest structure among them.

DGMOSFET is the structure that makes gate terminals in top and bottom. There are symmetric DGMOSFET which has the same top/bottom structures, and asymmetric DGMOSFET which is produced for controlling short channel effects more efficiently by making top and bottom gate oxide structures different. Dutta et al. reported a threshold voltage model that does not include tunneling current for asymmetric DGMOSFETs [8]. In addition, Munteanu et al. analyzed tunneling currents only for symmetric double-gate MOSFETs [9]. However, since the tunneling current is a significant factor in sub-10 nm, this paper proposes a threshold voltage model including the tunneling current for the asymmetric DGMOSFET in order to consider the effect on the top and bottom gate oxide thicknesses. Although the asymmetric DGMOSFET is the device developed for deducing short channel effects, the short channel effects by tunneling current cannot become ignored in case of reducing the channel length to sub-10nm. Therefore, this study will observe threshold voltage roll-off with tunneling effects according to the change of top and bottom gate oxide thicknesses of asymmetric DGMOSFET and the change of channel silicon thickness. Koh et al. presented the dependence of threshold voltage on the gate oxide thickness, taking into accounting gate leakage current [10]. A method for reducing the gate leakage current due to the decreasing the thickness of gate oxide film will also be discussed. For this, the model of Ding et al. [11] who induced a series form of hermeneutic potential distribution model from Poisson's equation was used, and WKB (Wentzel-Kramers-Brillouin) approximation was used for inducing the tunneling current model.

In section 2, the tunneling current model, which was calculated using potential distribution induced basically by Ding's model and WKB approximation, will be explained. Section 3 will analyze threshold voltage roll-off according to the changes of oxide and silicon thickness using induced current model, and the conclusion will be made in section 4.

2. CURRENT MODEL OF ASYMMETRIC DGMOSFET

Figure 1 shows the schematic sectional diagram of asymmetric DGMOSFT including the relations of tunneling current (I_{tunn}) and thermionic emission current (I_{ther}) to potential energy. As shown in Figure 1, off-current is composed of thermionic emission current and tunneling current, and the flow of the carrier in the channel will be controlled by gate voltage. Especially, the factor to affect the flow of the carrier is the oxide capacitance which changes according to the oxide thickness of top and bottom gates.

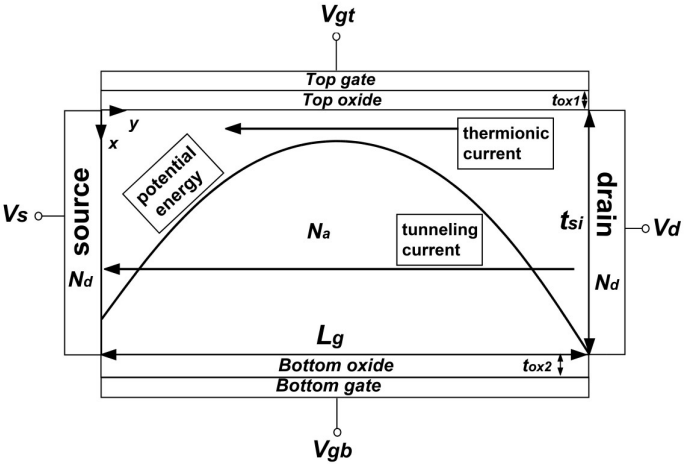

Figure 1. Schematic sectional diagram and currents of asymmetric double gate MOSFET

Because silicon dioxide is generally used as oxide film and the permittivity is fixed, the biggest factor to affect the oxide capacitance is the oxide thickness. Therefore, threshold voltage roll-off will be observed by watching the carrier flow which is changing according to the oxide thickness. For this, potential distribution is calculated using Poisson's equation at first. Different from already published papers [12, 13], constant charge distribution was used. This is because the charge distribution can be ignored due to the very small number of charges inside the channel in sub-10 nm DGMOSFET. In case that potential distribution model using constant doping distribution is used, Poisson's equation is represented as following.

$$\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} = \frac{qN_a}{\epsilon_{si}} \quad (1)$$

Here, ϵ_{si} is the permittivity of silicon, and N_a is the doping concentration of channel doping. The solving process of (1), thermionic emission current, and tunneling current model were already represented in previously published paper [14]. Total off-currents are as following.

$$I_{tot} = I_{ther} + I_{tunn} \quad (2)$$

In case that the value calculated in (2) is 0.1 μA/μm, top gate voltage is defined as threshold voltage [15]. Afterwards, threshold voltage roll-off will be calculated by using the oxide thickness of top/bottom gate and silicon thickness as parameters, and the effect of structural parameters on threshold voltage will be considered.

3. THRESHOLD VOLTAGE ROLL OFF ASYMMETRIC DGMOSFET

In order to demonstrate the validity of the model explained in section 2, 2D simulation results [9] were compared with the results of this paper in Figure 2. Because the case of ϕ_m=4.6 V resulting from being calculated with a parameter of the work function of gate material is consistent with 2D simulation result as shown in Figure 2, this study will analyze threshold voltage roll-off using ϕ_m=4.6 V. In addition, even though the complicated Gaussian distribution function was not used like in the previously published papers [12, 13], threshold voltage roll-off was consistent well as the result of comparison. So threshold voltage roll-off will be considered by (2) using the potential distribution model of this study and threshold voltage defined in TCAD.

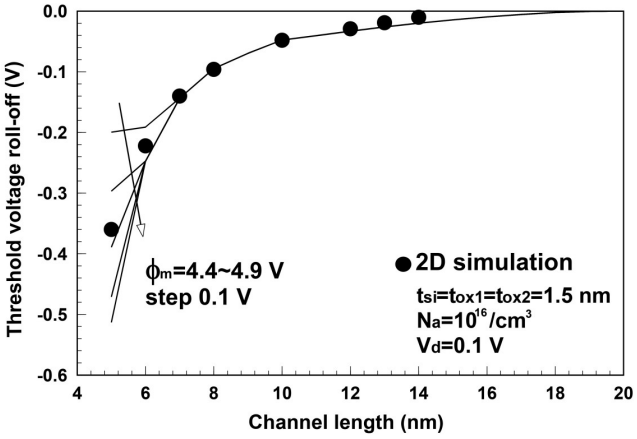

Figure 2. Threshold voltage roll-off of this model (solid line) and 2D Medici simulation (dot) under given conditions

The result of calculating threshold voltage roll-off according to the change of bottom gate oxide thickness was shown in Figure 3 under the given condition. It was found that threshold voltage roll-off changed into approximately -0.52~-0.28 V according to bottom gate oxide thickness, as the result of calculating off-current including tunneling current when the thickness of top gate oxide and silicon was fixed at 1.5nm and the channel length was changed from 10 nm to 5nm. However, in the case of not including tunneling current, threshold voltage roll-off was -0.28 V~-0.12 V, which shows a sensible difference. Especially as channel length gets shorter, the change of threshold voltage roll-off according to the change of oxide thickness appears more greatly. As the channel length decreases, the threshold voltage roll-off due to the tunneling effect is further exacerbated. Moreover, as channel length gets shorter, oxide thickness influences threshold voltage roll-off more sensitively. Even when parameters of top/bottom oxide thickness were exchanged mutually, the same result was induced. Figure 3 shows, it can be found that threshold voltage roll-off increases if bottom oxide thickness increases. Therefore, in order to decrease threshold voltage roll-off, oxide thickness should be made as thin as possible during the manufacturing process.

Like the above, because tunneling current cannot ignore in condition of sub-10nm, from now on, only threshold voltage roll-off including tunneling current will be considered.

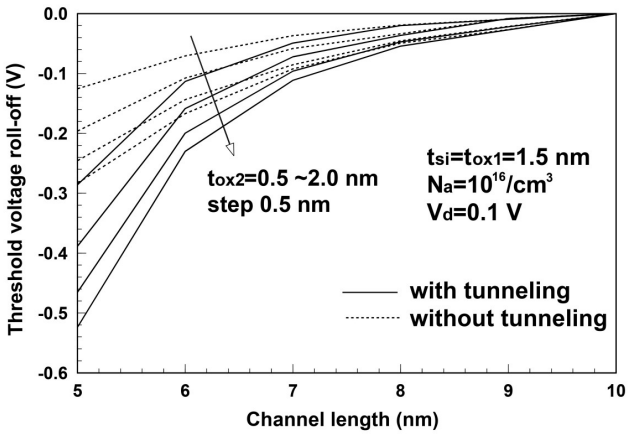

Figure 3. Threshold voltage roll-off for channel length with bottom gate oxide thickness as a parameter

Short channel effects occur according to silicon thickness making up channel, as well as channel length. To observe this effect, after top/bottom oxide thickness is fixed at 1.5nm, threshold voltage roll-off including tunneling current is illustrated in Figure 4 with silicon thickness changing from 1 to 4 nm. As shown in Figure 4, it can be observed that threshold voltage roll-off decreases greatly in case that silicon thickness decreased. It can be observed in the Figure 4 that when channel length decreases from 10nm into 5nm, threshold voltage roll-off is approximately -0.3 V in 1 nm of silicon thickness and increases to -1.9 V in case that silicon thickness increases to 4nm. That is, as silicon thickness increases, short channel effects appears greatly. As shown in Figure 4, it is comprehensible that threshold voltage roll-off, in case of channel length decreasing from 10 nm into 5 nm, increases nearly twice if silicon thickness increases by 1 nm. If Figure 3 and Figure 4 are compared, it can be found that not oxide thickness but the change of silicon thickness affects threshold voltage roll-off more greatly. Like the above, because threshold voltage roll-off is great if silicon thickness increases to 4nm in sub-10 nm DGMOSFET, silicon thickness in designing DGMOSFET should be as thin as possible in production process.

In order to observe the effect of silicon thickness and oxide thickness on the threshold voltage roll-off in detail, Figure 5. shows the contour plot of the tunneling current and the thermionic current according to the channel dimension change under the same bias condition as Figure 3 and Figure 4. As shown in Figure 5, the thermionic current is dominant over the tunneling current when the channel length is near 10 nm. However, when the channel length is reduced to 5 nm, the tunneling current increases with the increase of the total drain current.

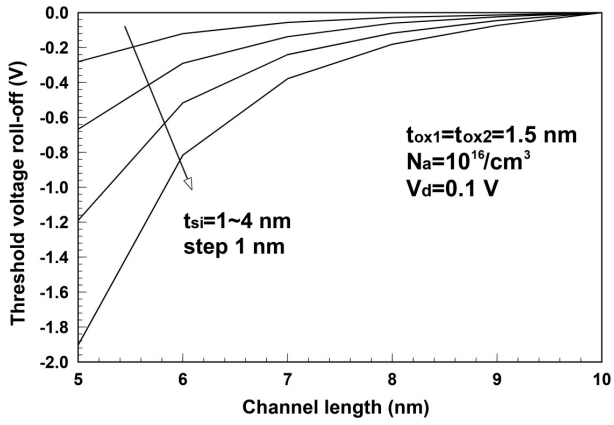

Figure 4. Threshold voltage roll-off for channel length with silicon thickness as a parameter

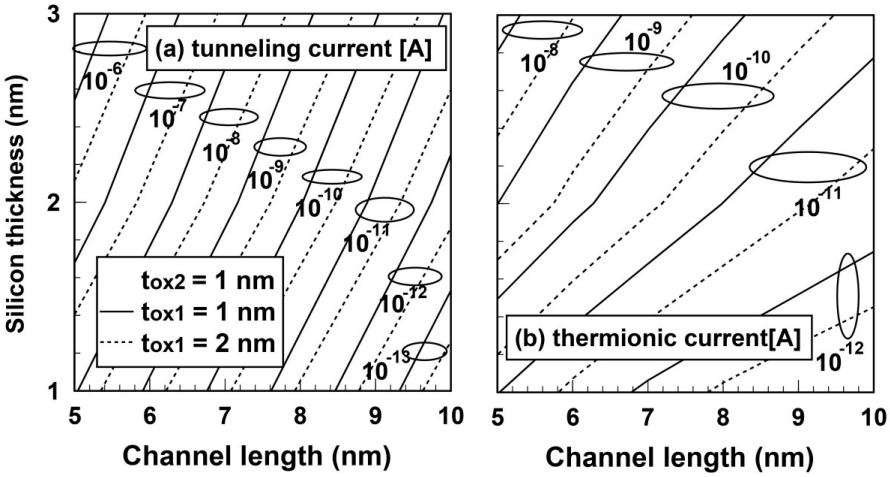

Figure 5. Contours of (a) tunneling current and (b) thermionic current for silicon thickness and channel length with top gate oxide thickness as a parameter

The increase in the tunneling current greatly reduces the threshold voltage, which significantly increases the threshold voltage roll-off. Comparing with the variations of the tunneling current with respect to the change of the silicon thickness and the oxide film thickness in Figure 5(a), it can be found that silicon thickness variation has a greater impact on threshold voltage roll-off than oxide thickness variation.

As considered in Figure 3 and Figure 4, channel length and silicon thickness affect threshold voltage roll-off greatly. To consider the effect of channel length and silicon thickness on threshold voltage roll-off more closely, threshold voltage is illustrated in Figure 6 in the condition that bottom gate oxide thickness is given as parameter. As shown in Figure 6, as the silicon thickness increases, threshold voltage decreases greatly. Also, it can be found that as the channel length gets shorter, threshold voltage roll-off occurs very seriously. Especially, if channel length gets shorter, threshold voltage roll-off according to bottom gate oxide thickness occurs more remarkably. As mentioned in Figure 3, it can be found that as bottom gate oxide thickness gets thinner, threshold voltage roll-off decreases, and as bottom gate oxide thickness gets thicker, threshold voltage roll-off increases.

In case that channel length is very short like nearly 7 nm, minus threshold voltage is indicated over 3 nm of silicon thickness according to bottom gate oxide thickness. However, it can be comprehensible in Figure 6 that minus threshold voltage appears even over 5 nm of silicon thickness if channel length gets longer by 10 nm. Because operation of DGMOSFET is changed into enhancement mode or depletion mode if threshold voltage is changed into minus and plus, the design should be made very carefully. Because such phenomenon.

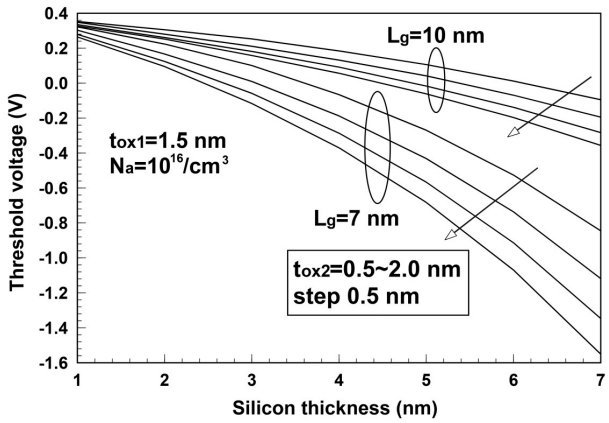

Figure 6. Threshold voltages for silicon thickness with a parameter of bottom gate oxide thickness. Occurs greatly in particular as oxide thickness increases, it is needed that oxide thickness is produced to be thin

The ranges of channel length and silicon thickness for sub-10 nm DGMOSFET to have 0.3 V of acceptable threshold voltage are indicated in Figure 7, in the ranges of top/bottom gate oxide thickness between 0.5 nm and 2 nm. As mentioned in Figure 3, it can be observed in Figure 7 that the result is consistent even though top and bottom gate oxide thicknesses are switched into each other. That is, it can be found that top and bottom gate oxide thicknesses for maintaining consistent threshold voltage are in inverse proportion. As shown in Figure 7(a), DGMOSFET with 0.3V of threshold voltage can be designed only when top/bottom gate oxide thickness should be sub-0.5 nm in case of sub-6 nm of channel length. However, because producing sub-0.5 nm of silicon dioxide film can bring difficulties in the process, the research and the process development of new oxide film should be made. Figure 7(b) is the contours to silicon thickness that threshold voltage in the change of top/bottom gate oxide thickness of simulation range under the given conditions satisfies 0.3V. As it can be also known in Figure 7(b), silicon thickness for having 0.3V of threshold voltage in 8 nm of channel length should be in the range of between 1 nm and 2 nm. It should be carefully considered in designing sub-10 nm of DGMOSFET because threshold voltage changes more responsively according to silicon thickness in comparison of Figure 7(a) and Figure 7(b).

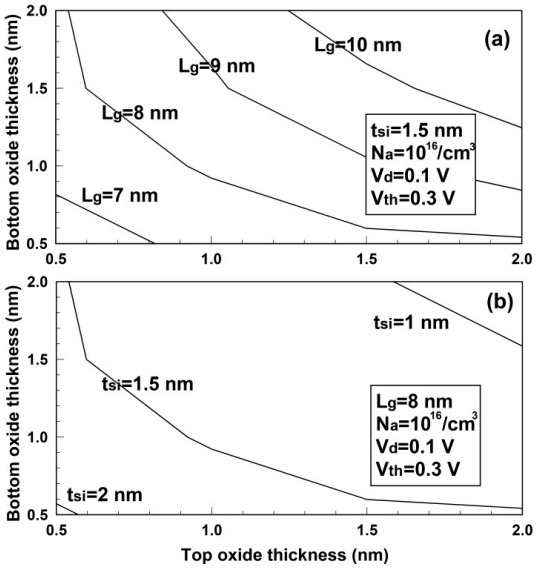

Figure 7. Contours for threshold voltage of 0.3 V for top and bottom gate oxide thickness in the case of (a) $t_{si} = 1.5\ nm$ and (b) $L_g = 8\ nm$.

4. CONCLUSION

We have analyzed the threshold voltage roll-off for asymmetric DGMOSFET that has been developed to reduce the short channel effect due to transistor size reduction. When the channel length is reduced to 10 nm or less, the threshold voltage roll-off phenomenon is inevitable even in a multi-gate MOSFET. Especially, for asymmetric DGMOSFETs, we analyzed the threshold voltage roll-off phenomenon including the tunneling current for the top and bottom gate oxide thickness variations. As a result, it was observed that the threshold voltage roll-off phenomenon was intensified by the tunneling current. The effect of the tunneling current has a great influence on the threshold voltage roll-off with the increase of the oxide film thickness, the increase of the channel thickness and the decrease of the channel length. In order to maintain the same threshold voltage, top gate oxide thickness was inversely proportional to bottom gate oxide thickness and vice versa for the DGMOSFETs with asymmetric oxide thicknesses regardless of the channel length and thickness. That is, even if the top and bottom gate oxide films are formed asymmetrically, it is possible to maintain the same threshold voltage as in the case of the symmetric type. As the channel length decreases, the thickness of the oxide film also decreases, which causes a serious problem of parasitic current at the gate terminal. However, in the asymmetric structure, the gate leakage current at the top gate can be decreased by increasing the thickness of the top gate oxide film related to the threshold voltage and decreasing bottom gate oxide thickness in order to maintain a constant threshold voltage. This result will be the basis of the technology that will lead to the miniaturization of the asymmetric DGMOSFET and will contribute to the improvement of the performance of the integrated circuit such as the system semiconductor.

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