International Journal of Electrical and Computer Engineering (IJECE)
Vol. 8, No. 6, December 2018, pp. 4863~4870
ISSN: 2088-8708, DOI: 10.11591/ijece.v8i6.pp4863-4870

Designing a Novel High Performance Four-to-Two Compressor Cell Based on CNTFET Technology for Low Voltages

Mehdi Bagherizadeh[1], Mona Moradi[2], Mostafa Torbi[3]
[1, 3]Department of Computer Engineering, Rafsanjan Branch, Islamic Azad University, Iran
[2]Young Researcher and Elite Club, Roudehen Branch, Islamic Azad University, Iran

Article Info

Article history:

Received Apr 15, 2018
Revised Jul 29, 2018
Accepted Aug 13, 2018

Keyword:

Carbon nanotube field effect transistor (CNTFET)
Four-to-two compressor
High speed
Low power
Nano electronic
Nanotechnology

ABSTRACT

Compressor cell is often placed in critical path of multiplier circuits to perform partial product summation. Therefore, it plays a significant role in determining the entire performance of multiplier and digital system. Respecting to the necessity of low power design for portable electronic, designing a low power and high-performance compressors seems to be a good solution to overcome of these problems for computations. In this paper a novel high performance four-to-two compressor cell is proposed using Carbon Nanotube Field Effect Transistors (CNTFETs) technology. The new cell is based on Majority Function, *NO*R, and *NAND* gates. The main advantage of proposed design in comparison with former cells is the ease of obtaining *CARRY* output by means of Majority function. Simulations have been done with 32nm technology node using Synopsys HSPICE software. Simulation results confirm the priority of the proposed cell compared to other state-of-the-art four-to-two compressor cells.

Corresponding Author:

Mehdi Bagherizadeh,
Department of Computer Engineering,
Rafsanjan Branch, Islamic Azad University,
Rafsanjan, Iran.
Email: m.bagherizadeh@srbiau.ac.ir

1. INTRODUCTION

Today, in VLSI systems fast arithmetic computation structures such as multipliers and adders are the most frequently utilized circuits [1], [2]. Multipliers are the most significant parts of arithmetic circuits from in terms of performance and power. Digital signal processors and microprocessors rely on the effective implementation of floating point units and common arithmetic logic units to perform dedicated algorithms such as filtering and convolution. In many of these applications, multipliers are considered as the critical part dictating the overall circuit performance when constrained by computation speed and power consumption. Multipliers commonly include three sub functions: 1) partial product generation; 2) partial product reduction; 3) final addition with carry propagating [3]. Compressor cells are generally employed in multi-operand adders to reduce the number of operands and in multipliers. These cells are used to reduce the number of partial products. In the design of the multiplier units the four-to-two compressors are the most wide used modules [4]-[6].

The needs of scaling down the size of transistor in Nano ranges in current MOSFET technology leads to some challenges such as reliability, power consumption, less control of the gate, leakage power and high lithography costs [7]-[9]. Hence, to overcome these difficulties of nanoscale MOSFETs, new technologies such as Single-Electron Transistor (SET), Quantum-Dot Cellular Automata, and Carbon Nanotube Field Effect Transistor (CNTFET) have been studied in many literatures [8]. Among these technologies CNTFET seems to be the most feasible promising successor due to its remarkable features and its similarities with MOSFET technology[8],[10]. CNTFET technology benefit from ballistic operation and

one dimensional band structure, and low OFF-current and the same mobility for both n-type CNTFET and p-type CNTFET. This feature facilities the transistor sizing of complex circuits easier [11]. Therefore, CNTFET can be used for designing energy efficient integrated circuits. The diameter of the CNT relies on the chiral vector. The Chiral vector indicates the electronic characteristics and arrangement angle of carbon atoms along CNTs. It is determined by (n1, n2) integer pair. If $n_1 - n_2 = 3i\,(i \in Z)$, CNT is metallic, otherwise is semiconductor [12]. The diameter of nanotubes in nanometer is computed using the equation (1):

$$D_{CNT} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{1}$$

It worth to mention that the desired threshold voltage of the CNTFET based transistors could be adjusted based on the diameter of nanotubes which are located under the transistor gate (equation 2) [12].

$$V_t \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{\alpha E_\pi}{e D_{CNT}} \approx \frac{0.43}{D_{CNT}} \tag{2}$$

Where, $\alpha (\cong 0.249nm)$ is the CNT lattice constant, E_π is the energy of carbon $\pi - \pi$ band in the tight bonding model, e is the electron charge, and D_{CNT} is the diameter of nanotubes..

Compressor cells are generally employed in multi-operand adders to reduce the number of operands and in multipliers. The four-to-two compressor compresses five partial products bits into three. This compressor has four inputs called *X1; X2; X*3 and *X4* and two outputs, *SUM* and *CARRY* along with a *CARRY-IN (Cin*) and a *CARRY-OUT (Cout).* The input Cin is the output from the previous cascaded compressor. The Cout is the output to the compressor in the next stage.

In the literature many four-to-two compressor cells have been presented previously [13]-[15]. Figure 1 shows the structure of the four-to-two compressor cell proposed in [13]. The main idea of this design originated from truth table of the four-to-two compressor. This structure is composed of a single array of capacitors and CNTFET-based network. In this design CNTFET with different threshold voltage are used [11].

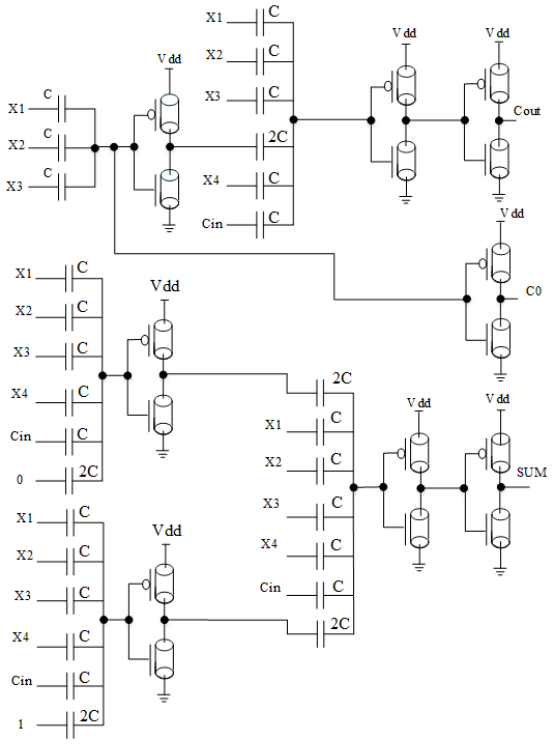

Figure 1. The Four-to-Two compressor structure in [10]

Figure 2, exhibits the structure of the four-to-two compressor cell discussed in [14]. It consists of seventy transistors. It has about three 2-way XOR critical path delay. This compressor is based on new description of logical equations that describe the corresponding functionality [12].

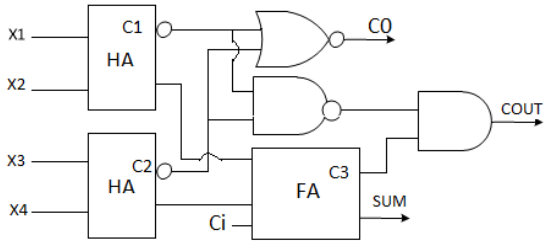

Figure 2. The Four-to-Two compressor structure in [14]

Figure 3 demonstrates the structure of four-to-two compressor cell proposed in [15]. It consists of seventy-two transistors. The critical path delay of this compressor equals to the delays of "one ‘NAND', two ‘2-way XORs’, one ‘2-way XNOR’" gates [13].

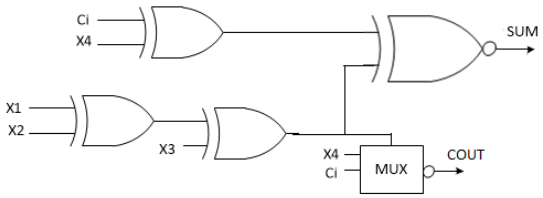

Figure 3. The Four-to-Two compressor structure in [15]

In this paper a new four-to-two compressor cell based on Majority Function, NOR, and NAND gates is presented. The main advantage of proposed design in comparison with previous cells is that the COUT1 (CARRY) output obtained using Majority function.

2. RESEARCH METHOD

In this section a new design for a high performance four-to-two compressor is presented. The proposed four-to-two compressor cell is based on the equations (3), (4), and (5). The Block diagram of the proposed design is shown in Figure 4.

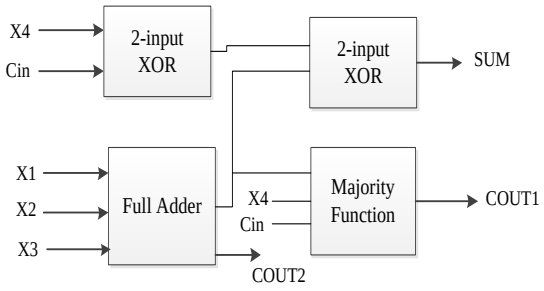

Figure 4. The block diagram of proposed four-to-two compressor

To obtain SUM output, one full adder and two 2-input XOR gates are employed. As mentioned the performance of the proposed four-to-two compressor cell depends on the method that uses the

implementation of the full adder, XOR, and Majority function blocks. To increase the efficiency of proposed cell, full adder which is designed in [16] has been used. To design this full adder, the unique properties of the CNTFET transistors are utilized. In order to produce the outputs of Majority-not, NAND, and NOR modules, three-input capacitors networks and inverters with different thresholds are used.

$$SUM = X1 \oplus X2 \oplus X3 \oplus X4 \oplus X5 \quad (3)$$

$$COUT1 = Majority[(X1 \oplus X2 \oplus X3), X4, Cin] \quad (4)$$

$$COUT2 = Majority(X1, X2, X3) \quad (5)$$

To produce the 2-input XOR function, 6 transistors in symmetric manner are used. Figure 5 displays the 2-inputs XOR gate that employs Cin and X4 signals as input signals to generate the SUM signal.

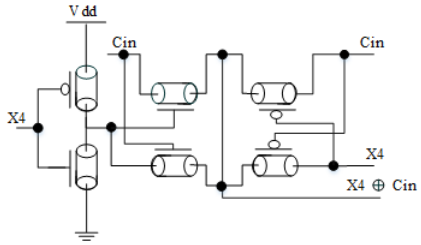

Figure 5. 1st proposed 2-inputs XOR gate

Figure 6 shows the 2-inputs XOR gate that hires S (equation 6) and Cin⊕X4 signals as input signals to generate the SUM signal.

$$S = X1 \oplus X2 \oplus X3 \quad (6)$$

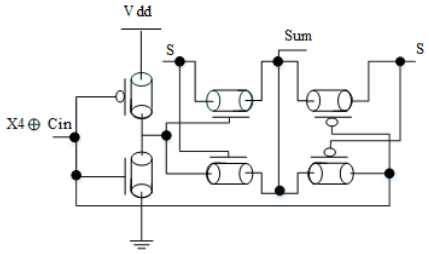

Figure 6. 2nd proposed 2-inputs XOR gate

The Cout2 output is based on Majority of X1, X2, and X3 inputs. This signal is employed as one of the elements required to produce the SUM signal. This method makes the proposed four-to-two structure more efficient.

In the proposed design, unlike the previous four-to-two compressor structures, the Cout1 output is obtained easily using one Majority function. The transistor level implementation of the proposed cell is shown in Figure 7. As it is shown the S node and one 3-inputs XOR function, are used for both SUM and Cout1 outputs. It makes the proposed design more effective.

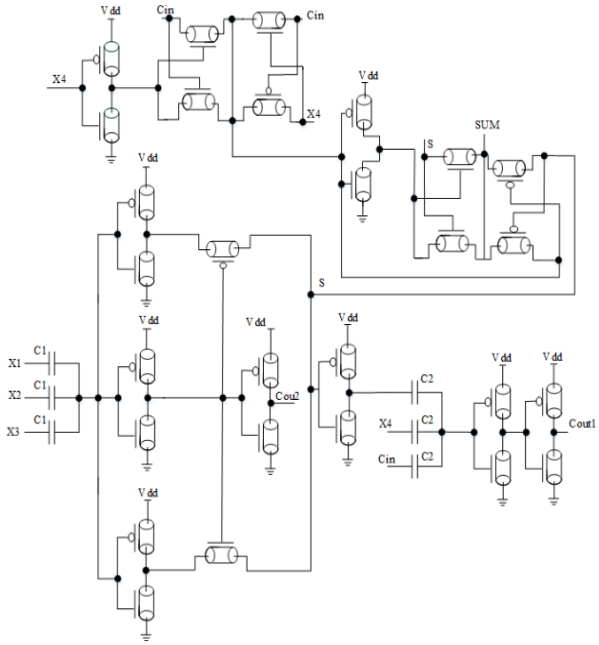

Figure 7. The schematic of the proposed four-to-two compressor

3. RESULTS AND ANALYSIS

To perform simulations, the Synopsys HSPICE tool has with the 32nm Compact SPICE model presented in [17], [18] has been used. This model is developed for MOSFET-like CNTFETs with SWCNTs as their channel considers non-ideal parameter such as Parasitic including CNT [19], Gate resistances, capacitances, Source/Drain, and Schottky Barrier Effects. Simulation has been done on previous four-to-two compressor cells [13]-[15] and the results are compared with the proposed design. The delay of output signals is measured from the time that input signals before the buffers reach to 50% of their voltage level to the moment that output signals reach to the same level. Then the maximum delay is reported as the delay of the circuit. The power consumption is the average power consumption measured during a long time [8], [19]. Finally the power-delay product (PDP) which compromises between delay and power consumption is reported as a figure of merit. Transistors are adjusted in a way that the minimum PDP could be obtained.

Table 1 shows the simulation results at 0.65V supply voltages and at 250MHz operating frequency with 2.1fF output load capacitance in room temperature. As it is shown the proposed four-to-two compressor structure has low delay, low power consumption, and the best PDP in comparison with other cells.

Table 1. The simulation results at 0.65V and at 250 MHz, 2.1fF

Design	Delay (E-10)	Power (E-7)	PDP (E-15J)
Design [13]	5.1121	7.1563	0.36583
Design [14]	55.908	5.7699	3.2259
Design [15]	51.327	5.2209	2.6797
Proposed Design	2.4910	4.8820	0.12161

Nowadays, VLSI circuits with the capability of working in high frequencies are required [19]. All designs are simulated at higher frequencies such as 100 MHz, 250MHz and 500MHz. Table 2 shows the cell performance versus frequency increments. It can be realized that the proposed structure has the best performance among all compared circuits at high frequency operation. All designs have also been simulated in a vast range of temperatures from 0^{oC} to 100^{oC} at 100MHz operating frequency and 2.1fF load capacitor to examine the immunity of the circuits to the temperature noise and variations.

The results are shown in Figure 8 The results exhibit that the proposed design has normal functionality in spite of temperature variations. The presented design also surpasses other designs in terms of performance.

Table 2. The simulation results in Different Operating Frequencies

Design	100MHz	250MHz	500MHz
Delay(E-10)			
Design [13]	5.1121	63.689	81.511
Design [14]	55.908	5.7699	3.2259
Design [15]	51.327	58.401	74.907
Proposed Design	2.4910	2.84473	3.6701
Average Power			
Design [13]	7.1563	7.2344	7.3907
Design [14]	5.7699	5.8332	5.9914
Design [15]	5.2209	5.2842	5.4424
Proposed Design	4.8820	4.9332	5.0612
PDP(E-15)			
Design [13]	0.36583	0.4210	0.55209
Design [14]	3.2258	3.7151	4.8836
Design [15]	2.6797	3.0860	4.0767
Proposed Design	0.1216	0.1403	0.1857

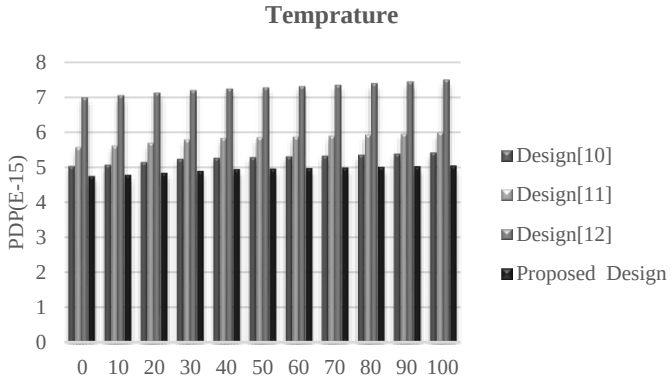

Figure 8. PDP versus supply Temperature Variations

The simulations have been carried out at 0.5V, 0.65V, 0.85V, 1.1V, and 1.4V power supplies at 100MHz operating frequency at room temperature can see in Figure 9.

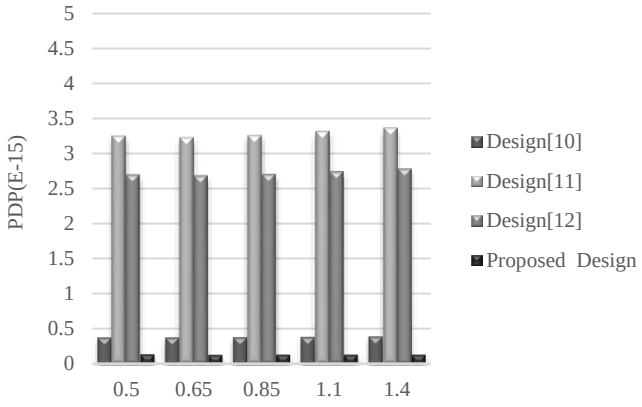

Figure 9. PDP versus supply voltage Variations

Different capacitors are employed as the output load to examine the driving power of the proposed design more precisely. The capacity of output load is considered as 1.5fF, 2.1 FF, 2.8fF, 3.6fF and 4.5fF at room temperature and 100MHz operating frequency. The simulation results are demonstrated at Figure 10 respectively.

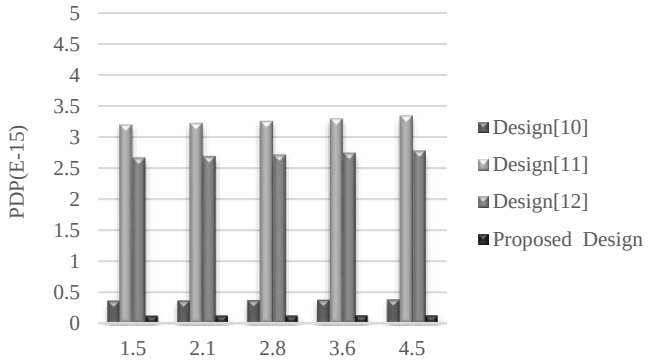

Figure 10. PDP versus Load Variations

4. CONCLUSION

Compressor cell is one of the most important circuits because of its effect on the multiplication process which is frequently used in the digital system. In this paper a novel four-to-two compressor cell was presented using Capacitor network and Majority function, NAND and NOR gates is presented. Employing Majority function reduced its delay significantly. The proposed cell includes twenty six transistors and six capacitors. The four-to-two compressor cells was simulated using Synopsys HSPICE tool with 32nm CNTFET Compact SPICE model. Simulation results confirmed the priority of the proposed cell compared to other state-of-the-art four-to-two compressor cells.

ACKNOWLEDGEMENT

This paper is supported by mentioned affiliations.

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BIOGRAPHIES OF AUTHORS

Mehdi Bagherizadeh received his B.Sc. degree from Shahid Bahonar University in computer hardware engineering. He is also received M.Sc. and Ph.D degree in computer architecture from Science and Research Branch, Islamic Azad University, Tehran, Iran. He is currently an Assistant Professor in Department of Computer Engineering, Islamic Azad University, Rafsanjan. Iran. He is working on VLSI and circuit design based on CNFET, Application Specific Instruction set Processor, and WSN, and VANET.
E-mail: m.bagherizadeh@srbiau.ac.ir

Mona Moradi received her B.S. and M.Sc. degrees in Hardware Engineering. She has Ph.D. degree in 2015 at Science and Research Branch of Islamic Azad University under supervision of Prof. Keivan Navi. Her research interests include VLSI, Digital Integrated Circuits, MVL, Arithmetic Circuits, CNTFET, nano electronic, hardware security and Cryptography. She is now assistant professor at Islamic Azad University in Roudehen Branch.
E-mail: mo.moradi@riau.ac.ir

Mostafa Torabi received his B.Sc degree in Computer Software Engineering from Meybod Branch, Islamic Azad university, Meybod, Iran. He is also received M.Sc degree from Najafabad Branch, Islamic Azad University, Najafabad, Iran in Computer Software Engineering. He is currently an assistant professor in Department of Computer Engeenering, Islamic Azad University, Rafsanjan, Iran. His reaserch interests are: WSN, VANET and Claud Computings.
E-mail: m.torabi@iaurafsanjan.ac.ir