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Phase Frequency Detector and Charge Pump for Low Jitter PLL Applications

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ABSTRACT

In this paper a new technique is presented to improve the jitter performance of conventional phase frequency detectors by completely removing the unnecessary one-shot pulse. This technique uses a variable pulse-height circuit to control the unnecessary one-shot pulse height. In addition, a novel charge-pump circuit with perfect current-matching characteristics is used to improve the output jitter performance of conventional charge pumps. This circuit is composed of a pair of symmetrical pump circuits to obtain a good current matching. As a result, the proposed charge-pump circuit has perfect current-matching characteristics, wide output range, no glitch output current, and no jump output voltage. In order to verify such operation, circuit simulation is performed using 0.18 μm CMOS process parameters.

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1. INTRODUCTION

Phase-locked loops (PLLs) are widely used for clock synchronization in microprocessors, digital signal processors, and wireless communication systems [1]. An increasing number of PLL applications for high-speed data transmission are demanding a lower jitter and a higher operating frequency to improve overall system performance.

One of the essential building blocks of PLL is the phase frequency detector (PFD). This monitors the phase and frequency difference between the reference frequency (Fref) and the divided voltage-controlled oscillator (VCO) output (Fback). Therefore, the PFD might generate an up signal (UP) if the Fref signal leads the Fback signal and a down signal (DOWN) if the Fref signal lags the Fback signal. However, an unnecessary one-shot pulse associated with the delay time of the reset path is generated at the UP and DOWN output, which in turn creates a current mismatch between the UP and DOWN current path of the charge pump. Thus, the spectral purity of the VCO output is degraded, and jitters are generated in the PLL. Various methods have already been developed to improve the jitter performance of conventional PFDs [2]-[7]. We propose a new architecture to minimize such jitter problem. In this architecture, a variable pulse-height circuit is added to the PFD output node to control the unnecessary one-shot pulse height due to the input signal.

The charge pump uses switches to control the voltage connection to the capacitor. As a result, the charge-pump tunes the control voltage of the VCO by charging or discharging the loop filter capacitor according to the pulse width of the UP or DOWN signal. In addition, the main problems of the conventional charge pumps are current mismatches, glitch output current, and jump output voltage. They also degrade the spectral purity of the VCO output and cause jitters in the PLL [8]-[15]. Accordingly, we propose a novel charge-pump circuit with almost perfect current-matching characteristics to minimize such problems.

The organization of this paper is as follows. The proposed circuit implementation is described in Section 2. Simulation results validating the proposed strategy are presented and discussed in Section 3, and Section 4 presents the conclusions.

2. PHASE-LOCKED LOOP DESIGN

2.1. PFD design

2.1.1. Standard PFD (s-PFD)

Figure 1 (a) shows the schematic of the s-PFD. It consists of six reset paths whose delay times generate an unnecessary one-shot pulse at the UP and DOWN output. Typically this reset delay time of the internal node affects the PFD speed.

2.1.2. Conventional Precharged PFD (cp-PFD)

A schematic of a cp-PFD circuit is shown in Figure 1 (b). The reset path of the cp-PFD is shorter than that of the s-PFD because the reset process of the cp-PFD is composed of a three-gate feedback path. This means that the cp-PFD can overcome the speed limitation of the s-PFD and reduces dead zones. Nonetheless, according to input signals Fref and Fback, two true single-phase clocked D flip-flops are immediately reset through the NOR gate when the input signals of the NOR gate are logic "low." Meanwhile, an unnecessary one-shot pulse is generated equivalent to the delay time at the UP and DOWN output due to the delay time of the reset path. The period of the reset pulse lasts from the rising edge of the latter input signal between the Fref and Fback to the falling edge of the reset pulse. Thus, the width and height of the unnecessary one-shot pulse are also similar to those of the reset pulse.

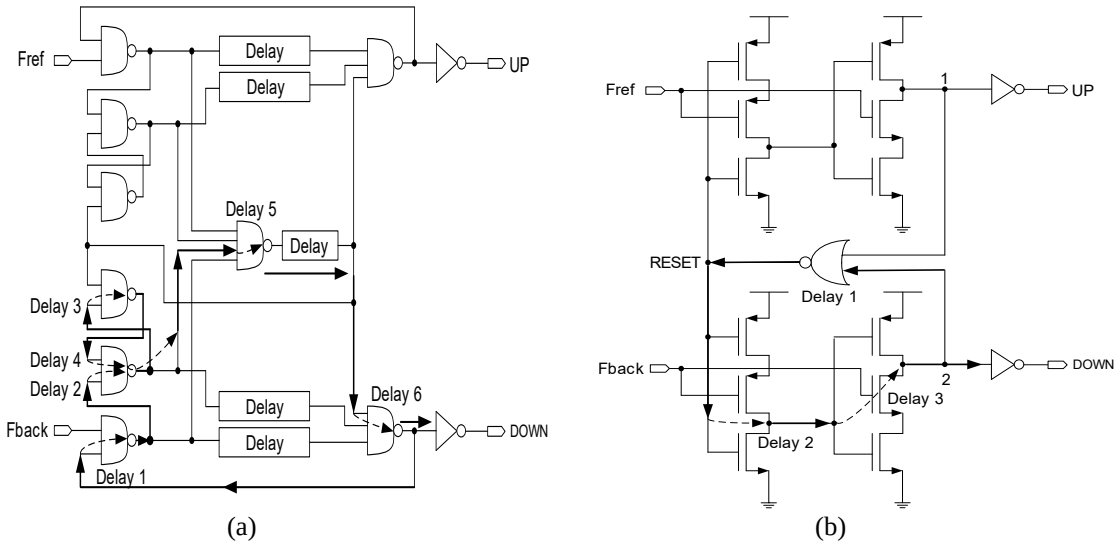


Figure 1. (a) Schematic of s-PFD. (b) Schematic of cp-PFD

2.1.3. Proposed PFD

To solve the cp-PFD problems, an improved PFD is proposed in Figure 2 (a). Pf feedback transistors are inserted to prevent any charge loss due to leakage currents at nodes A and B. In addition, a PFD-improved block, which consists of a modified inverter, a voltage-divider resistor (VDR), and a buffer, is configured in the existing UP and DOWN nodes. First, a modified inverter is inserted between nodes 1 and 3 and between nodes 2 and 4 to reduce the width and height of the unnecessary one-shot pulse. Figure 2 (a) shows that identical PMOS M2 and M2' transistors are connected in series. Thus, when the transistors are on, their resistance can be approximated as R_{on1}. This resistance and VDR make up a voltage divider for adjusting the level of a signal. Such divider can increase the rise time and make the unnecessary one-shot pulse whose width is approximately two times shorter than that of the reset pulse. In Figure 2 (b), this one-shot pulse does not arrive at the existing peak point because of the effects of the following phase buffer, and it starts to decrease from the 10.3-ns time point along with the reset pulse that has already reached the peak point. As a result, the width and height of the unnecessary one-shot pulse are reduced to less than those of the reset pulse.

Second, VDR1 and VDR2 connected at nodes 3 and 4 are operated by input signals Fref and Fback, respectively. Each VDR consists of four identical NMOS transistors connected in series. When a VDR is on, its resistance can be expressed as R_{on2}. Using the voltage division between the modified inverter and VDR, the voltages of nodes 3 and 4 is approximated as

$$V_{3,4} = \frac{R_{on2}\, V_{DD}}{R_{on1}+R_{on2}}. \quad (1)$$

These voltages also reduce the width and height of the unnecessary one-shot pulse. Thus, the height of the unnecessary one-shot pulse can be reduced to a point below the maximum low input voltage that is interpreted by the first inverter of the following phase buffer. As a result, the unnecessary one-shot pulse has no effect on the following charge pump because of the buffer action. Further, this technique is only applied to unnecessary one-shot pulses and does not have any effect on the output data signals. When the "high" generated output data are equivalent to the difference between the two rising edges of the input signals from nodes 3 and 4, the voltage-divider theorem is also applied. The height of the output data is reduced to a point above the minimum high input voltage that is interpreted by the first inverter of the following phase buffer. In addition, the output data are completely restored by the buffer.

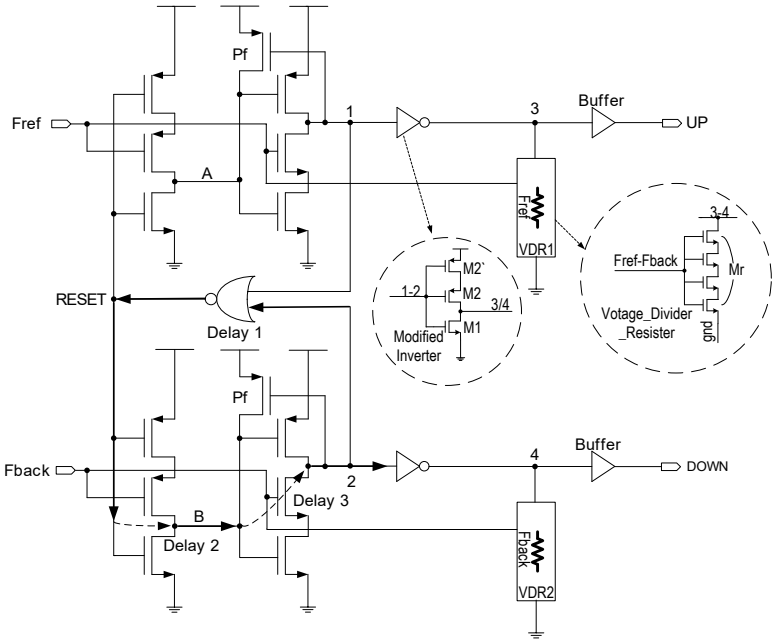


Figure 2(a). Schematic of the proposed PFD

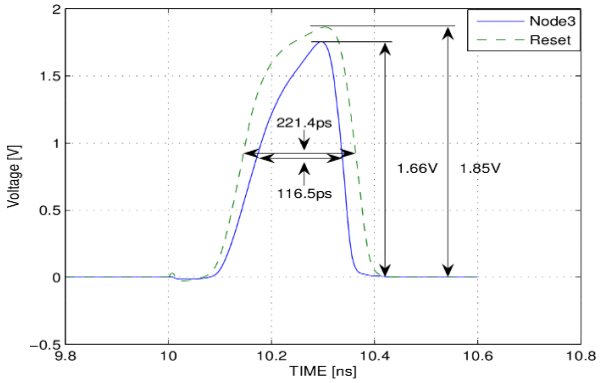


Figure 2(b). Simulation results of the reset pulse and unnecessary one-shot pulse for the proposed PFD

2.2. Charage pump design

2.2.1. Standard Charge Pump

Figure 3 (a) shows the basic structure of a conventional charge pump that has a PMOS and an NMOS transistor at the top and bottom, respectively. However, the use of such pumping MOS as a current source tends to produce glitches whenever the pumping MOS is turned on or off. These glitches are due to the charge injection of transistor channel charge and the clock feedthrough between the gate and the drain. This process produces a higher current than intended when the pumping MOS is initially opened. Furthermore, in most charge pumps, the circuits are designed to respond to the UP and DOWN output of the PFD, which in turn are directly connected to the output structure of the PMOS and NMOS switches. Thus, these switches cause the mismatches between the current sourcing and current sinking, and then generate a discordant switching time. The design of the charge pump should enable the sourcing and sinking currents to have the same amount of current for the same length of UP and DOWN from the PFD. The phase offset caused by a current mismatch eventually increases the output timing jitter.

2.2.2. Proposed Charge Pump

To solve the glitch problems, a novel charge-pump circuit with nearly perfect current-matching characteristics, no glitch output current, and no jump output voltage is proposed in Figure 3 (b), which includes a symmetrical pair of pump-up and pump-down circuits. This charge pump can have three types of input status depending on UP or DOWN of the PFD. First, when UP is "high" and DOWN is "low," M12 turns off, which causes M8 and M9 to stop operating. When M1 turns on, Amplifier_A turns into a cascode amplifier that enables M3 to operate as a current source, and its current flows through the cascode current mirror to the output node. Such cascoding minimizes the glitch and high output resistance provides good current sourcing. The voltage gain of the UP cascode amplifier can be approximated as

$$|A_{VU}| = \frac{g_{m1}\,(g_{m2}+g_{mb2})\,r_{o3}}{1+g_{m2}+g_{mb2}}. \quad (2)$$

Second, when UP and DOWN are both "low," M1 and M12 turn off, which causes M5 and M8 to stop operating. As a result, the control voltage Vcontrol node maintains a constant voltage and enters a high-impedance status. Finally, when UP is "low" and DOWN is "high," M1 turns off, which causes M4 and M5 to stop operating. When M12 turns on, Amplifier_B turns into a cascode amplifier that allows M10 to function as a current source. and its current flows through the cascode current mirror to the output node. Such cascoding also minimizes the glitch and high output resistance provides good current sinking. The voltage gain of the DOWN cascode amplifier can be approximated as

$$|A_{VD}| = \frac{g_{m12}\,(g_{m11}+g_{mb11})\,r_{o10}}{1+g_{m11}+g_{mb11}}. \quad (3)$$

M2 and M11 adjust control voltage Vcontrol to the desired level using Vbias1 and Vbias2, whereas M13 and M14 control the timing of the UP input to conform to that of the DOWN input.

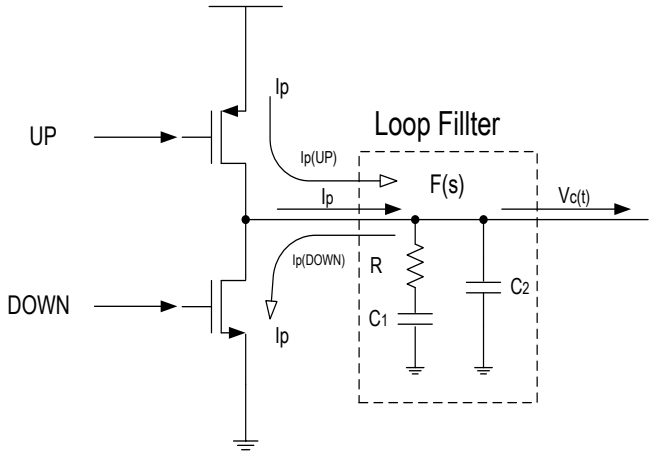


Figure 3(a). Structure of the conventional charge pump

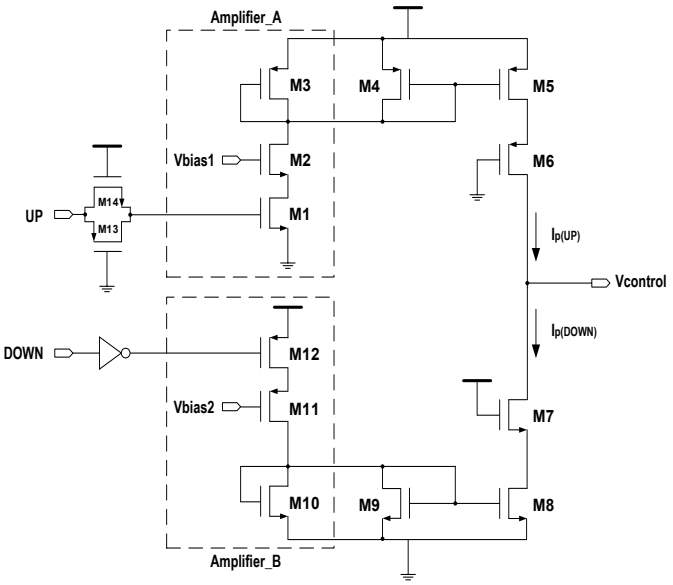


Figure 3(b). Schematic of the proposed charge pump

2.3. Loop filter, VCO, and frequency divider

The input voltage of the VCO is controlled in the time domain according to the amount of the sourcing or sinking current of the charge pump and the values of R and C of the loop filter shown in Figure 4 (a).

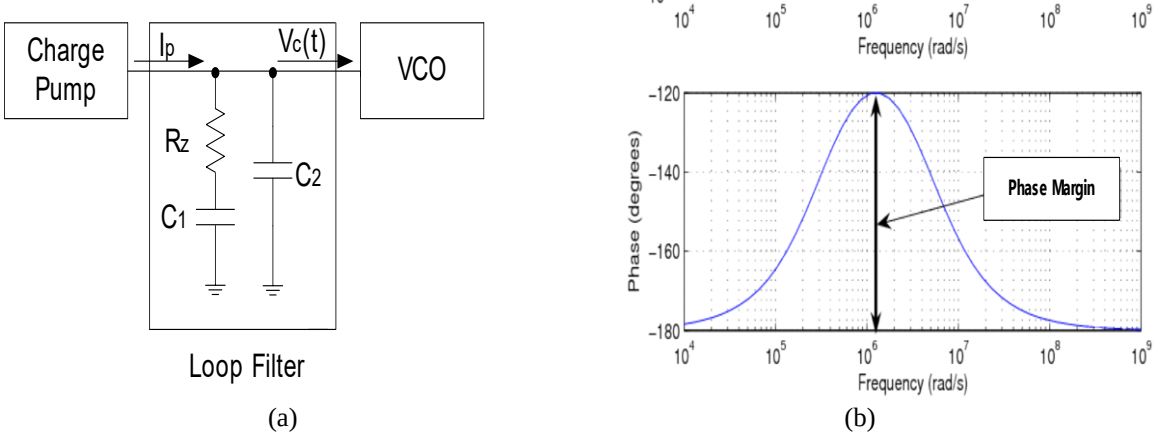


Figure 4. (a) The second-order loop filter. (b) The cross-over frequency and phase margin

Using the cross-over frequency ω_c, the element values R_z, C_1, and C_2 of the loop filter can be expressed as

$$R_z = \frac{N}{I_p K_{vco}} \omega_c,\ C_1 = \frac{1}{\omega_z R_z},\ C_2 = \frac{1}{\omega_p R_z} \quad (4)$$

where N is the value of frequency divider, I_p is the current gain of charge pump, K_{vco} is the gain of the VCO, ω_z is the zero frequency, and ω_p is the pole frequency. An integrated-circuit VCO is implemented as the ring oscillator shown in Figure 5 (a). Typically the VCO outputs a signal with a frequency proportional to the control voltage. Figure 5 (b) shows a delay cell used in the oscillator.

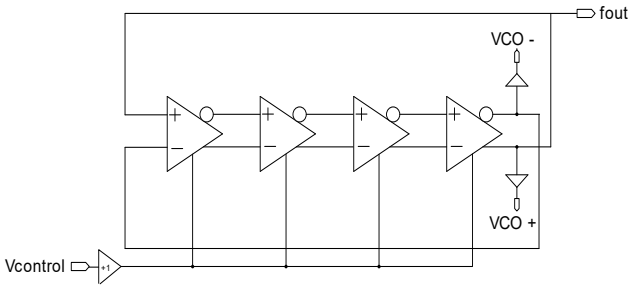


Figure 5(a). VCO structure using the dual-output ring oscillator with differential delay cells

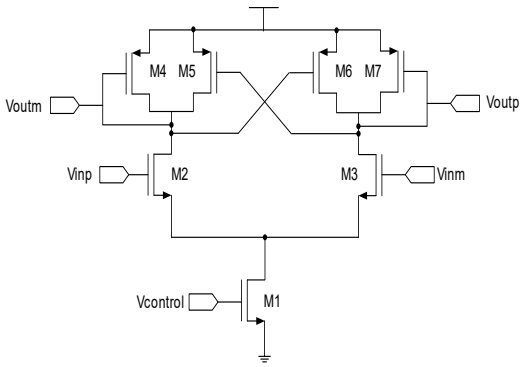


Figure 5(b). Schematic of a differential delay cell

The frequency divider consists of a synchronous 4/5 frequency divider that requires high frequency operation and an asynchronous 16/32 frequency divider that operates at low frequency. It is operated according to the value of Mode and SW, and is selected as ÷ N or ÷ N + 1 according to the selected value of Mode. According to the selection signal of SW, the value of ÷ N to N is adjusted to 64 or 128.

Table 1. Dividing ratio according to the value of SW and Mode

SW	Mode	Fout
0	0	VCO/128
0	1	VCO/129
1	0	VCO/64
1	1	VCO/65

Figure 7 (a) shows a true single phase clipping (TSPC) D flip-flop structure used in the asynchronous 16/32 frequency divider operating at low frequency. Figure 7 (b) shows a complementary clocking D (CCD) flip-flop structure used in the frequency divider. The M4 and M8 are added to prevent the current driving capability from decreases when node A and node B are conducting at high speed in TSPC D flip flop structure. It is applied to a synchronous 4/5 frequency divider which requires stable and high-speed operation at high frequency.

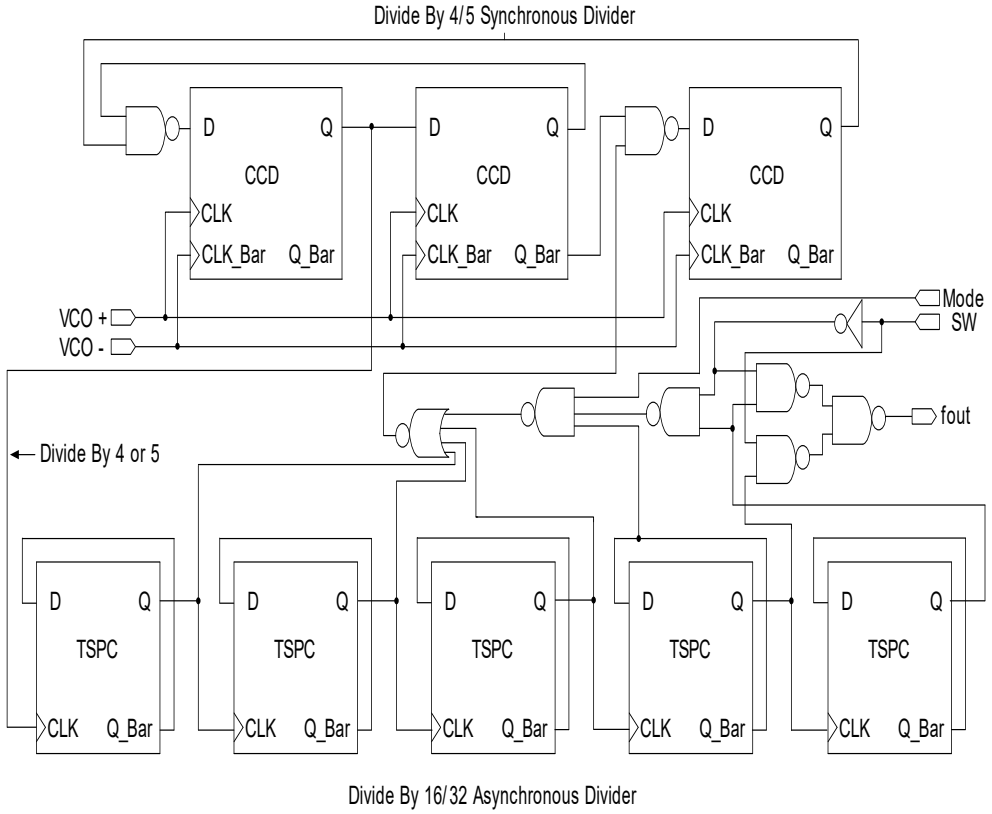
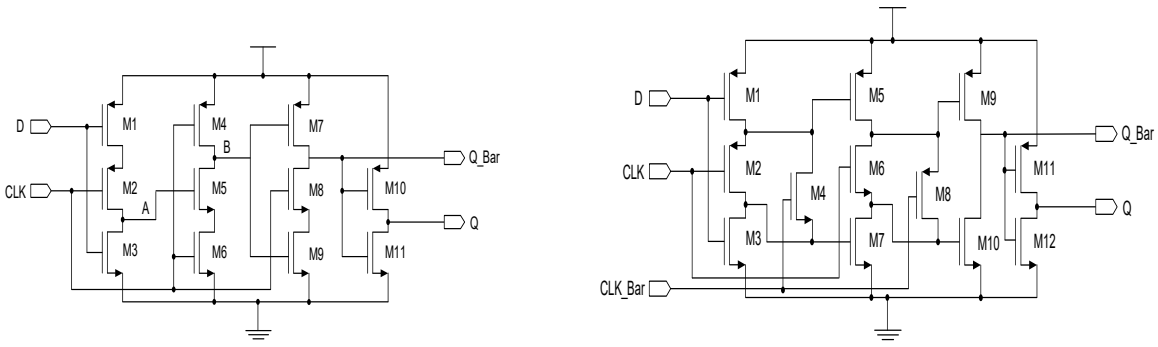


Figure 6. Structure of divide-by-64/65/128/129 dual-modulus prescaler



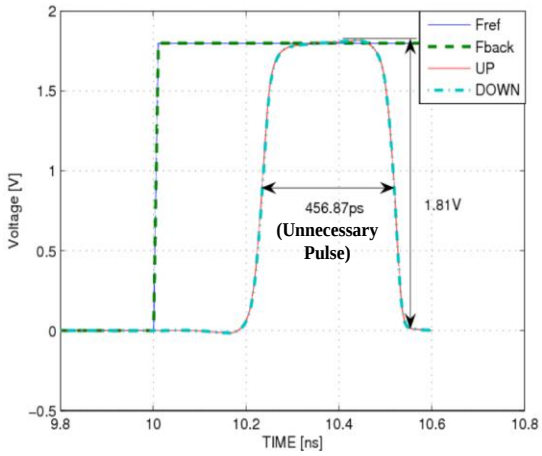
(a) (b)

Figure 7**.** (a) Schematic of TSPC D flip-flop. (b) Schematic of complementary clocking D flip-flop

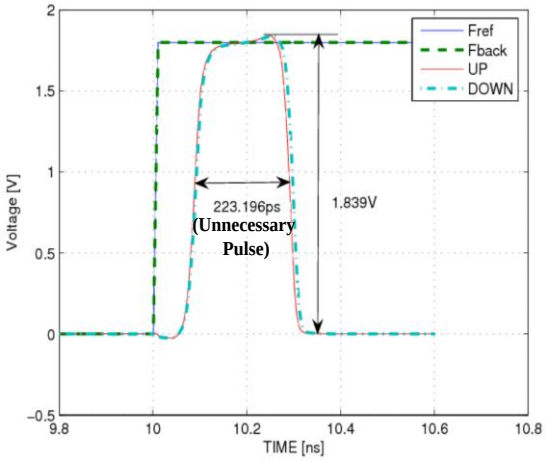
3. SIMULATION RESULTS

3.1. Proposed PFD simulation results

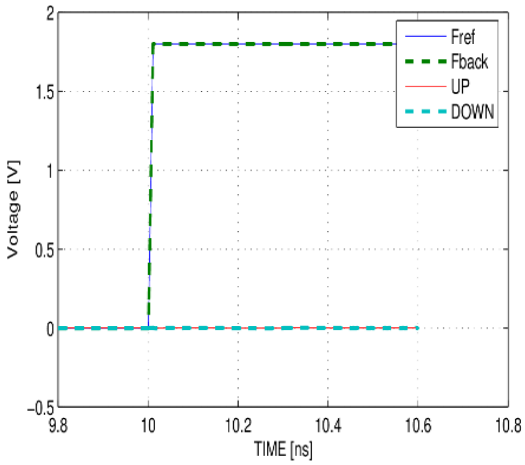
Figure 8 (a) shows the simulation results of the s-PFD. When the input signals were in phase, the width of the unnecessary one-shot pulse was 456.87 ps at 0.9 V, and the maximum height was 1.81 V. Figure 8 (b) shows the simulation results of the cp-PFD. When the input signals were in phase, the width of the unnecessary one-shot pulse was 223.19 ps at 0.9 V, and the maximum height was 1.83 V. Meanwhile, Figure 8 (c) shows the simulation results of the proposed PFD. When the input signals were in phase, the width of the unnecessary one-shot pulse was 13.5 ps at 0.98 µV, and the maximum height was 1.96 µV, which would prevent an UP and DOWN current mismatch in the charge-pump circuit. Moreover, the power consumed at 100 MHz was 77.36 µW with a 1.8-V supply voltage. Figure 9 (a-e) shows the full simulation results of the proposed PFD.



(a) s-PFD



(b) cp-PFD



(c) Proposed PFD

Figure 8. Simulation results of the output signals when the input signals are in phase

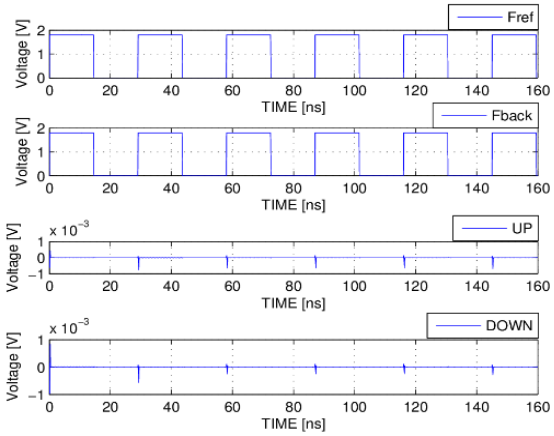


Figure 9(a). Fref and Fback have the same phase and frequency

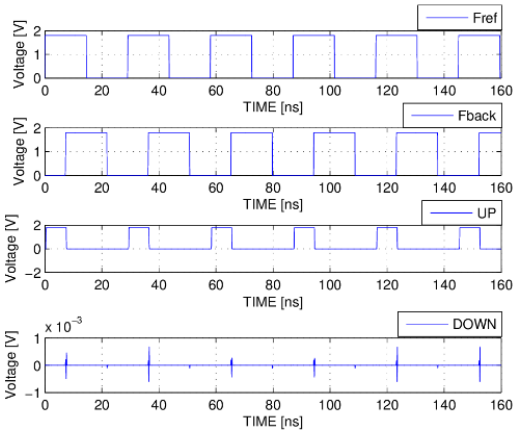


Figure 9(b). When Fref is a phase faster than Fback for the same frequency

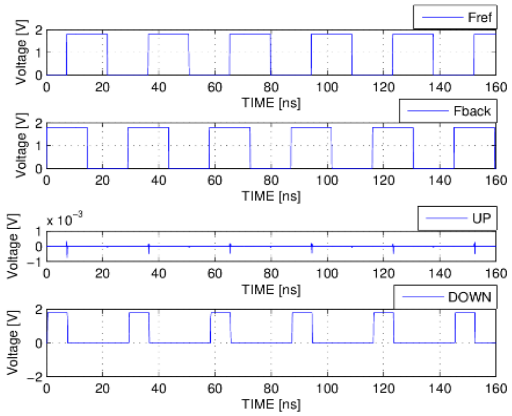


Figure 9(c). When Fback is a phase faster than Fref for the same frequency

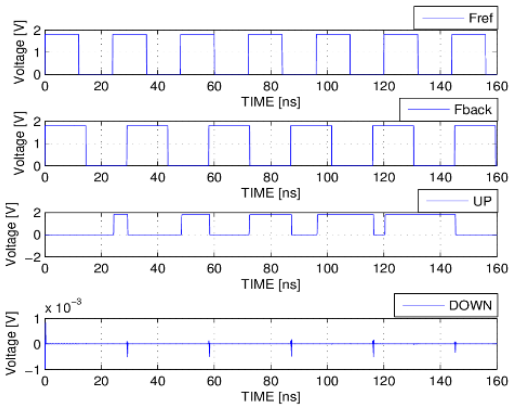


Figure 9(d). Fback frequency is higher than Fref frequency

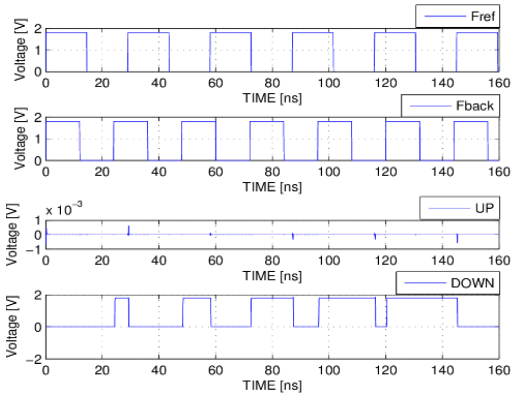


Figure 9(e). Fref frequency is higher than Fback frequency

3.2. Proposed charge pump simulation results

Figure 10 shows the simulation results of the standard charge pump. Figure 11 shows the waveforms of source current Ip (up) and sinking current Ip (down) of the proposed charge pump when a 100-MHz square wave is used, along with the control voltage Vcontrol up/down output waveform generated by Ip (up) and Ip (down). As shown, source current Ip (up) is +100 µA, whereas sinking current Ip (down) is -100 µA. Figure 12 shows the resulting waveform of current Ip and control voltage Vcontrol of the charge pump when the up and down input signals were both "low." In this case, when Vcontrol was fixed at 0.9 V, current Ip was 0 A, causing it to stop operating. Figure 13 shows that the output waveforms of full Vcontrol (up) and full Vcontrol (down) of the control voltage Vcontrol are perfectly symmetrical at 0.9 V. Furthermore, it can be seen that there are no glitch in the current waveform and no jump phenomenon in the voltage waveform.

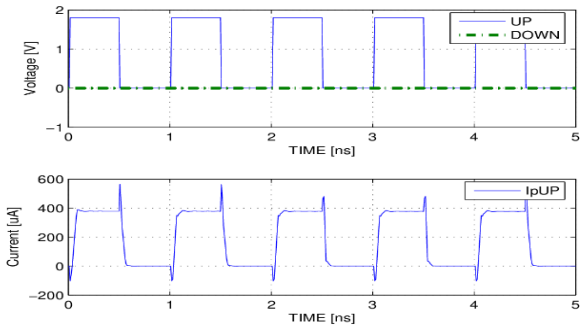
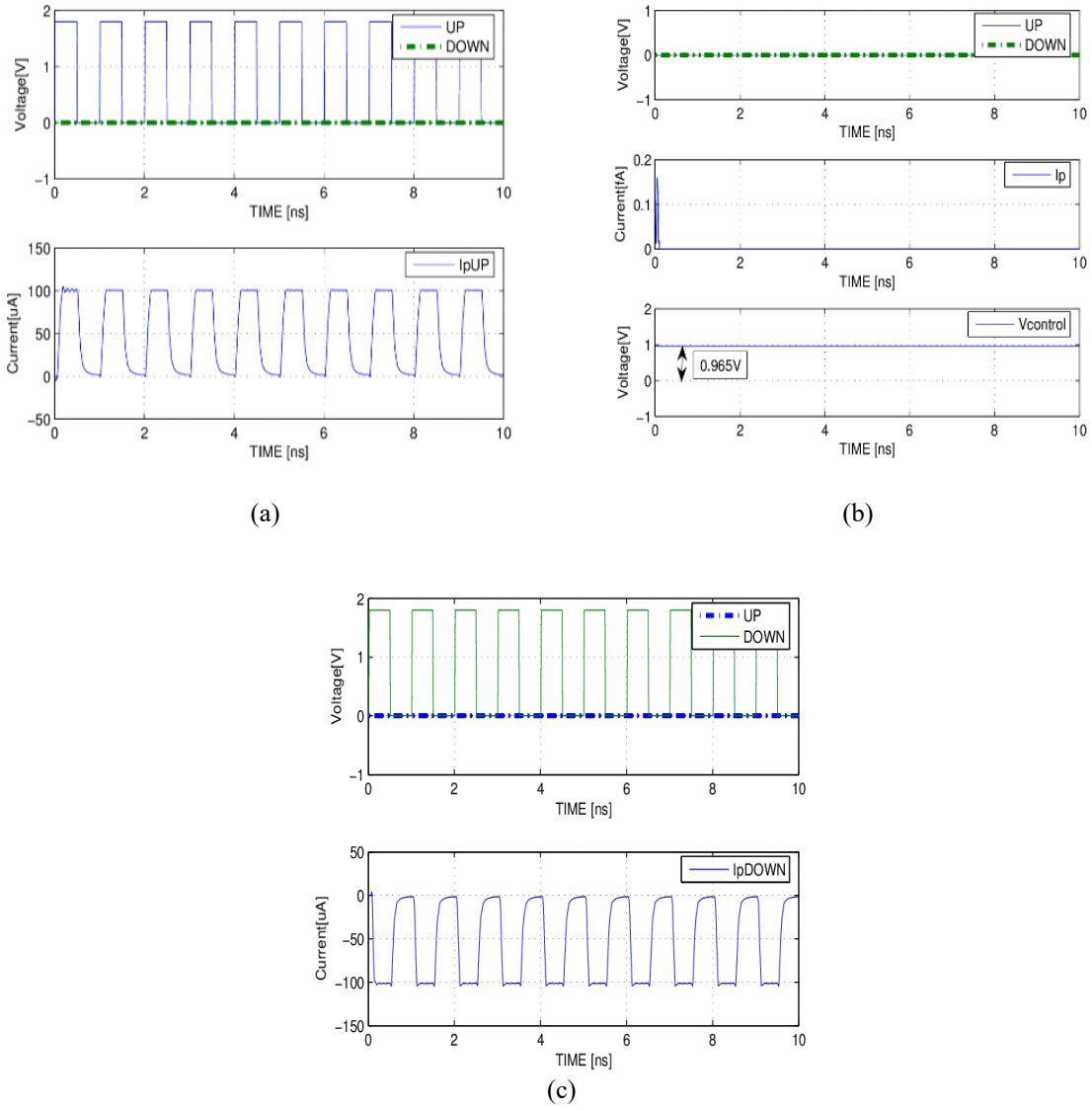


Figure 10. Output current Ip (up) waveform of the standard charge pump



(a) (b)

(c)

Figure 11. Simulation results of the proposed charge pump. (a) Source current output waveform. (b) Ip and Vcontrol output waveform when UP and DOWN are zero. (c) Sinking current output waveform

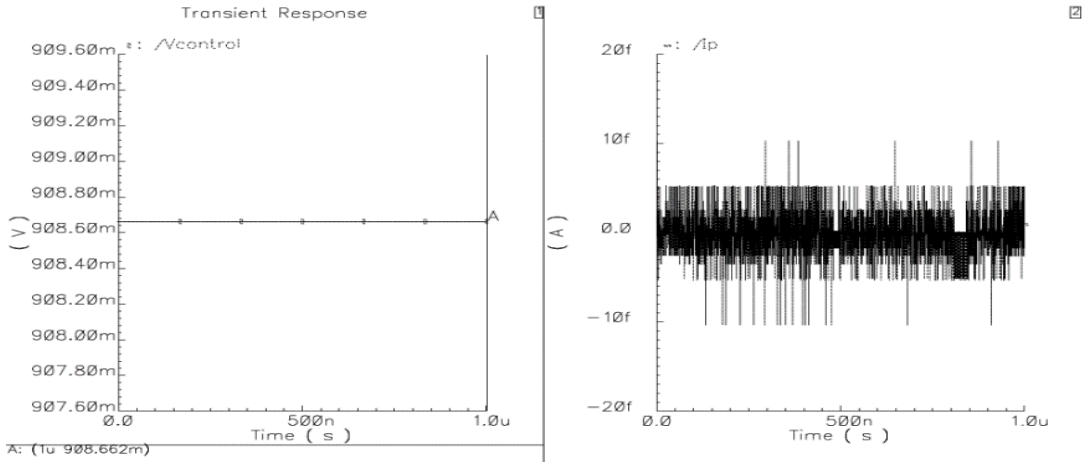


Figure 12. Output voltage and current waveforms when the up and down input signals are "low."

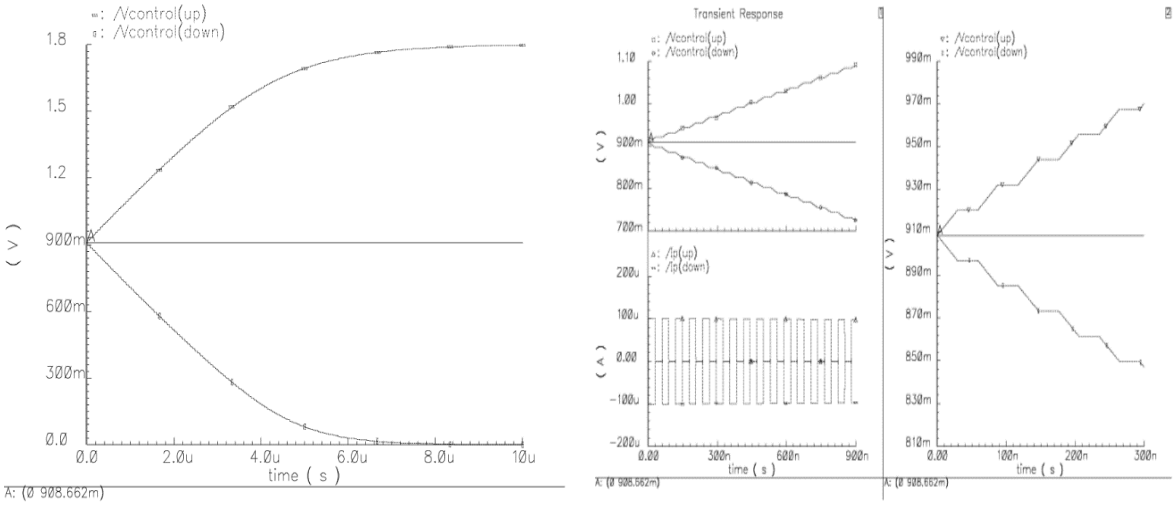


Figure 13**.** Simulation results of the proposed charge pump: full pumping up/down output voltage waveform

3.3. Designed PLL Simulation Results

Figure 14 shows the simulation results of the designed PLL with a 2.1779 GHz output. The PLL has a lock time of 20 µs. From these results, it can be seen that this PLL circuit exactly and stably works. Table 2 shows the performance comparison of the designed PLL with the published results [16].

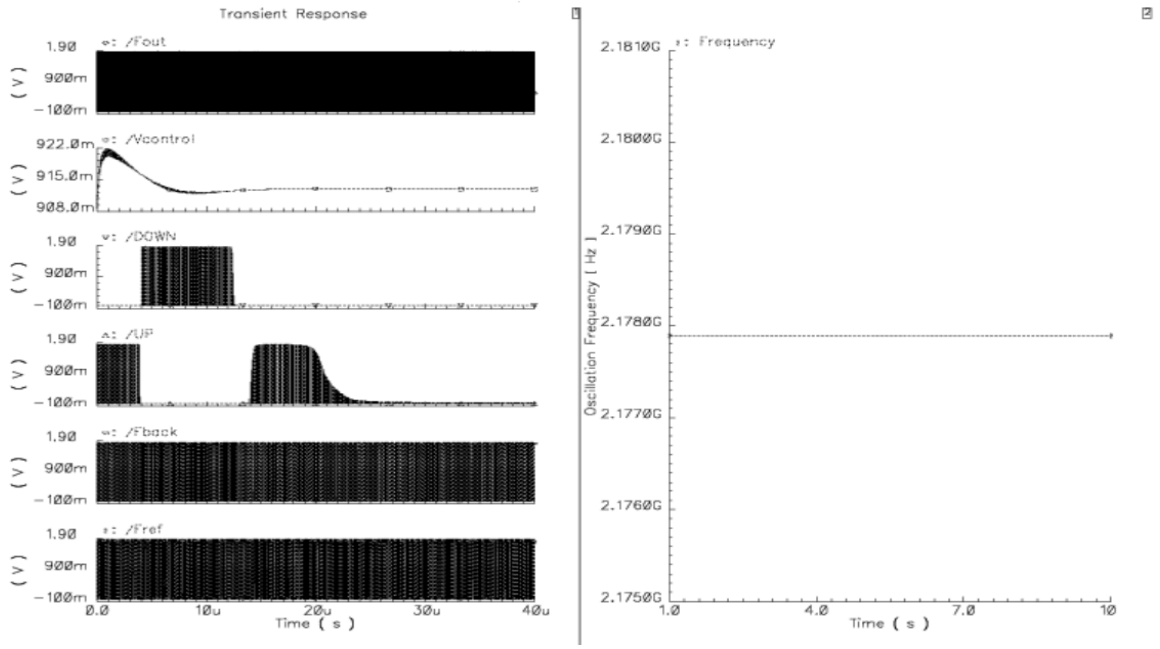


Figure 14. Full simulation results of the designed PLL with a 2.1779 GHz output using the proposed PFD and proposed charge pump

Table 2. Performance comparison of the designed PLL

Performance	[16]	This work
Power supply	1.8 V	1.8 V
Power dissipation	29.6 mW at 2.409 GHz	29.952 mW at 2.1779 GHz
Output frequencies	2.368 ~ 2.496 GHz	333.8 MHz ~ 2.7 GHz
Phase noise	– 113.0 dBc/Hz @ 1 MHz	– 90.39 dBc/Hz @ 1 MHz
Settling time	~ 20 µs (Hybrid PLL) ~ 80 µs (Normal Integer-N PLL)	~ 20 µs

4. CONCLUSION

A new technique has been presented to improve the output jitter performance of conventional PFDs. The proposed circuitry added a variable pulse-height element to the PFD output node, and the simulation results demonstrated that this technique reduces the width and height of the unnecessary one-shot pulse compared with the s-PFD and cp-PFD. In addition, a novel charge pump with good current-matching characteristics has been used to improve the output jitter performance of a conventional charge pump. This charge pump consisted of a pair of symmetrical pump-up and pump-down circuits. The simulation results demonstrated that the charge pump has nearly perfect current-matching characteristics, wide output range, more stable step output voltage, and no glitch current. Such circuits can be used in low-power and low-jitter PLL applications.

REFERENCES

[1] P. N. Metange and K. B. Khanchandani, "Analysis and design of high performance phase frequency detector, charge pump and loop filter circuits for phase locked loop in wireless applications," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 4, pp. 397-405, 2016.

[2] J. Strzelecki and S. Ren, "Near-zero dead zone phase frequency detector with wide input frequency difference," *Electronics Letters*, vol. 51, pp. 1059-1061, 2015.

[3] S. L. Kai, *et al.*, "Fast-lock dual charge pump analog DLL using improved phase frequency detector," *2007 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, pp. 1-5, 2007.

[4] E. R. Suraparaju, *et al.*, "Simple high-resolution CMOS phase frequency detector," *Electronics Letters*, vol. 51, pp. 1647-1649, 2015.

[5] C. Hsu, *et al.*, "A sub-sampling-assisted phase-frequency detector for low-noise PLLs with robust qperation under supply interference," *IEEE Transactions on Circuits and Systems*, vol. 62, pp. 90-99, 2015.

[6] K. Minhad, *et al.*, "Investigating phase detectors: Advances in mature and emerging phase-frequency and time-to-digital detectors in phase-locked looped systems," *IEEE Microwave Magazine*, vol. 56, pp. 56-78, 2015.

[7] U. Nanda and D. P. Acharya, "An efficient technique for low power fast locking PLL operating in minimized dead zone condition," *2017 Devices for Integrated Circuit (DevIC)*, pp. 396-400, 2017.

[8] W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 545-548, 1999.

[9] Z. Tao, *et al.*, "A CMOS charge pump with a novel structure in PLL," *Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology*, vol. 2, pp. 1555-1558, 2004.

[10] K. Arshak, *et al.*, "Improved charge pump for reduced clock feed through and charge sharing suppression," *Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems*, vol. 1, pp. 192-194, 2004.

[11] S. Cheng, *et al.*, "Design and analysis of an ultrahigh-speed glitch-free fully differential charge pump with minimum output current variation and accurate matching," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol/issue: 53(9), pp. 843-847, 2006.

[12] N. Joram, *et al.*, "High swing PLL charge pump with current mismatch reduction," *Electronics Letters*, vol. 50, pp. 661-663, 2014.

[13] L. Xia, *et al.*, "Built-in self-test structure for fault detection of charge-pump phase-locked loop," *IET Circuits, Devices & Systems*, vol. 10, pp. 317-321, 2016.

[14] H. Liu, *et al.*, "A calibrated charge pump for mismatch reduction in PLL," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 10, pp. 2304-2308, 2012.

[15] B. Na, *et al.*, "An improved charge pump with suppressed charge sharing effect," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 12, pp. 1245-1249, 2014.

[16] K, Woo, *et al.*, "Fast-lock hybrid PLL combining fractional- N and integer-N modes of differing bandwidths," *IEEE Journal of Solid-State Circuits*, vol/issue: 43(2), pp. 379-389, 2008.

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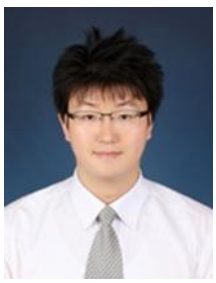

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