International Journal of Electrical and Computer Engineering (IJECE)
Vol. 8, No. 6, December 2018, pp. 4922~4931
ISSN: 2088-8708, DOI: 10.11591/ijece.v8i6.pp4922-4931

Analysis of CMOS Comparator in 90nm Technology with Different Power Reduction Techniques

Anil Khatak[1], Manoj Kumar[2], Sanjeev Dhull[3]
[1]Department of Biomedical Engineering, GJUS&T, India
[2]USICT, Guru Gobind Singh Indraprastha University, India
[3]Department of ECE, GJUS&T, HISAR, India

Article Info

Article history:

Received Jan 26, 2018
Revised Jun 17, 2018
Accepted Jul 22, 2018

Keyword:

Cascode
Cascode voltage switch logic (CVSL)
Current drawn (CD)
Power consumption (PC)
Pseudo
Regenerative
Ultra deep submicron (UDSM)

ABSTRACT

To reduce power consumption of regenerative comparator three different techniques are incorporated in this work. These techniques provide a way to achieve low power consumption through their mechanism that alters the operation of the circuit. These techniques are pseudo NMOS, CVSL (cascode voltage switch logic)/DCVS (differential cascode voltage switch) & power gating. Initially regenerative comparator is simulated at 90 nm CMOS technology with 0.7 V supply voltage. Results shows total power consumption of 15.02 µW with considerably large leakage current of 52.03 nA. Further, with pseudo NMOS technique total power consumption increases to 126.53 µW while CVSL shows total power consumption of 18.94 µW with leakage current of 1270.13 nA. More then 90% reduction is attained in total power consumption and leakage current by employing the power gating technique. Moreover, the variations in the power consumption with temperature is also recorded for all three reported techniques where power gating again show optimum variations with least power consumption. Four more conventional comparator circuits are also simulated in 90nm CMOS technology for comparison. Comparison shows better results for regenerative comparator with power gating technique. Simulations are executed by employing SPICE based on 90 nm CMOS technology.

Corresponding Author:

Anil Khatak,
Department of BME,
GJUS&T, HISAR,
Haryana, India.
Email: khatak10anil@gmail.com

1. INTRODUCTION

Comparators are backbone of many imperative ADC's & DAC's circuits [1]-[3]. Converter circuits are mainly studied with parameters i.e. data conversion speed, precision & power consumption [4]. Comaprators are the most essential component of ADC's as its precision significantly defines the working genre of these circuits [5]. As to attain these high-performance parameters new techniques are evolving which led to more complex and heavy architectures. It is found that energy-controlled applications such as portable cellphone devices, devices in health field, wireless networks, etc., require effective power managing analog-to-digital converters (ADCs) for a longer working extent [6], [7]. High speed comparators consume high power with greater chip area which led to degraded reliability with increased cost of cooling & packaging [8]. Hence, designing a high-speed comparator having small power consumption becomes difficult with least power supply.

As in the UDSM CMOS technology device size & supply voltage is dwindling so it is strenuous to design a high-speed comparator circuit for low voltages levels [9]-[11]. Regenerative comparator is very high speed stable comparator with large power consumption which restrict its applicability in nano electronics

domain [12], [13]. So, in order to counter this regenerative comparator is designed by incorporating different power reduction techniques such that it can comply with the device designer's requisites.

Three different power reduction techniques are employed on regenerative comparator [13] in order to drop its power consumption level so that it can be employed for designing high performance circuits with marginal power consumption. Initially regenerative comparator is design with pseudo NMOS technology with load circuit used as grounded PMOS transistor [14]. After that CVSL (cascode voltage switch logic)/DCVS (differential cascode voltage switch) technology is used on regenerative comparator. CVSL technique certainly improves parameters like circuit delay, power dissipation. One more point which makes this technique more applicable is that the digital circuits can be easily structured on the basis of tabular methods and Karnaugh maps (K-maps) [15]. Third power reduction technique is power gating that substantially reduces the power consumption of regenerative comparator. Power gating technique provides a mechanism through gating device that save static leakage power [16]. Nano scale circuits are very subtle to temperature variations so temperature variations are also noted for these comparators [17].

The further arrangement of article is as follows. Segment 2 provides a hasty overview of the circuit description along with different power reduction techniques. Section 3 provides details about the simulations, analysis of power dissipation and temperature variation for different power reduction techniques following comparison with conventional comparators in segment 4 with conclusion & references in the end.

2. DIFFERENT POWER REDUCTION TECHNIQUES

2.1. Regenerative Comparator in CMOS Technology

Figure 1 depicts the architecture for regenerative comparator in CMOS technology. The input is a differential pair amplifier which cosists mos devices. These devices are kept in feeble inversion state that amplifies the input difference signal. Positive feedbeck & regeneration are employed in the second stage & they became active when reset point is initiated with low signal and thus difference signal is transformed to VDD & VSS accordingly as final digital output [13]. This comparator architecture easily incorporates large signals due to high input common-mode range. An ON & OFF chip current source utilized in this schematic provides additional functionalities with which current can be modified for various sampling frequencies. Inputs are given through transistor T1, T2 and lower rail of MOS transistors are used for biasing purpose. Two NOR gates are used at end of the schematic which are latched together to provide regenerative feedback at the output that enhances the speed of this comparator.

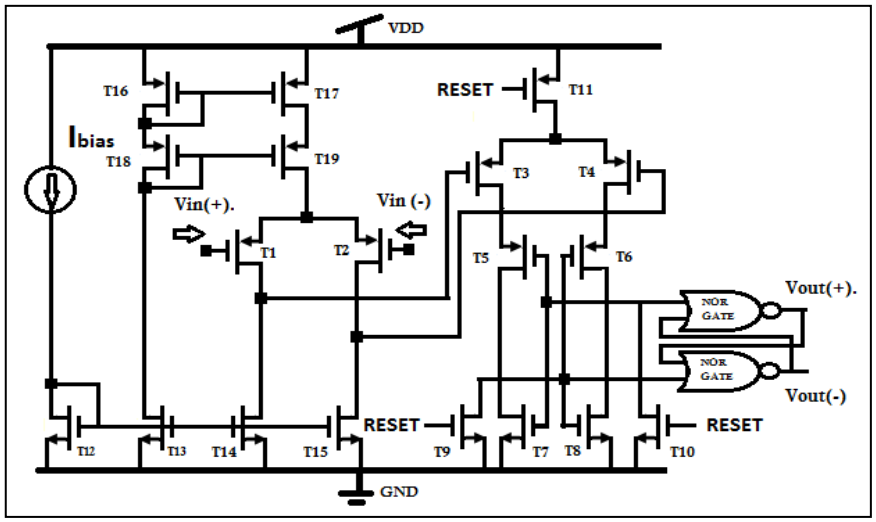


Figure 1. Regenerative Comparator in CMOS Technology

2.2. Regenerative Comparator in PSUEDO NMOS Technology

Figure 2 shows the structure of regenerative comparator employing pseudo NMOS technology [14], [18]. This technique engages a grounded PMOS as load for NMOS steering circuit.

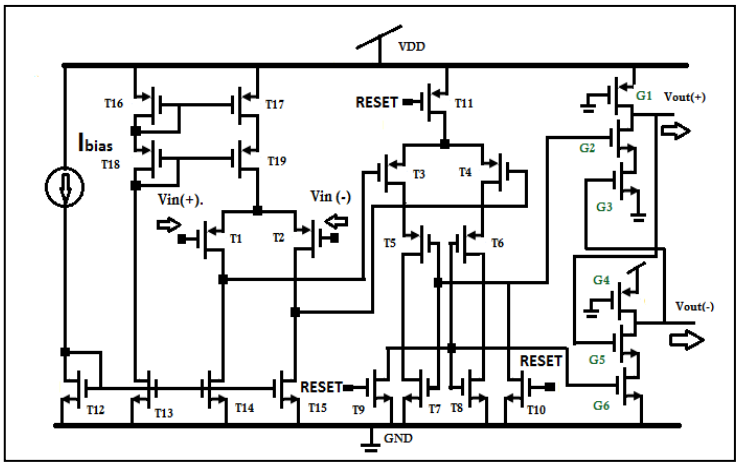


Figure 2. Regenerative comparator in pseudo NMOS technology

This circuit use overall 25 MOSFET. The input signal is feed through T1 & T2 MOSFET's which are arranged in fully differential pair. Second stage is used for amplification then two NOR gates to provide regenerative feedback in the end. G1, G2, G3, G4, G5 & G6 MOSFET'S are structured in pseudo NMOS technology which forms the two NOR gates at end of circuit. Inverted and non-inverted output is then taken from Vout (-) & Vout (+).

2.3. Regenerative Comparator in CVSL Technology

Figure 3 depicts the architecture for regenerative comparator designed in CVSL technology [15] [19]. CVSL technology is nothing but cascade voltage switch logic or differential voltage switch logic [20]. MOS transistors G1 to G12 are used to design NOR gates in CVSL technology. Gate voltage to these MOSFET'S are applied in differential form that alter the on & off time of these MOSFET'S which results in decrease in power dissipation [21]. Inputs are given to the gate terminal of T1 & T2 MOSFET's & output from Vout (+) and Vout (-). The number of MOSFET used for this architecture is 31.

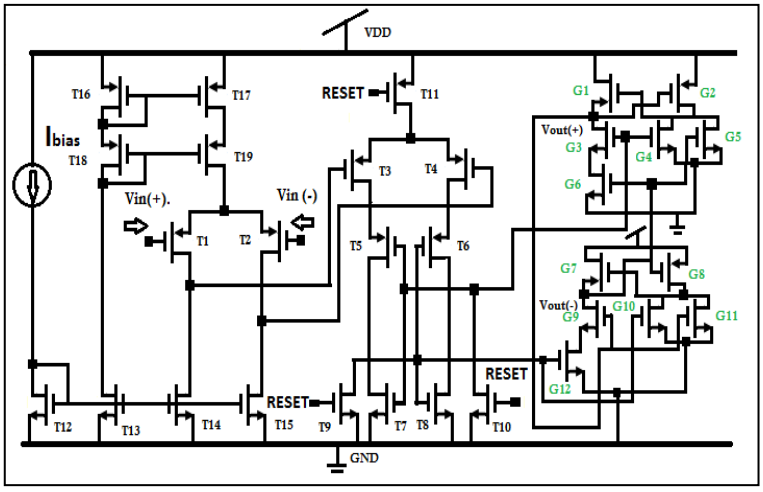


Figure 3. Regenerative Comparator in CVSL technology

2.4. Regenerative Comparator in Power Gating Technology

Figure 4 depicts the architecture for regenerative comparator using power gating technology [16]. Power Gating is the most effective technique to reduce the power dissipation especially leakage power [22] [23]. Pre-charge and evaluation mode are followed for the execution of full comparison phase. Dual input fully differential pair that comprise of T1 & T2 MOSFET's are used for feeding the input signal and output

from Vout (+) and Vout (-). P1, P2, P3 & P4 MOSFETS are used to operate the circuit in Pre-charge and evaluation mode. G1 to G8 MOSFET'S are used for designing two nor gates at the end of the schematic. Substantial power reduction is obtained with this technique. Total MOS devices used in this technique is same as CVSL technology.

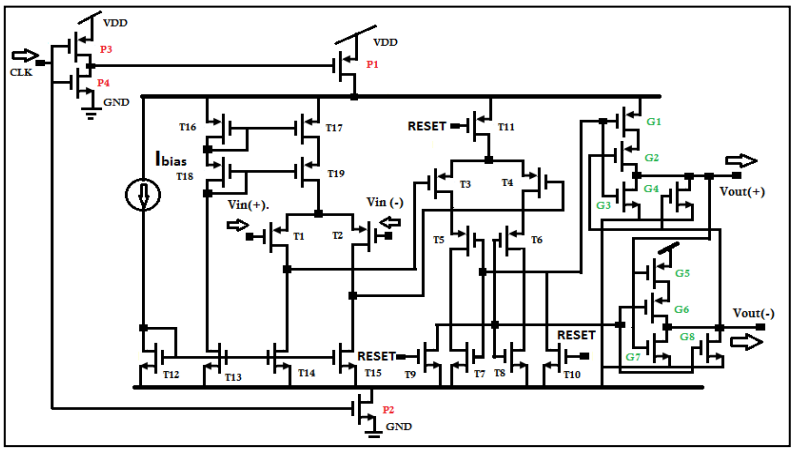
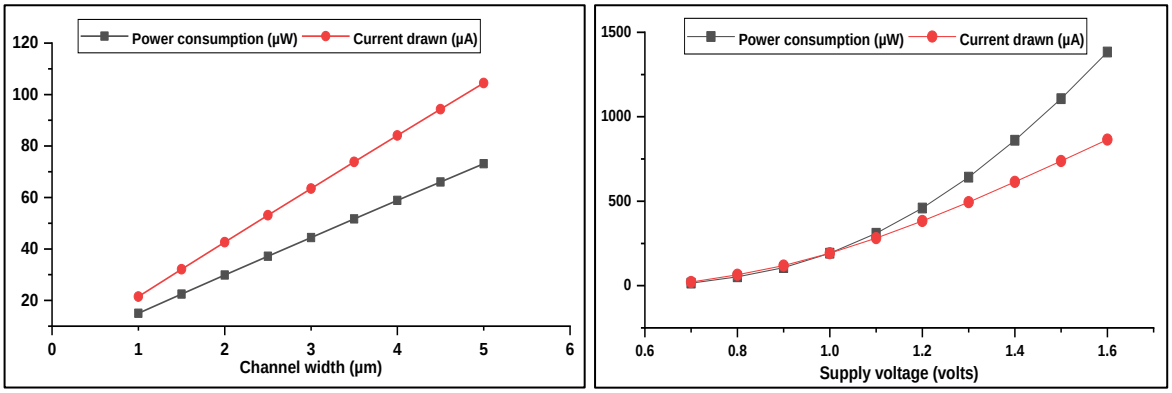


Figure 4. Regenerative Comparator in Power Gating Technology

3. RESULTS AND DISCUSSION

In this segment transient analysis for the above four circuits are done by varying channel width, supply voltage and temperature. Simulations are performed using spice based 90 nm CMOS technology.

Figure 5 gives the graphical details regarding to the power consumption and current drawn for the regenerative comparator [8] and its variation with channel width and supply voltage respectively. In Figure 5(a) channel width is varied from 1 µm to 5 µm by keeping the supply voltage constant (0.7 V). The percentage increase due to the variation in channel width is 38.67. Figure 5(b) shows variations in power dissipation and current drawn by varying the supply voltage from 1.7 V to 0.7 V at channel width of 1µm. Due to this variation power dissipation decreases by 98 percent.



(a) (b)

Figure 5. (a) Power consumption & current drawn vs channel width; (b) Power consumption & current drawn vs supply voltage

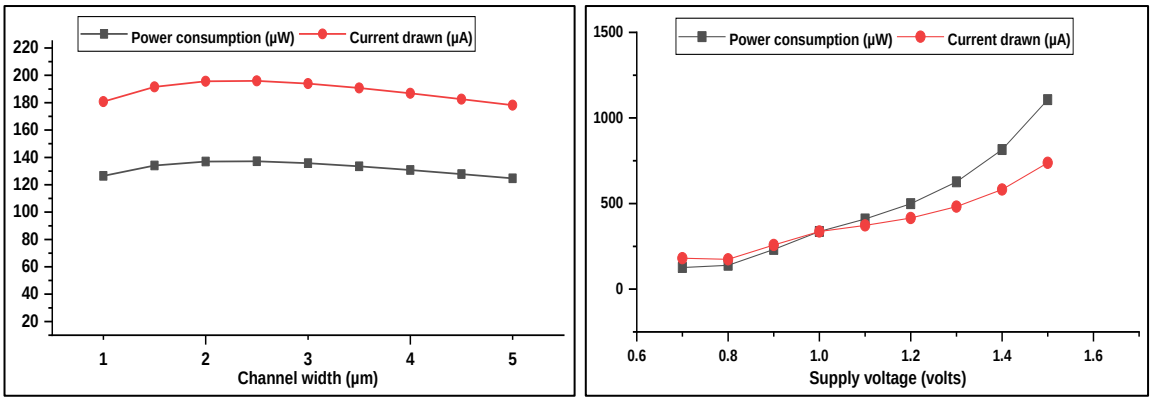
Table 1 gives the details regarding to the variations in power consumption and current drawn by the circuit to the varying temperature in different modes i.e. leakage, static, dynamic, total. Power consumption and current drawn values shows variations when temperature varies from -35° to 80° Celsius.

Table 1. Total, static, dynamic & leakage power consumption of regenerative comparator at different temperature

	Leakage		Static		Dynamic		Total	
Temp	PC (nW)	CD (nA)	PC (µW)	CD (µA)	PC (µW)	CD (µA)	PC (µW)	CD (µA)
80°	122.85	175.50	13.57	19.39	1.91	2.73	15.49	22.12
75°	111.62	159.46	13.62	19.45	1.84	2.64	15.47	22.10
65°	091.41	130.59	13.70	19.58	1.71	2.44	15.41	22.02
55°	074.02	105.75	13.78	19.69	1.56	2.23	15.35	21.93
45°	059.22	084.60	13.85	19.79	1.41	2.02	15.26	21.81
35°	046.76	066.81	13.90	19.86	1.25	1.79	15.16	21.65
25°	036.42	052.03	13.92	19.89	1.09	1.56	15.02	21.46
15°	027.96	039.94	13.92	19.89	0.93	1.34	14.86	21.23
05°	021.14	030.20	13.88	19.83	0.78	1.12	14.66	20.95
00°	018.28	026.11	13.84	19.77	0.71	1.01	14.55	20.79
-05°	015.74	022.49	13.79	19.70	0.64	0.91	14.43	20.62
-15°	011.56	016.52	13.64	19.49	0.51	0.73	14.16	20.23
-25°	008.39	011.99	13.44	19.20	0.41	0.58	13.85	19.79
-35°	006.04	008.63	13.18	18.82	0.32	0.46	13.50	19.29

As the temperature increases leakage & dynamic power consumption increases on the other hand static power consumption also shows this increasing pattern but slight variation at higher temperatures. Thus, the total power consumption also increases from 13.50 µW at -35° C to 15.49 µW at 80° C. Total power consumption increases by 14 percent due to the variation in temperature.

Figure 6 gives the graphical details regarding to the power consumption and current drawn for the regenerative comparator designed using psuedo NMOS technology and its variation with channel width and Supply voltage respectively. In Figure 6(a) channel width is varied from 1 µm to 5 µm by keeping the supply voltage constant (0.7 V). The power consumption is maximum at 2.5 µm that is 137.13 µW at this circuit also draw maximum current from supply voltage. Figure 6(b) shows variations in power dissipation and current drawn by varying the supply voltage from 1.7 V to 0.7 V at channel width of 1 µm. Due to this variation minimum power consumption is at 0.7 V that is 126.53 µW and maximum at 1.5 V that is 1106.00 µW.



(a) (b)

Figure 6. (a) Power consumption & current drawn vs channel width; (b) Power consumption & current drawn vs supply voltage

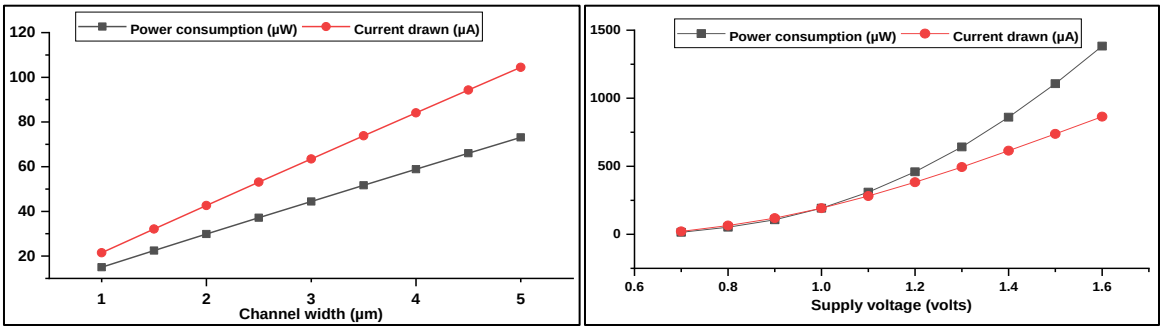
Table 2 gives the details regarding to the variations in power consumption and current drawn by the circuit to the varying temperature in different modes i.e. leakage, static, dynamic, total. Power consumption and current drawn values shows variations when temperature varies from -35° to 80° Celsius. As the temperature increases leakage & dynamic power consumption increases with approximately 300% variation.

Table 2. Total, static, dynamic & leakage power consumption of regenerative comparator (psuedo NMOS) at different temperature

Temp	Leakage		Static		Dynamic		Total	
	PC (µW)	CD (µA)	PC (µW)	CD (µA)	PC (µW)	CD (µA)	PC (µW)	CD (µA)
80°	15.62	22.31	080.43	114.90	326.61	466.59	407.04	581.49
75°	14.84	21.20	081.36	116.23	330.40	472.00	411.77	588.24
65°	13.34	19.06	083.29	118.99	080.38	114.83	163.67	233.82
55°	11.92	17.03	085.31	121.87	063.16	090.23	148.47	212.11
45°	10.59	15.13	087.42	124.89	051.38	073.40	138.81	198.30
35°	09.35	13.36	089.64	128.06	042.21	060.30	131.85	188.37
25°	08.22	11.74	091.97	131.39	034.55	049.36	126.53	180.75
15°	07.19	10.28	094.42	134.89	027.51	039.30	121.93	174.19
05°	06.28	08.98	097.01	138.58	020.06	028.66	117.07	167.25
00°	05.87	08.39	098.35	140.50	016.10	023.00	114.46	163.51
-05°	05.49	07.84	099.73	142.48	012.09	017.27	111.82	159.75
-15°	04.82	06.89	102.61	146.59	004.00	005.72	106.62	152.32
-25°	04.29	06.13	105.66	150.95	-003.97	-005.68	101.69	145.27
-35°	03.89	05.56	108.90	155.57	-011.31	-016.17	097.58	139.40

On the other hand, static power consumption follows inverse rule with temperature having maximum value of 108.90 µW at -35° C. Thus, the total power consumption also increases from 97.58 µW at -35° C to 407.04 µW at 80° C. Total power consumption increases by 317% due to the variation in temperature.

Figure 7 gives the graphical details regarding to the power consumption and current drawn for the regenerative comparator designed using CVSL technology and its variation with channel width and supply voltage respectively. Figure 7(a) depict the varitions when channel width is varied from 1 µm to 5 µm by keeping the supply voltage constant (0.7 V). The power consumption for this circuit is maximum at 5 µm that is 256.67 µW and draw maximum current from supply voltage. On the otherside in figure 7(b) the variations in power dissipation and current drawn by varying the supply voltage from 1.7 V to 0.7 V at channel width of 1 µm is shown. Due to this variation minimum power consumption is at 0.7 V that is 18.94 µW and maximum at 1.3 V that is 399.59 µW.



(a) (b)

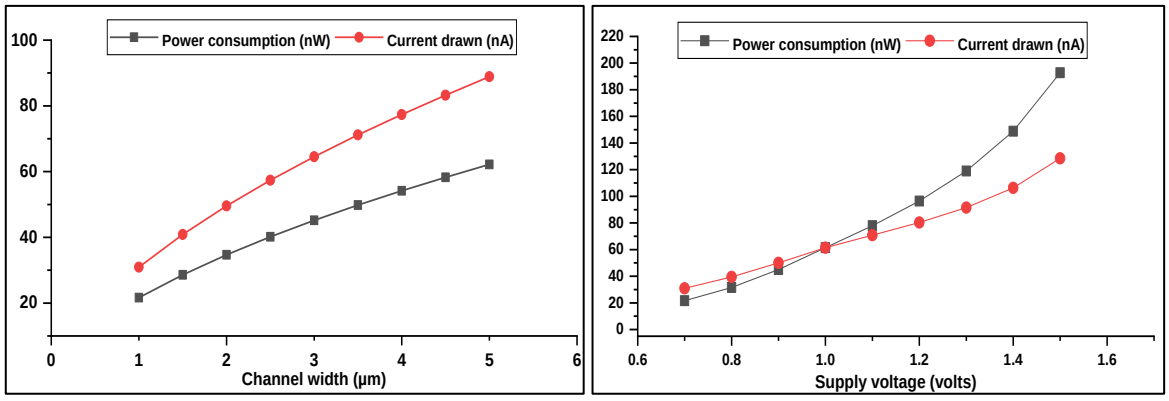
Figure 7. (a) Power consumption & current drawn vs channel width; (b) Power consumption & current drawn vs supply voltage

Table 3 gives the details regarding to the variations in power consumption and current drawn by the regenerative comparator designed using CVSL technology to the varying temperature in different modes i.e. leakage, static, dynamic, total. Power consumption and current drawn values shows variations when temperature varies from -35° to 80° Celsius. As the temperature increases leakage power consumption increases with approximately 300% percent variation maximum value of 2378.64 nW at 80° C. On the other hand, static power consumption increases with increase in temperature having maximum value of 0.93 µW at 80° C. Dynamic power consumption shows abrupt nature as it increases and decreases with temperature variations. Maximum value of dynamic power consumption is 23.37 µW at 65° C & minimum value of 16.34 µW at -5° C. Thus, the total power consumption also follows the same abrupt nature as dynamic power consumption follows. Total power consumption attains its maximum value of 24.20µW at 65° C and minimum value of 16.77 µW at -5° C.

Table 3. Total, static, dynamic & leakage Power consumption of regenerative comparator (CVSL Technology) at different temperature

Temp	Leakage		Static		Dynamic		Total	
	PC (nW)	CD (nA)	PC (µW)	CD (µA)	PC (µW)	CD (µA)	PC (µW)	CD (µA)
80°	2378.64	3398.06	0.93	1.33	00.00	00.01	00.94	01.34
75°	2261.27	3230.38	0.89	1.28	00.00	00.01	00.90	01.29
65°	2035.81	2908.30	0.82	1.18	23.37	33.39	24.20	34.57
55°	1823.35	2604.78	0.76	1.08	21.25	30.36	22.02	31.45
45°	1624.54	2320.77	0.69	0.99	19.96	28.52	20.66	29.52
35°	1439.97	2057.09	0.63	0.91	19.06	27.23	19.70	28.14
25°	1270.13	1814.47	0.58	0.83	18.36	26.23	18.94	27.06
15°	1115.49	1593.55	0.52	0.75	17.74	25.34	18.27	26.10
05°	0976.45	1394.94	0.47	0.68	17.05	24.37	17.53	25.05
00°	0912.92	1304.18	0.45	0.64	16.69	23.85	17.15	24.50
-05°	0853.44	1219.21	0.43	0.61	16.34	23.34	16.77	23.96
-15°	0746.86	0166.95	0.38	0.55	22.19	31.71	22.58	32.26
-25°	0657.17	0938.82	0.34	0.49	19.33	27.62	19.68	28.12
-35°	0584.98	0835.69	0.30	0.44	18.03	25.76	18.34	26.20

Figure 8 gives the details regarding to the power consumption and current drawn for the regenerative comparator designed using power gating technology. Figure 8(a) grphicaly shows the variations when channel width is varied from 1 µm to 5 µm by keeping the supply voltage constant (0.7 V). The power consumption is maximum at 5 µm that is 62.20 µW at this circuit also draw maximum current of 88.86 µA from supply voltage. Figure 8(b) shows variations in power dissipation and current drawn by varying the supply voltage from 1.7 V to 0.7 V at channel width of 1 µm. Due to this variation minimum power consumption is at 0.7 V that is 21.66 µW and maximum at 1.5 V that is 192.75 µW.



(a) (b)

Figure 8. (a) Power consumption & current drawn vs channel width; (b) Power consumption & current drawn vs supply voltage

Table 4 gives the details regarding to the variations in power consumption and current drawn by the regenerative comparator designed using power gating technology to the varying temperature in different modes i.e. leakage, static, dynamic, total. As the temperature increases leakage power consumption increases with approximately 300% percent variation maximum value of 33.53 nW at 80° C. On the other hand, static power consumption increases with increase in temperature having maximum value of 46.53 nW at 80° C.

Table 4. Total, static, dynamic & leakage Power consumption of regenerative comparator (gating Technology) at different temperature

Temp	Leakage		Static		Dynamic		Total	
	PC (nW)	CD (nA)	PC (nW)	CD (nA)	PC (nW)	CD (nA)	PC (nW)	CD (nA)
80°	33.53	47.91	46.53	66.47	0.00760	0.01086	46.52	66.46
75°	30.36	43.37	43.74	62.48	0.00511	0.00730	43.73	62.48
65°	24.66	35.24	38.48	54.97	0.00238	0.00339	38.48	54.97
55°	19.80	28.29	33.66	48.09	0.00118	0.00167	33.66	48.08
45°	15.69	22.41	29.26	41.81	0.00062	0.00087	29.26	41.80
35°	12.25	17.51	25.26	36.09	0.00034	0.00048	25.26	36.09
25°	09.43	13.47	21.66	30.95	0.00019	0.00026	21.66	30.95
15°	07.13	10.19	18.46	26.38	0.00009	0.00013	18.46	26.38
05°	05.30	07.58	15.68	22.41	0.00003	0.00003	15.68	22.41
00°	04.54	06.49	14.45	20.65	0.00000	0.00000	14.45	20.65
-05°	03.58	05.11	13.32	19.03	0.00003	0.00003	13.32	19.03
-15°	02.58	03.68	11.37	16.25	0.00007	0.00009	11.37	16.25
-25°	01.83	02.62	09.82	14.03	0.00011	0.00015	09.82	14.03
-35°	01.41	02.01	08.92	12.95	0.28376	0.61164	08.64	12.34

Dynamic power consumption shows very small variations of few nW. Thus, the total power consumption also attains marginal value as compared to earlier discuss circuits. Total power consumption attains its maximum value of 46.52 nW at 80° C and minimum value of 8.64 nW at -35° C.

Table 5 shows the brief comparison of the results for all four types of schematics discussed above. The regenerative comparator using power gating technique shows minimum power consumption of 21.66614 nW as compared to others while drawing a current of 30.95163 nA from 0.7 V supply voltage.

Table 5. Comparison of results

	Regenerative comparator	Regenerative comparator with pseudo NMOS	Regenerative comparator with CVSL	Regenerative comparator with power gating
Temperature	25°C	25°C	25°C	25°C
No. Of MOSFETS	27	25	31	31
Channel Length	90 nm	90 nm	90 nm	90 nm
Channel Width	1 µm	1 µm	1 µm	1 µm
Supply voltage	0.7 V	0.7 V	0.7 V	0.7 V
Total Power consumption	15.02696µW	126.53128 µW	18.94745 µW	21.66614nW
Total Current drawn	21.46708µA	180.75897 µA	27.06779 µA	30.95163nA

Table 6 shows the variations in the power consumptions for all four schematics when the temperature is varied from -35° to +80° Celsius.

Table 6. Percentage variation Power consumption (PC) with temperature

	Regenerative comparator	Regenerative comparator with pseudo NMOS	Regenerative comparator with CVSL	Regenerative comparator with power gating
Temperature	-35° to +80°	-35° to +80°	-35° to +80°	-35° to +80°
Leakage PC	83.39 to 237.27	52.63 to 89.93	45957.2 to 87.27	85.02 to 255.65
Static PC	5.37 to 2.51	18.40 to 12.55	46.79 to 60.57	58.80 to 114.76
Dynamic PC	70.19 to 74.16	132.75 to 845.24	1.79 to 99.95	149247 to 3900
Total PC	10.10 to 3.08	22.87 to 221.69	3.17 to 95.02	60.11 to 114.72

4. COMPARISON

In order to compare simulation results four more comparator structures are again simulated in 90nm CMOS technology. These four structures are dynamic comparator (conventional) [24], dynamic comparator (double tail) [24], dynamic comparator (modified double tail) [24], comparator with two cross-coupled inverters [25]. Results that are obtained after simulation along with four recent comparator structures [26] [27]-[29] which are also included for comparison are shown in Table 7. Regenerative comparator (Power gating) shows optimum results in comparison.

Table 7. Comparison of results at 25° Celsius

	No. of MOSFETS	Channel Length	Channel Width	Supply voltage	Total Power consumption
Dynamic Comparator (Conventional) [24]	09	90 nm	1 µm	0.7 V	02.77 nW
Dynamic Comparator (Double Tail) [24]	14	90 nm	1 µm	0.7 V	10.60 nW
Dynamic Comparator (Modified Double Tail) [24]	18	90 nm	1 µm	0.7 V	14.19 nW
Comparator with two cross-coupled inverters [25]	15	90 nm	1 µm	0.7 V	13.84 µW
[26]	14	90 nm	-	1.0 V	82.00 µW
[27]	-	40 nm	-	0.6 V	01.50 µW
[28]	16	180 nm	-	1.6 V	17.00 µW
[29]	06	65 nm	-	1.2 V	755.00 µW
Regenerative comparator [13]	27	90 nm	1 µm	0.7 V	15.02 µW
Regenerative comparator with power gating	31	90 nm	1 µm	0.7 V	21.66 nW

So, by comparing on the basis of power consumption with its variation with channel width, supply voltage & temperatures it is clearly observed that regenerative comparator with power gating show good performance with respect to others.

5. CONCLUSION

Three different power reduction techniques are implemented on regenerative comparator circuits. Out of these three techniques power gating technique shows substantial decrease in total power consumption along with the reduction in leakage current. Total power consumption of 15.026 µW reduced to 21.666 nW for regenerative comparator with power gating technique which certainly improves its performance. Four conventional & four recent comparator structures are compared with regenerative comparator (power gating). Hence it is observed that the regenerative comparator with power gating technique shows optimum power consumption with high speed of operation due to regenerative latch at its end. This definitely will increase its applicabilties in high speed and low power UDSM data converter circuits designs.

REFERENCES

[1] B. Razavi, "Principles of Data Conversion System Design," *AT&T Bell laboratories*, IEEE Press, 1995.
[2] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, Second Edition, 2002.
[3] C. Fayomi, *et al.*, "Low power/low voltage high-speed CMOS differential track and latch comparator with rail-to-rail input," *Proc.ISCAS5*, pp. 653–656, 2000.
[4] A. Al, *et al.*, "An Improved A Low Power CMOS TIQ Comparator Flash ADC," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol/issue: 12(7), pp. 5204-5210, 2014.
[5] M. Marufuzzaman, *et al.*, "Design of 3-Bit ADC in 0.18µm CMOS Process," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol. 12, pp. 5197-5203, 2014.
[6] M. Muhamad, *et al.*, "Design of Low Power Low Noise Amplifier using Gm-boosted Technique," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 9, pp. 685-689, 2018.
[7] B. Goll and H. Zimmermann, "Low power 600MHz comparator for 0.5V supply voltage in 0.12µm CMOS," *IEEE Electron. Lett.* Vol/issue: 43(7), pp. 388-390, 2007.
[8] S. Goyal and V. Sulochana, "Design of Low Leakage Multi Threshold (V_{th}) CMOS Level Shifter," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 3, pp. 584-592, 2013.
[9] N. Mukahar and S. H. Ruslan, "A 93.36 dB, 161 MHz CMOS Operational Transconductance Amplifier (OTA) for a 16 Bit Pipeline Analog-to-Digital Converter (ADC)," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 2, pp. 106-111, 2012.
[10] S. K. Patnaik and S. Banerjee, "Noise and Error Analysis and Optimization of a CMOS Latched Comparator, International Conference on Communication Technology and System Design 2011," *Procedia Engineering*, vol. 30, pp. 210–217, 2012.
[11] G. M. Yin, *et al.*, "A high-speed CMOS comparator with 8-bit resolution," *IEEE J. Solid State Circuits*, vol/issue: 27(2), pp. 208–211, 1992.
[12] J. N. Reddy, *et al.*, "Subthreshold Dual Mode Logic," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 3, pp. 141-148, 2014.
[13] M. Saberi and R. Lotfi, "Segmented Architecture for Successive Approximation Analog-to-Digital Converters," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol/issue: 22(3), 2014.
[14] H. Jeong, *et al.*, "Pseudo NMOS Based Sense Amplifier for High Speed Single-Ended SRAM," *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille*, pp. 331-334, 2014.
[15] K. M. Chu and D. L. Pulfrey, "A Comparison of CMOS Circuit Techniques: Differential Cascode Voltage Switch Logic Versus Conventional Logic," *IEEE Journal of Solid-State Circuits*, vol/issue: SC-22(4), 1987.
[16] K. Lee and S. S. Wong, "Fault-Tolerant FPGA with Column-Based Redundancy and Power Gating Using RRAM," *IEEE Transactions on Computers*, vol/issue: 66(6), 2017.

[17] B. H. Nagpara, "A 45 nm 6 Bit Low Power Current Steering Digital to Analog Converter Using GDI Logic," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol/issue: 16(1), pp. 46-51, 2015.
[18] P. Zhao, *et al*., "Low-Power Clocked-Pseudo-NMOS Flip-Flop for Level Conversion in Dual Supply Systems," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol/issue: 17(9), pp. 1196-1202, 2009.
[19] R. F. Mirzaee, *et al*., "Differential Cascode Voltage Switch (DCVS) Strategies by CNTFET Technology for Standard Ternary Logic," *Microelectronics Journal*, 2013. http://dx.doi.org/10.1016/j.mejo.2013.08.010i
[20] M. C. Casey, *et al.*, "HBD Using Cascode-Voltage Switch Logic Gates for SET Tolerant Digital Designs," *IEEE Transactions on Nuclear Science*, vol/issue: 52(6), 2005.
[21] M. C. Casey, *et al.*, "Single-Event Tolerant Latch Using Cascode-Voltage Switch Logic Gates," *IEEE Transactions on Nuclear Science*, vol/issue: 53(6), 2006.
[22] J. J. Johannaha, *et al.*, "Standby and dynamic power minimization using enhanced hybrid power gating structure for deep-submicron CMOS VLSI," *Microelectronics Journal*, 2017. http://dx.doi.org/10.1016/j.mejo.2017.02.003
[23] A. R. Trivedi, *et al.*, "In Situ Power Gating Efficiency Learner for Fine-Grained Self-Adaptive Power Gating," *IEEE Transactions on Circuits and Systems*, vol/issue: 61(5), 2014.
[24] S. B. Mashhadi and R. Lotfi, "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator," *IEEE Transactions onVery Large Scale Integration (VLSI) Systems*, vol/issue: 22(2), 2014.
[25] J. I. Lee and J. I. Song, "Flash ADC Architecture using Multiplexers to Reduce a Preamplifier and Comparator Count," *IEEE*, 2013.
[26] A. Rezapour, *et al*., "Low Power High Speed Dynamic Comparator," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, pp. 1-5, 2018.
[27] O. Aiello, *et al.*, "Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation down to 0.3 V," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, pp. 1-5, 2018.
[28] A. Khorami and M. Sharifkhani, "A Low-Power High-Speed Comparator for Precise Applications," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, pp. 1–12, 2018.
[29] M. Nasrollahpour, *et al.*, "A high-speed, low-offset and low-power differential comparator for analog to digital converters," *2017 International SoC Design Conference (ISOCC)*, Seoul, Korea (South), pp. 220-221, 2017.