International Journal of Electrical and Computer Engineering (IJECE)
Vol. 6, No. 1, February 2016, pp. 320~329
ISSN: 2088-8708, DOI: 10.11591/ijece.v6i1.8700

Modelling and Design of Inverter Threshold Quantization Based Current Comparator using Artificial Neural Networks

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Article Info

Article history:

Received Aug 1, 2015
Revised Oct 4, 2015
Accepted Oct 21, 2015

Keyword:

Artificial neural networks
Aspect ratio elements
CMOS inverter
Current comparator
Multilayer perceptron

ABSTRACT

Performance of a MOS based circuit is highly influenced by the transistor dimensions chosen for that circuit. Thus, proper dimensioning of the transistors plays a key role in determining its overall performance. While choosing the dimension is critical, it is equally difficult, primarily due to complex mathematical formulations that come into play when moving into the submicron level. The drain current is the most affected parameter which in turn affects all other parameters. Thus, there is a constant quest to come up with techniques and procedure to simplify the dimensioning process while still keeping the parameters under check. This study presents one such novel technique to estimate the transistor dimensions for a current comparator structure, using the artificial neural networks approach. The approach uses Multilayer perceptrons as the artificial neural network architectures. The technique involves a two step process. In the first step, training and test data are obtained by doing SPICE simulations of modelled circuit using 0.18µm TSMC CMOS technology parameters. In the second step, this training and test data is applied to the developed neural network architecture using MATLAB R2007b.

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1. INTRODUCTION

The last few years have witnessed a tremendous growth in the field of intelligent systems such as fuzzy logic and expert systems. Inspired by biological neural networks, one such success has been achieved in evolution of artificial neural networks (ANNs) [1]. ANNs are characterized by their distinctive capabilities of exhibiting massive parallelism, generalization ability and being good function approximators. This renders them useful for solving a variety of problems in pattern recognition, prediction, optimization and associative memory [2]-[4]. Additionally, they are also being employed in circuit modelling [5].

Traditional approach for determination of the design parameters of any circuit employs mathematical modelling and analysis of various equations. This procedure is quiet complex and arduous especially when working in submicron technology where the dependence of various circuit parameters is governed by complex and non-linear equations. An alternative approach to reduce this complexity is provided by artificial neural network (ANN) where the network is trained to imitate the behaviour of the circuit being designed.

Recently, ANNs have been used to model analog and digital circuits, specifically focussing on determination of transistor dimensions, as in [6]-[9]. Further, in [10], the switching characteristics of CMOS inverter have also been modelled while Microwave transistors and circuit modelling have been elucidated in [11]-[12]. In [13] the speed control the speed of a Double Star Induction Motor has been modelled Induction

Motor. Further, in [14] a solution for OTA circuits modelling has been proposed. An illustration of technology independent circuits sizing for basic analog circuits has been described in [15].

In this paper, as a first, a current comparator structure has been modelled and transistor dimensions of the constituent transistors are determined using ANN. Two ANN architectures have been used to separately model the different stages of the current comparator. The training and test data have been obtained from the SPICE simulations of the circuit using 0.18 μm TSMC parameters. The neural network toolbox of MATLAB R2007b has been used to train ANN architectures. The trained nets have been simulated in MATLAB to obtain the transistor dimensions which are subsequently used for verifying the current comparator functionality and determining various performance parameters.

2. CURRENT COMPARATOR

A current comparator is a very popular current mode circuit that compares an input current with a reference current and provides output as voltage [16]–[24]. It essentially calculates the difference between the input and the reference current and depicts the results as a voltage level at the output. However, these circuits [16]-[24] are not complete current comparators as they lack the differencing structure and directly process the pre-calculated difference between the input and reference currents to obtain the output voltage level. Thus, for the structures of [16]–[24] to be considered fully functional current comparators, it is necessary to include a current differencing structure at the input. The current comparator employed and modelled in this paper eliminates this drawback and uses an internally generated reference for comparison with the input current, thereby eliminating the need of an additional current differencing structure.

2.1. Modeled Current Comparator

This modelled current comparator is shown in Figure 1. It comprises of three stages namely a current to voltage converter (Stage 1); a symmetric inverter (Stage 2) and an additional inverter (Stage 3). A brief description of each stage is as follows: Stage 1 comprising a diode connected NMOS (Mn1) is designed to provide an output voltage ($V_{GS,ref}$) equal to half of voltage swing of the following symmetric inverter for given reference current (I_{ref}). The input current whenever differs from I_{ref}, a deviation in the value from $V_{GS,ref}$ is observed at the gate of Mn1. The Stage 2 comprising Mp2-Mn2 is a symmetrical CMOS inverter with switching voltage equal to $V_{GS,ref}$. It provides an output equal to $V_{GS,ref}$ for an input of $V_{GS,ref}$. Any deviation from $V_{GS,ref}$ at input of Stage 2 causes a larger variation at its output. Thus when input current (I_{in}) < I_{ref} the output of Stage 1 becomes less than $V_{GS,ref}$ which in turn makes output of Stage 2 high. Similarly when I_{in} > I_{ref} the output of Stage 2 becomes low. Stage 3 comprising Mp3-Mn3 is an additional CMOS inverter that provides rail to rail swing at the output node.

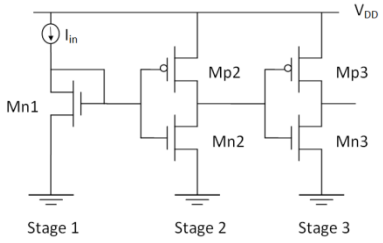

Figure 1. Modelled Current Comparator

For modelling the circuit, aspect ratio of the transistors used in Stages 1 and 2 can be calculated using the following method:

The transistor Mn1, being diode connected, operates in saturation region. The reference current I_{ref} is related to the gate to source voltage $V_{GS,ref}$ by

$$I_{ref} = \frac{\mu_n C_{ox}}{2} \times \left(\frac{W}{L}\right)_{Mn1} \times \left(V_{GS,ref} - V_{To,n}\right)^2 \quad (1)$$

where the symbols have their usual meanings. Hence aspect ratio for Mn1 is given by

$$\left(\frac{W}{L}\right)_{Mn1} = \frac{2I_{ref}}{\mu_n C_{ox}\left(V_{GS,ref}-V_{To,n}\right)^2} \quad (2)$$

The inverter in Stage 2 is symmetric so transistors Mp2 and Mn2 also operate in saturation region at its switching threshold ($V_{GS,ref}$). Equating drain currents of Mp2 and Mn2 gives

$$\frac{\mu_n C_{ox}}{2} \times \left(\frac{W}{L}\right)_{Mn2} \times \left(V_{GS,n} - V_{To,n}\right)^2 = \frac{\mu_p C_{ox}}{2} \times \left(\frac{W}{L}\right)_{Mp2} \times \left(V_{GS,p} - V_{To,p}\right)^2 \quad (3)$$

Using $V_{GS,n} = V_{GS,ref}$ and $V_{GS,p} = V_{GS,ref} - V_{DD}$ for stage 2, (3) modifies to

$$\frac{\mu_n C_{ox}}{2} \times \left(\frac{W}{L}\right)_{Mn2} X \left(V_{GS,\,ref} - V_{T0,\,n}\right)^2 = \frac{\mu_p C_{ox}}{2} \times \left(\frac{W}{L}\right)_{Mp2} \times \left(V_{GS,\,ref} - V_{DD} - V_{To,\,p}\right)^2 \quad (4)$$

or

$$\mu_n \times \left(\frac{W}{L}\right)_{Mn2} \times \left(V_{GS,\,ref} - V_{T0,\,n}\right)^2 = \mu_p \times \left(\frac{W}{L}\right)_{Mp2} \times \left(V_{GS,\,ref} - V_{DD} - V_{To,\,p}\right)^2 \quad (5)$$

or

$$V_{GS,ref} \times \left(1 + \sqrt{\frac{\mu_p\left(\frac{W}{L}\right)_{Mp2}}{\mu_n\left(\frac{W}{L}\right)_{Mn2}}}\right) = V_{To,n} + \sqrt{\frac{\mu_p\left(\frac{W}{L}\right)_{Mp2}}{\mu_n\left(\frac{W}{L}\right)_{Mn2}}} \times \left(V_{DD} + V_{To,p}\right) \quad (6)$$

The value of switching threshold voltage of the stage 2 CMOS Inverter is given by

$$V_{GS,ref} = \frac{V_{To,n} + \sqrt{\frac{\mu_p\left(\frac{W}{L}\right)_{Mp2}}{\mu_n\left(\frac{W}{L}\right)_{Mn2}}} \times \left(V_{DD} + V_{To,p}\right)}{\left(1 + \sqrt{\frac{\mu_p\left(\frac{W}{L}\right)_{Mp2}}{\mu_n\left(\frac{W}{L}\right)_{Mn2}}}\right)} \quad (7)$$

The aspect ratio for Mn2 and Mp2 are related as:

$$\frac{\left(\frac{W}{L}\right)_{Mn2}}{\left(\frac{W}{L}\right)_{Mp2}} = \frac{\left(V_{GS,ref} - V_{DD} - V_{To,p}\right)^2}{\left(V_{GS,ref} - V_{To,n}\right)^2} \quad (8)$$

The aspect ratio of CMOS inverter in Stage 3 is kept identical to the one used in Stage 2 for the sake of regularity.

2.2. Role of Neural Networks

The method outlined in section 2.1 for aspect ratios calculation is effective for hand calculation. When working with small geometry devices, this method does not provide correct estimation for aspect ratio due to complex nonlinear dependence of drain current (I_D) on gate-source(V_{GS}), drain-source(V_{DS}) and bulk-source (V_{BS}) voltages. The general expression for drain current in level 3 [25] model is given by

$$I_D = \frac{\mu_s C_{ox}}{(1-\lambda V_{DS})} \times \frac{W}{L_{eff}} \times \begin{Bmatrix} \left[V_{GS} - V_{FB} - 2|\Phi_F|\frac{V_{DS}}{2}\right] \times V_{DS} \\ -\frac{2}{3} \times \gamma\left[(V_{DS} - V_{BS} + 2|\Phi_F|)^{3/2} - (V_{BS} + 2|\Phi_F|)^{3/2}\right] \end{Bmatrix} \quad (9)$$

where $\mu_s = \frac{\mu}{1+\theta(V_{GS}-V_T)}$, $L_{eff} = L - \Delta L$ and the symbols have their usual meaning. The drain current of (9) is simplified for linear and saturation regions respectively as

$$I_D = \mu_s C_{ox} \times \frac{W}{L_{eff}} \times \left[V_{GS} - V_T - \frac{1+F_B}{2} \times V_{DS}\right] \times V_{DS} \quad (10)$$

$$I_D = \mu_s C_{ox} \times \frac{W}{L_{eff}} \left\{ \begin{array}{c} \left[V_{GS} - V_{FB} - 2|\Phi_F| - \frac{V_{DS}}{2}\right] \times V_{DS} \\ -\frac{2}{3} \times \gamma \times \left[(V_{DS} - V_{BS} + 2|\Phi_F|)^{3/2} - (-V_{BS} + 2|\Phi_F|)^{3/2}\right] \end{array} \right\} \quad (11)$$

where F_B represents dependence of the bulk depletion charge on the three dimensional geometry of the MOSFET and is given by

$$F_B = \frac{\gamma \cdot F_S}{4\sqrt{|2\Phi_F| + V_{SB}}} + F_n \quad (12)$$

Here, parameters F_s and F_n are empirical parameters and are influenced by short channel and narrow channel effects respectively. It is clear from (9) – (12) that the nonlinear and complex dependence of drain current on various parameters makes exact aspect ratios determination too laborious through hand calculations. The neural networks, with (9) – (12) as function approximators, can however be employed to provide sufficiently reliable and accurate results. The current piece of work illustrates the use of ANNs in determining the channel length and width of each of the transistors in Figure 1.

3. CONSTRUCTION OF ANN MODELS

A neuron is one of the basic elements in ANN model which comprises of set of inputs, weight coefficients, also known as synaptic weights, and an activation function [15]. Neurons form the basis of an input layer that has sensory units to collect the information from its environment, an output layer and a number of optional intermediate layer(s) called hidden layers. These hidden layers perform the task of transforming input space to output space. The network is trained using sets of inputs with their corresponding outputs through a training algorithm. Here Multilayer Perceptron (MLP) algorithm is used for finding optimized aspect ratios of the devices used in Figure1.

The MLP is the most common architecture employed for ANN [26] and can implement arbitrary mappings between input and output [27]-[30]. It uses back propagation as learning algorithm wherein the synaptic strengths are systematically modified so that network approximates the desired response more closely. The MLP architecture is shown in Figure 2 where *Li, Lj(j = 1,2,..k), Lo* represent respectively the input layer, *k* hidden layers and the output layer. The input layer receives the input variables used for classification. The network processes the input data present at input layer and calculations are performed in subsequent layers until an output is reached at every output node. This output is subsequently compared against desired output and error is computed. The error is then propagated backwards through the ANN and is used to adjust the synaptic weights that control the network. The training procedure is described with the help of Figure 3.

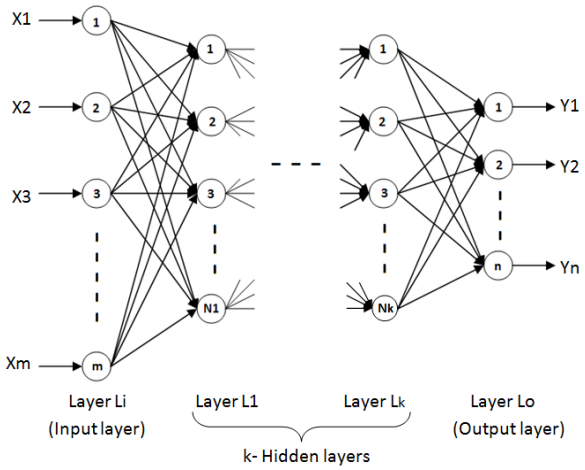

Figure 2. MLP Structure

3.1. Design of ANN Model for STAGE 1

The ANN structure of Figure 2 is used to model Stage 1. The inputs to the network are current I_{ref} and the gate to source voltage $V_{GS,ref}$ (=$V_{DS,ref}$) while the channel length (L_{Mn1}) and width (W_{Mn1}) are regarded as the network outputs. Hence, two neurons each in input and output layer were employed and the MLP of Figure 2 is trained. The channel width and length of the transistor were varied randomly between 0.28 µm and 6.0 µm. For each combination of aspect ratios elements, current from the current source was also varied from 100nA to 2.5mA and the corresponding gate to source voltages ($V_{GS,ref}$) were obtained. This set of data comprising of 1477 samples was then utilized to train the ANN structure in Figure 2 employing Levenberg – Marquardt (LM) back propagation method as the training algorithm. In accordance with the above considerations, the simulations were performed on MATLAB R2007b Neural Network toolbox by considering 3000 epochs and a learning rate of 1.2. The activation function for hidden layers' neurons was taken to be tangent-sigmoid function while pure linear function was chosen for output layer. The training error was aimed at $1x10^{-6}$ and the training was stopped when validation checks reached their maximum value. The corresponding dimensions of transistor Mn1 (channel length (L_{Mn1}) and width (W_{Mn1})) were obtained after training and the value of $V_{GS,ref}$ was estimated through SPICE simulation by applying I_{ref} =5 µA.

Two hidden layers having 5 neurons, and 4 neurons respectively were selected after carrying out the ANN implementation of circuit through a number of iterations in which the number of hidden layers and number of neurons in each layer were varied. In the first iteration, a single layer with a single neuron was employed. However, a single hidden layer in the ANN modelling of stage1 produced a large mean square error as well as large % error between desired and estimated value of V_{GSref}, as depicted in Figure 4. Hence the modelling of the circuit was carried using 2 hidden layers. Numerous iterations were carried out by varying the number of neurons in each hidden layer beginning with one in each layer and finally an optimum solution was reached with keeping neurons as 5 and 4 in the layer 1 and 2 respectively for which the training error was found to be $1.63x10^{-5}$. The results of iterations of stage1 have been consolidated and illustrated in Figure 5, wherein % error between desired and estimated value V_{GSref} has been plotted with respect to the number of neurons in hidden layer 2 for different fixed values of number of neurons in hidden layer 1 (*NL1).* Solid line for NL1=5 is the desired characteristic which yields minimum % error between desired and estimated value of V_{GSref}. Figure 6 depicts the final MLP developed for Stage 1 with one input layer, one output layer and two hidden layers comprising 2, 2, 5 and 4 neurons respectively.

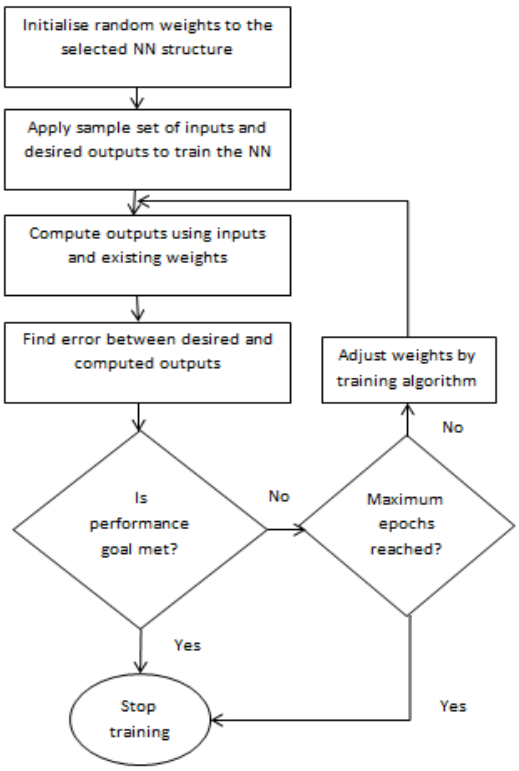

Figure 3. ANN Training Procedure

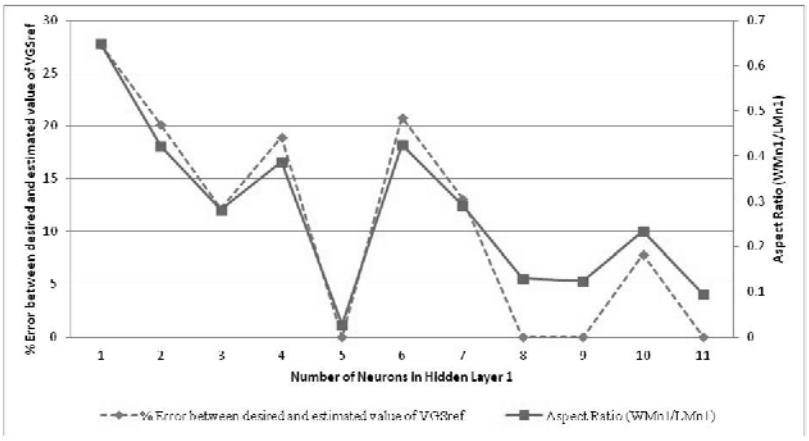

Figure 4. Stage 1-% Error between desired and estimated value of V_{GSref}. Vs Number of Neurons in Hidden Layer 1

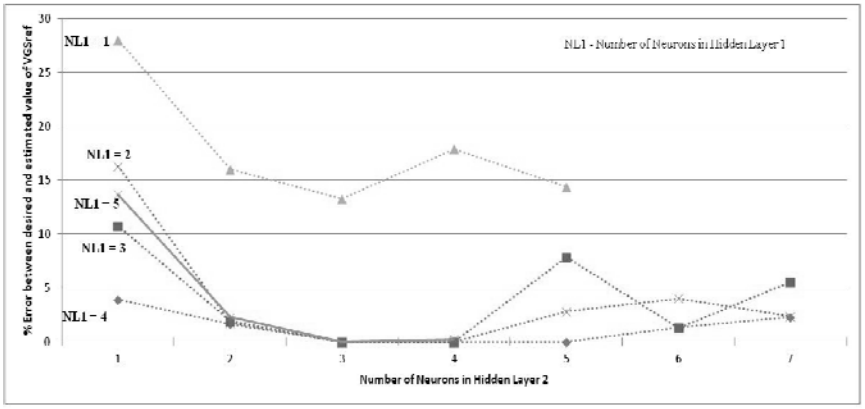

Figure 5. Stage 1-% Error between desired and estimated value of V_{GSref}. Vs Number of Neurons in Hidden Layer 2 for different fixed values of Number of Neurons in Hidden Layer 1

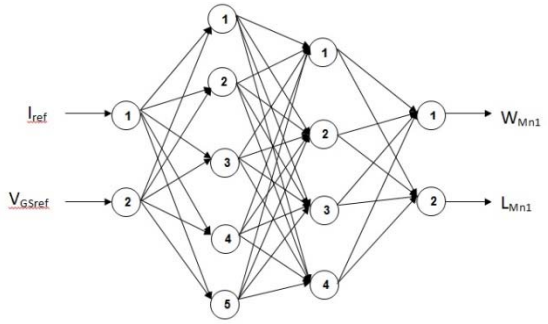

Figure 6. MLP used for implementing stage 1

3.2. Design of ANN Model for Stage 2

Similar to Stage 1, the ANN structure of Figure 2 is used to model Stage 2. The training approach used here is same as that described in subsection 3.1. The channel lengths and channel widths are varied between 0.18 µm and 6.0 µm while the input voltage (V_{in}) is changed from 0 V to 1.8 V during SPICE simulations. A total of 1365 samples were collected in this case. The inputs to the network are input voltage (V_{in}), the output voltage (V_{out}), and channel lengths (L_{Mp2} and L_{Mn2}) of transistors Mp2 and Mn2. The outputs are the channel widths (W_{Mp2} and W_{Mn2}) of transistors Mp2 and Mn2. Hence an input layer with 4 neurons and

output layer with 2 neurons were selected. The number of hidden layers was then increased to two and similar process was carried out. It was observed that by keeping neurons as 6 and 7 in the layer 1 and 2 respectively a minimum % error of 0.11% between desired and estimated value of V_{out} was achieved.
In an attempt to explore the possibility of obtaining smaller transistor sizes as compared to those of two hidden layers, another hidden layer was added. The number of neurons were initially fixed as one per hidden layer and then progressively increased. It was observed that the % error between desired and estimated value of V_{out} is minimum (0.16%) when number of neurons are 6, 4 and 5 respectively in hidden layer 1, 2 and 3 with channel width of transistor MP2 and MN2 (W_{Mp2} and W_{Mn2}) equal to 16.8544 µm and 5.1729 µm respectively. Further, when numbers of neurons are 8, 10 and 7 in hidden layer 1, 2 and 3 respectively, the value of % error between desired and estimated value of V_{out} equal to 2.43% and channel width of transistor MP2 and MN2 (W_{Mp2} and W_{Mn2}) equal to 6.23 µm and 1.7972 µm respectively.

Hence there is a trade off between the number of neurons and transistor sizing. However, we have chosen three hidden layers having 8 neurons, 10 neurons and 7 neurons respectively, giving preference to small transistor sizes over number of neurons. Figure 7 depicts the final MLP developed for Stage 2 with one input layer, one output layer and three hidden layers comprising 4, 2, 8, 10 and 7 neurons respectively. The training error for Stage 2 implementation achieved a value of 9.97518 x10^{-7}.

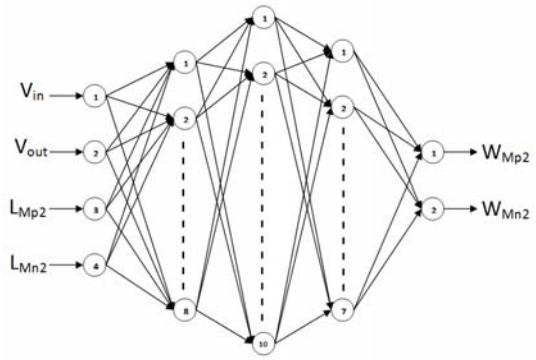

Figure 7. MLP Structure developed for stage 2

4. RESULTS AND ANALYSIS

The current comparator of Figure1 is designed for a reference current of 5µA. The power supply (V_{DD}) of 1.8 V is used. The training and test data is gathered through SPICE simulations based on TSMC 0.18µm CMOS technology parameters. As discussed in section 2.1, the value of $V_{GS,ref}$ for given reference current is taken as $V_{DD}/2$ (0.9 V) for Stage 1. The dimensions for transistor Mn1 are computed using the method described in section 3.1. As Stage 2 uses a symmetrical inverter, the output voltage is $V_{DD}/2$ for an input $V_{GS,ref}$ of $V_{DD}/2$. For stage 2, the inputs are taken as $V_{in} = V_{out} = 0.9$ V, and the channel lengths are taken as $L_p = L_n = 0.18$ µm. The results obtained from MATLAB for Stages 1 and 2 are summarized respectively in Table 1 and Table 2.

The current comparator can also be designed for any reference value other than 5µA by training the MLP network for stage 1 (Figure 4) while keeping the designs of stages 2 and 3 unaltered. Alternatively, it can be emphasized that Stages 2 and 3 once designed for both input and output of $V_{DD}/2$ can be universally employed for any current comparator with any reference value, just by altering the design aspects of stage 1. This renders the structure highly flexible and more adaptable.

Table 1. Result of simulation of ANN of stage 1 in MATLAB

	Parameters	Values
Inputs	I_{ref}	5µA
to NN	$V_{GS,ref}$	0.9V
Outputs	W_{Mn1}	0.2811µm
of NN	L_{Mn1}	1.6020µm

Table 2. Result of simulation of ANN of stage 2 and 3 in MATLAB

	Parameters	Values
Inputs to NN	V_{in}	0.9V
	V_{out}	0.9V
	L_{Mp2}	0.18µm
	L_{Mn2}	0.18µm
Outputs of NN	W_{Mp2}	6.2335µm
	W_{Mn2}	1.7972µm

For the purpose of verification and testing, the modelled current comparator is simulated in SPICE by considering the estimated aspect ratios of transistors Mn1, Mn2 and Mp2 (Table 2 and 3) using 0.18µm TSMC technology and a supply Voltage of 1.8 V. The value of $V_{GS,ref}$ (stage 1) for an input reference current (I_{ref}) of 5 µA and the V_{out} (stage 2) for an input voltage (V_{in}) of 0.9V are determined. The same have been reported in the Table 4 along with their desired values and percentage error. The layout of the modelled current comparator was developed using Microwind Software as illustrated in Figure 8. Post-layout simulations were carried out and the results are shown in Table 4. It is found that there is close agreement between desired and estimated values for both pre and post layout results.

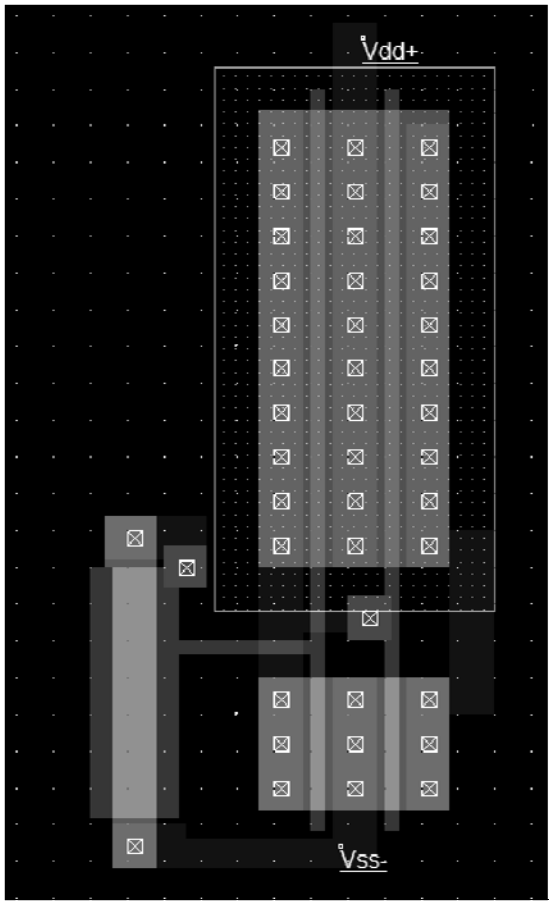

Figure 8. Layout of the Modelled Current Comparator

Table 4.Comparison between desired and estimated values

Parameter	Desired value	Estimated value		%Error	
		Prelayout	Postlayout	Prelayout	Postlayout
V_{GSref} (stage 1)	900 mV	897.223 mV	896.548mV	0.31	0.38
V_{out} (stage 2)	900 mV	921.844 mV	905.913mV	2.43	.657

5. CONCLUSION

This work introduces a pioneer design of an implemented current comparator with the help of ANNs. The ANN implementation is simple and curtails the manual labour needed to solve the complex mathematical equations governing the functioning of the transistors at the submicron level where short channel effects play vital roles. Satisfactory performance for the circuit has been recorded for the predicted aspect ratios parameters using ANN. Further the layout has also been developed for this current comparator and the Pre-layout and Post-layout results are found to be in close agreement.

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