

New Two Simple Sinusoidal Generators with Four 45° Phase Shifted Voltage Outputs Using Single FDCCII and Grounded Components

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ABSTRACT

Two new 45° phase shifted sinusoidal oscillator configurations employing single Second Generation Fully Differential Current Conveyor (FDCCII), two grounded capacitors and two grounded resistors are presented. The proposed oscillators can provide four sinusoidal voltage outputs with each a 45° phase difference. These circuits can also be utilized as voltage-mode quadrature oscillators. Additional output stages incorporation in FDCCII can also result in current outputs spaced 45 degree apart. The proposed circuits enjoy the simplicity and less passive and active component. The Total Harmonic Distortion (THD) of the output waveforms was reasonability values (less than 4.5%). The circuits can supply two equi-quadrature outputs and the Lissajous patterns confirm the quadrature voltage output waveforms. The workability of the circuits is simulated by PSPICE 0.18 μm CMOS technology. The non-ideal analysis and simulation results verifying theoretical analyses are also investigated.

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1. INTRODUCTION

In analog circuit design, sinusoidal oscillators are linear circuits and represent important basic blocks in electric and electronic engineering applications, as for example in signal processing, instrumentation, measurement, communication and control systems [1-5]. Many types of multiphase sinusoidal oscillators (MSOs) have various applications. They can be found in telecommunications for phase modulators, quadrature mixers [6] and single-sideband generators [7], for measurement purposes in vector generators or selective voltmeters [8] or in power electronic system [9].

Numerous multiphase sinusoid oscillator circuits employing different types of active elements such as operational transconductance amplifier (OTA), current feedback operational amplifier (CFOA), current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) current conveyors (CCs) and its different variations have been reported in the literature. [10]-[23].

Fully differential signal processing can be used to extend the dynamic range of analog blocks [24]. Therefore fully differential circuit configurations have been widely used in high frequency analog applications such as switch capacitor filters and mute standard wireless receivers [25], [26] and the references cited therein. Recently fully differential current conveyor (FDCC) based oscillator as a single active element in the circuit design was introduced in the literature [27]-[29].

There are many papers which design of multiphase sine-wave oscillator with four 45° phase shifted voltage outputs using different active and passive components in the literature. Z-copy voltage differencing transconductance amplifier (ZC-VDTA) and five passive elements are used in the design of [30], while the

design of [31] uses single Z-copy controlled gain voltage differencing current conveyor (ZC-CG-VDCC) and four active components. Two Differential Voltage Current Conveyors (DVCCs) and four passive components are used in the design of [32].

FDCCs based voltage mode 45° phase shift outputs have not been earlier attempted in the available literature. This paper presents two new dual mode multiphase oscillator topologies using only a single FDCC, two capacitors and two resistors. The proposed topologies are preferred for IC fabrication due to all the passive components are grounded. These topologies can generate four sinusoidal voltage outputs each with 45° phase difference. These topologies can also be utilized as voltage-mode quadrature oscillators. Additional Z+ and Z- stages incorporation in FDCCII can also result in two sinusoidal current-mode outputs each with 45° separation. Simultaneous four current outputs can also be generated with additional Z stages and two voltages to current converters such as CCII converter.

2. PROPOSED CIRCUITS

The FDCCII was introduced by Alzaher, Elwan and Ismail in 2000 [33], where each of the terminals has been doubled with respect to the original CCII. It is an eight-terminal analog building block shown symbolically in Figure 1, where Y1, Y2, Y3 and Y4 terminals are high impedance terminals while X+ and X- terminals are low impedance ones. The Z+ and Z- terminals exhibit high impedance nodes suitable for current outputs.

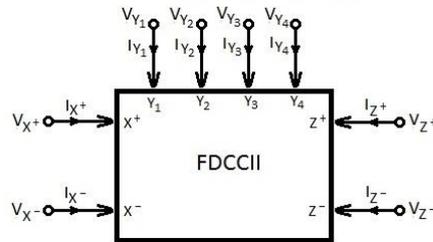


Figure 1. Circuit symbol of FDCCII

The ideal terminal characteristics of FDCCII can be defined by the hybrid matrix as given by Equation 1.

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \tag{1}$$

The proposed circuits are shown in Figure 2.

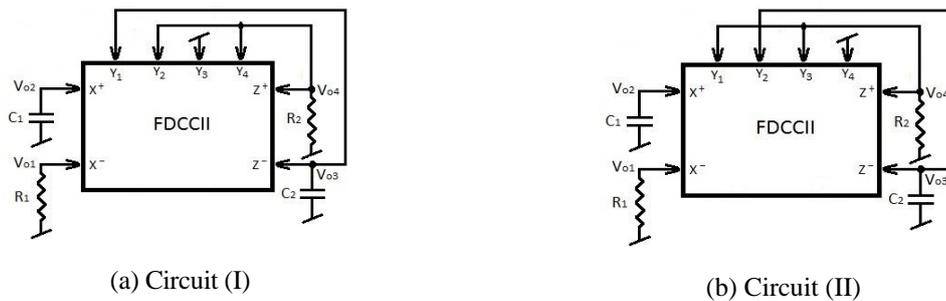


Figure 2. Proposed circuits

Routine analysis of these circuits, which provide four voltage outputs each with 45° phase difference yield the following characteristic equation:

$$s^2 C_1 C_2 + s(C_2 G_2 - C_1 G_1) + G_1 G_2 = 0 \quad (2)$$

The frequency of oscillation (FO) and the condition of oscillation (CO) can be obtained as

$$\text{CO: } C_2 G_2 \leq C_1 G_1 \quad (3)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \frac{1}{\sqrt{C_1 C_2 R_1 R_2}} \quad (4)$$

From Figure 2, under steady state and depending on the FDCC terminal characteristic equation, the currents I_{o1} (I_{R1}) and I_{o3} (I_{C2}) are equal hence the phase shift between V_{o1} and V_{o3} is 90° also the currents I_{o2} (I_{C1}) and I_{o4} (I_{R2}) are equal hence the phase shift between V_{o2} and V_{o4} is 90°, therefore the relationship between output voltages V_{o1} , V_{o2} , V_{o3} and V_{o4} are

$$\frac{V_{o1}}{V_{o3}} = (sC_2 R_1) \quad (5)$$

$$\frac{V_{o4}}{V_{o3}} = \frac{1}{2}(1 + sC_2 R_1) \quad (6)$$

$$\frac{V_{o3}}{V_{o2}} = (1 + sC_1 R_2) \quad (7)$$

Therefore at oscillating frequency, it can be easily shown that

$$V_{o1} = \sqrt{2} * V_{o4} \angle 45^\circ \quad (8)$$

$$V_{o4} = \frac{1}{\sqrt{2}} * V_{o3} \angle 45^\circ \quad (9)$$

$$V_{o3} = \sqrt{2} * V_{o2} \angle 45^\circ \quad (10)$$

It is clear from equations (8-10) that the phase difference between V_{o1} , V_{o2} , V_{o3} and V_{o4} is 45°. Figure 3 explains the phasor sequence and amplitude diagram of the output voltages.

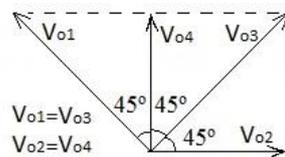


Figure 3. Phasor and voltage amplitude diagram of the proposed sinusoidal generators

Also, the phasor diagram shows two equi-quadrature voltage outputs. The first quadrature oscillator has been formed between V_{o1} and V_{o3} which their magnitude equals $\sqrt{2}$ the magnitude of the other outputs of the second quadrature oscillator represented by V_{o2} and V_{o4} . With the four voltage outputs, proposed circuits can simultaneously obtain two current output waveforms each with 45° separation by adding Z^+ and Z^- stages

incorporation in FDCCII. Getting four current output waveforms can be done by adding two voltage to current converters such as CCII converter and connect them to X⁻ and Z⁻ terminals.

3. NON IDEAL ANALYSIS

Incorporating the two sources of tracking errors into the ideal characteristic equation of the FDCCII leads to

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_{11} & -\beta_{12} & \beta_{13} & 0 \\ 0 & 0 & -\beta_{21} & \beta_{22} & 0 & \beta_{24} \\ \alpha_{01} & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_{02} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \tag{11}$$

where $\beta_v = 1 - e_v$ and $e_v (|e_v| \ll 1)$ denote the differential voltage tracking errors and $\alpha_i = 1 - e_i$ and $e_i (|e_i| \ll 1)$ denote the current tracking errors.

The non-ideal expression for the output voltages of Figure 3 is given by

$$s^2 C_1 C_2 + s \left[\frac{C_2 G_2}{\beta_{12} \alpha_1} + C_1 G_1 \left(\beta_{21} \alpha_2 - \frac{\beta_{11}}{\beta_{12}} \alpha_2 (\beta_{22} + \beta_{24}) \right) \right] + \frac{\beta_{21} \alpha_2}{\beta_{12} \alpha_1} G_1 G_2 = 0 \tag{12}$$

The FO and CO of the proposed circuits under non-ideal conditions are now found as

$$\text{CO: } C_2 G_2 \leq C_1 G_1 \alpha_1 \alpha_2 [\beta_{11} (\beta_{22} + \beta_{24}) - \beta_{12} \beta_{21}] \tag{13}$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{\beta_{21} \alpha_2 G_1 G_2}{\beta_{12} \alpha_1 C_1 C_2}} \tag{14}$$

From the above, the active and passive sensitivities of the frequency of oscillation are found as

$$S_{C_1}^{f_o} = S_{C_2}^{f_o} = S_{R_1}^{f_o} = S_{R_2}^{f_o} = S_{\alpha_1}^{f_o} = S_{\beta_{12}}^{f_o} = -\frac{1}{2}, S_{\alpha_2}^{f_o} = S_{\beta_{21}}^{f_o} = \frac{1}{2}, S_{\beta_{13}}^{f_o} = 0 \tag{15}$$

The active and passive sensitivities of the frequency of oscillation are found to be in the range $-1/2 \leq S_x^f \leq 1/2$, and the circuit, thus, enjoys low sensitivities.

4. SIMULATION RESULTS

The proposed generator circuits have been simulated to verify the theoretical analysis. The voltage mode oscillator of Figure 2(I) has been selected to verify the circuit performance. The FDCCII was realized based on the CMOS implementation from [34] as shown here in Figure 4.

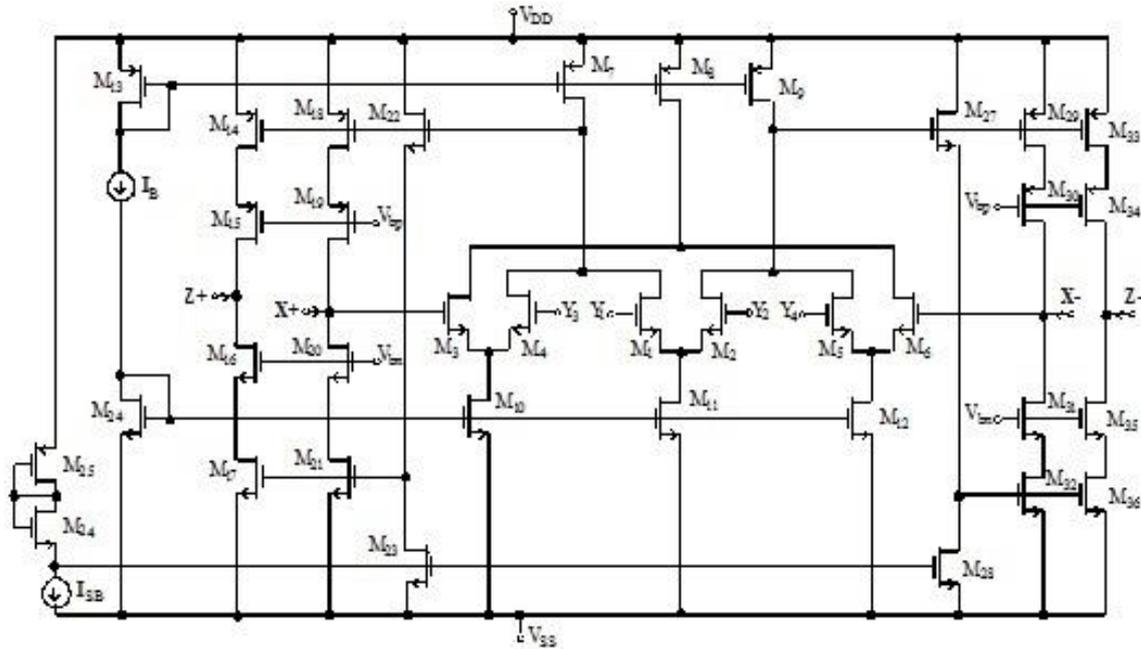


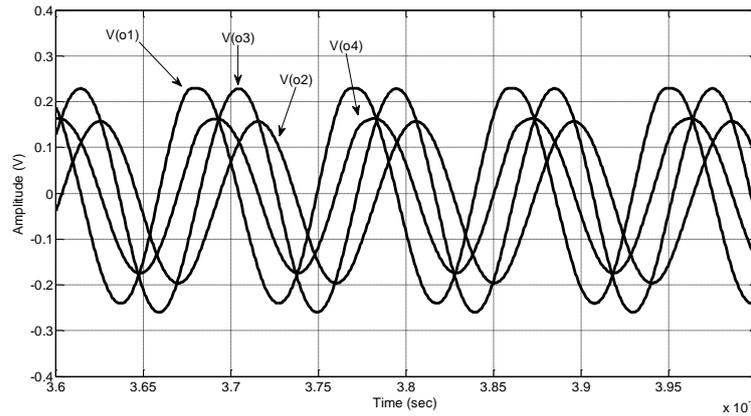
Figure 4. CMOS realization of the FDCCII [34]

PSPICE simulation based upon a CMOS FDCCII was implemented using 0.18 μm technology where the aspect ratios of the MOSFETs are shown in Table 1.

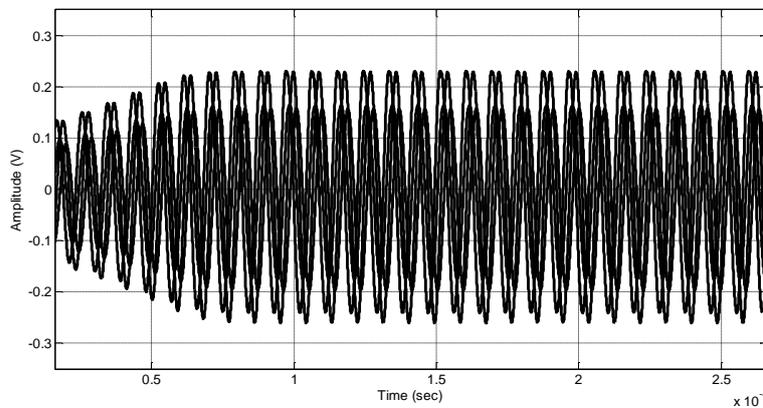
Table 1. Aspect ratios of MOSFETs

MOS transistors	W/L (μm)
M ₁ - M ₆	0.25/0.18
M ₇ , M ₈ , M ₉ , M ₁₃	0.25/0.18
M ₁₀ , M ₁₁ , M ₁₂ , M ₂₄	0.25/0.18
M ₁₄ , M ₁₅ , M ₁₈ , M ₁₉ , M ₂₅ , M ₂₉ , M ₃₀ , M ₃₃ , M ₃₄	0.5/0.18
M ₁₆ , M ₁₇ , M ₂₀ , M ₂₁ , M ₂₆ , M ₃₁ , M ₃₂ , M ₃₅ , M ₃₆	0.5/0.18
M ₂₂ , M ₂₃ , M ₂₇ , M ₂₈	0.25/0.18
M ₁₄ , M ₁₅ , M ₁₈ , M ₁₉ , M ₂₅ , M ₂₉ , M ₃₀ , M ₃₃ , M ₃₄	0.5/0.18

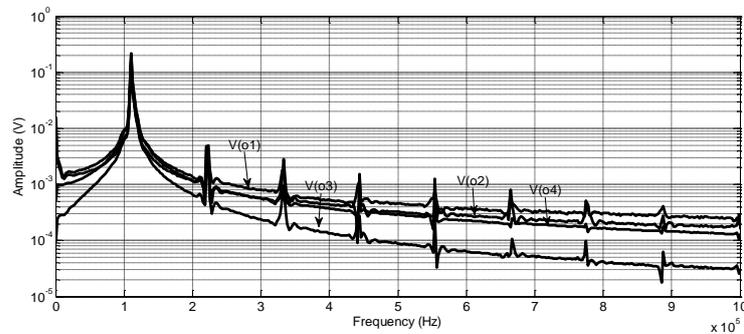
The CMOS FDCCII was biased with DC power supply voltages $V_{DD} = +1.5\text{ V}$, $V_{SS} = -1.5\text{ V}$ along with $I_B = 33\ \mu\text{A}$, $I_{SB} = 25\ \mu\text{A}$, $V_{bp} = 0.25\text{ V}$, and $V_{bn} = -0.3\text{ V}$. To achieve the oscillator with $f_o = 112\text{ kHz}$, the passive component values were chosen as $R_1 = R_2 = 20\text{ k}\Omega$, and $C_1 = C_2 = 71\text{ pF}$. Figure 5 shows the PSPICE-generated 45° phase shift voltage output waveforms of the oscillator realized from the proposed circuit, where the waveforms coincide with the phases and magnitudes of the phasor diagram shown in Figure 3. The Transient and steady state voltage output waveforms are shown in Figure 5(a) and 5(b) respectively. The frequency spectrums of these waveforms are shown in Figure 5(c). SPICE simulations frequency of generated voltage output waveforms has been found to be 111.7 kHz . The Total Harmonic Distortion (THD) of the output waveforms was $1.44 - 4.53\%$. Thus, a very good matching between theoretical values and PSPICE simulations is observed.



(a) Transient voltage output waveforms



(b) Voltage output waveforms



(c) Frequency spectrum

Figure 5. PSPICE Simulation results of the 45° phase shift Oscillator realized from the proposed circuits

The circuit has two quadrature outputs and the Lissajous patterns confirm the quadrature voltage output waveforms as shown in Figure 6.

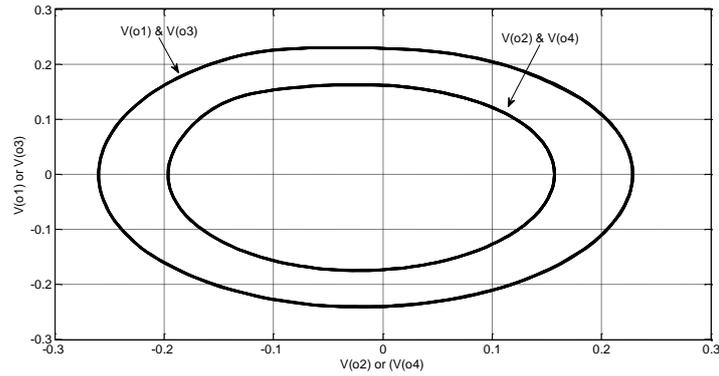


Figure 6. Lissajous patterns of quadrature voltage output waveforms (V_{o1} with V_{o3}) (V_{o2} with V_{o4})

By adding Z^+ and Z^- stages incorporation in FDCCII and two CCII converters (to change the voltage to current) connected to X^- and Z^- terminals the circuit can provide four current output waveforms each with 45° separation as shown in Figure 7.

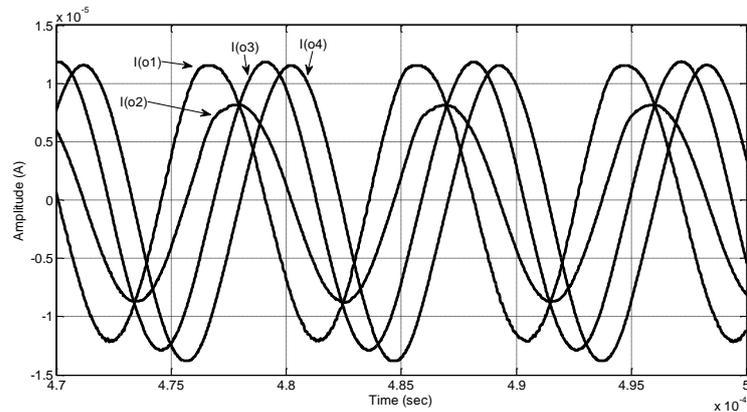


Figure 7. Current output waveforms

5. COMPARATIVE WITH OTHER WORKS

A comparison of multiphase sine-wave generator provides four 45° phase shifted voltage outputs using different active component presented recently in [30-32] (and the references cited therein) and proposed circuits are discussed below. The circuit in [30] uses single Z-copy voltage differencing transconductance amplifier (ZC-VDTA), two capacitors and three resistors. The drawback of ZC-VDTA is affected by temperature due to its transconductance. However, the circuit has more passive components. The circuit in [31] uses single Z-copy controlled gain voltage differencing current conveyor (ZC-CG-VDCC), two capacitors and two resistors. This circuit has one 45° phase shift between two voltage outputs and 90° between the other two outputs not equi-quadrature as presented in the proposed circuits which the outputs increase 45° sequentially. Also, this circuit suffers from the temperature effect due to the existence of transconductance in the internal circuit. The circuits of [30] and [31] are more complicated as compared with proposed circuits. The circuit in [32] uses the same passive component employed in the proposed circuits but it uses more active elements (two Differential Voltage Current Conveyors (DVCCs)), as well as FDCC has more current gain and bandwidth than DVCC [35] with same characteristics. Therefore the proposed circuits enjoy the simplicity and less active and passive components.

6. CONCLUSION

It is shown in this paper that two new circuits which are used single active element can generate four 45° phase separation voltage outputs. Because has the fully differential circuit which is suitable for analog

signal applications, FDCCII is used as an active element in these circuits. Also, these proposed circuit used only four passive components (two capacitors and two resistors). In addition, these circuits can achieve two voltage-mode equi-quadrature oscillators and can also provide four current output waveforms each with 45° separation by adding output stages incorporation in FDCCII and two CCII converters.

The previously reported 45° phase difference outputs oscillators in the literature may more complicate of the active circuits or more elements of the active or passive components as compared with the proposed circuits. Due to all the passive components of the proposed circuit are grounded therefore is preferred for IC fabrication. PSPICE 0.18 μm CMOS technology has been used to simulate the performance of the circuits. The simulation results are given to verify the presented theoretical analyses.

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