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Effect of Chirality and Oxide Thikness on the Performance of a Ballistic CNTFET

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Article Info	ABSTRACT
	Since the discovery of 1D nano-object, they are constantly revealing significant physical properties. In this regard, carbon nanotube (CNT) is considered as a promising candidate for application in future nanoelectronics devices like carbon nanotube field effect transistor (CNTFET). In this work, the impact of chirality and gate oxide thikness on the electrical characteristics of a CNTFET are studied. The chiralities used are (5, 0), (10, 0), (19, 0), (26, 0), and the gate oxide thikness varied from 1 to 5 nm. This work is based on a numerical simulation program based on surface potential model. CNTFET Modeling is useful for semiconductor industries for nano scale devices manufacturing. From our results we have observed that the output current increases with chirality increasing. We have also highlighted the importance of the gate oxide thickness on the drain current that increases when gate oxide is thin.

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1. INTRODUCTION

The progress in silicon technology continues to outpace the historic pace of Moore's Law, but the end of device scaling now seems to be only 10-15 years away [1]. A new alternative appears to overcome all these limitations. One of the most promising areas of research in the improvement of transistors performance is the use of carbon nanotubes (CNTs) that is considered today as the most important new materials with excellent properties [2] beyond the 11-nm technology node due to its superior electrical properties of CNTs [3] and the feasibility of using these devices to build FET transistors with geometrically excellent electrostatic control. The progress of CNTFET technology and the understanding of its device physics has been very active this last decade.

Carbon nanotubes were first discovered in 1991, and became rapidly the focus of much research activity, due to their exceptional electrical, mechanical, and thermal properties [4]. These devices, ideal elementary components for the realization of nano-devices, have the possibility of being able to be semiconductors or metal. This unique property makes the carbon nanotube an interesting candidate for the manufacture of a new electronic component based on nanotubes,such as Carbon NanoTube Field Effect Transistor called CNTFET [5]. CNTFET technology can be clubbed with bulk CMOS technology on a single chip and uses the same infrastructure allowing to provide improvements in electrostatics over CMOS technology. CNTFET transistors allow moore's Law sustaining to ensure further improvement in MOSFET performance. It is indispensable to look for an alternatives such as CNTFETs that give assurance to deliver much better performance than existing MOSFETs [6].

It is also important to recall that each new node has witnessed the integration of new materials and process steps that will achieve the objectives of the ITRS roadmap of SC industries. We quote amongo thers the integration of high-κ dielectrics that can reduces ignificantly the gate leakage. Mechanical strain applied in the channel and substrate orientation also allow carrier mobility improvement, as well as the use of alternative device geometries, such as double-gated devices. Of the several structures studied so far, CNTs have shown particular promise due to their size and unique electronic properties. Lately CNTFETs have been fabricated successfully [6].

In this paper, we have discussed the various simulation results [7] we have study the influence of chirality and gate insulator thikness on (I-V) characteristics of CNTFET, and observes the parameter changing eflect on it. Besides, further analysis has been done through the comparison of' the other group to justify result.

2. CARBON NANOTUBE

Carbon nanotubes (CNTs) have attracted extensive attention because of their unique properties [8], Carbon Nanotubes were discovered in 1991 by Sumio Iijima [9]. CNTs are made from cylindrical carbon molecules [10], CNTsowning remarkable physical properties, are large macromolecules that are unique for their size and shape. They are allotropes of carbon that are members of the fullerene structural family, which includes the spherical bucky balls. These cylinders of carbone atoms arranged on a honey-comb lattice, as a single layer of graphite and with almost the same nearest-neighbor C-C spacing that is ac-c = 1,44 A°. CNTs are, in fact made by rolling up of sheet of graphene into a cylinder. A carbon nanotube is composed of one or more graphene sheets rolled up on itself, describing a tubular geometry as shown in Figure 1. These nanostructures are constructed with length-to-diameter ratio of up to 1.32×108,their diameter is in the order of few nanometers [11]-[12]. CNTs are considered as very promising candidates in the field of nanoelectronics, such as CNT-MOSFETs devices.

Depending on the number of concentrically rolled-up graphene sheets, carbone nanotubes are classified to single-walled (SWNT), and multiwalled CNTs (MWNT), which consist of a single layer of graphene sheet wrapped up to form a seamless tube [13], as presented in Figure 1.
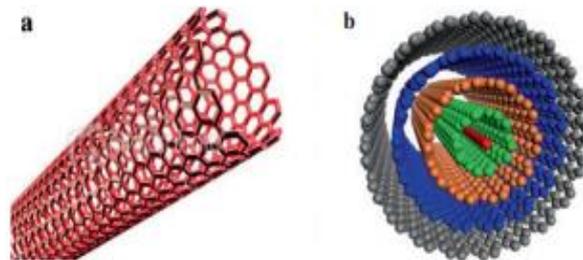

Figure 1. Basic structures of (a) single-walled, and (b) multi-walled CNTs

SWNTs, presented here, are more pliable than MWNTs and can be, flattened, twisted and bent into small circles or around sharp bends without breaking. SWNTsconsist of a single layer of graphene sheet wrapped up to form a seamless tube. The diameter andthehelicity of a SWNT are defined by the roll-up vector called chiral vector [14] given by:

$$\overrightarrow{C_h} = n\vec{a}_1 + m\,\vec{a}_2 \tag{1}$$

This roll-up vector connects crystallographically equivalent sites on this sheet, it defines the circumference on the surface of the tube connecting two equivalent carbon atoms as shown in Figure 2, a_1 and a_2 are the graphene lattice vectors.These unit vectors of the hexagonal latticecan be by [15] :

$$a_1 = (3/2a_{c-c}, \sqrt{3}/2a_{c-c}) \tag{2}$$
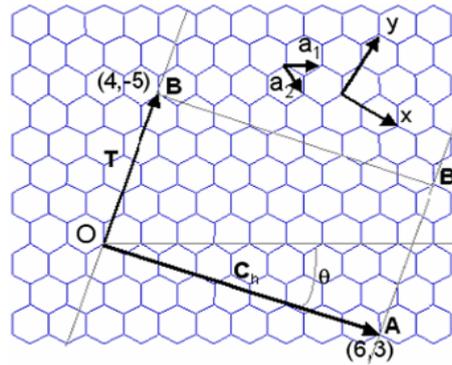
$$a_2 = (3/2a_{c-c}, \sqrt{-3}/2a_{c-c}) \tag{3}$$

Figure 2. 2D graphene sheet illustrating lattice vectors a1 and a2, and the roll-up vector [14]

n and m are integers, they determine if a SWNT will be a metal or a semiconductor. They are also called indexes also allow to determinethe chiral angle that is given by :

$$\theta = tan^{-1}\left(\frac{\sqrt{3n}}{2m+n}\right) \qquad (4)$$

The chiral angle θ is used to separate carbon nanotubes into three classes differentiated by their electronic properties: zig-zag (m = 0, n > 0, θ = 0˚), armchair (n = m, θ = 30˚), and chiral (0 < |m| < n, 0 < θ < 30˚) can see in Figure 3.
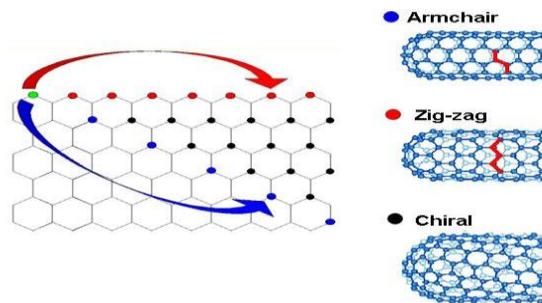

Figure 3. Examples of the three types of SWNTs identified by the integers (n, m)

Armchair carbon nanotubes are metallic. Zig-zag and chiral nanotubes can be semi-metals with a finite band gap if n – m/3 = integer and m ≠ n or semiconductors in all other cases. The band gap for the semi-metallic and semiconductor nanotubes scales in the order of the inverse of the CNT diameter giving each nanotube a distinctive electronic behavior. Each nanotube can be uniquely specified by its diameter'd' and its chiral angle θ. the diameter of the nanotube can be expressed as:

$$d = Ch/\pi = \sqrt{3}.a_{c-c}(m^2 + mn + n^2)^{1/2}/\pi] \qquad (5)$$

3.   CNTFET STRUCURE

The first CNFETs where conceived in a very easiest way, as only a proof of concept and a basic understand were the goals of these new devices.The first CNTFETs were reported in 1998.The first generation of CNTs are given in Figure 4.
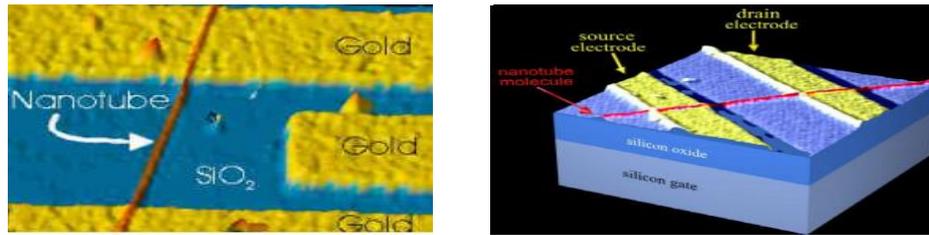
Figure 4. First generation of CNFETs [16]-[17]

CNFETs are considered as a potential candidate to replace MOSFETS beyond the 11nm technology node because of the good electrical transport properties of carbone nanotubes and also the feasibility of using CNTs to conceive CNTFETs with a very good electrostatic control [18].

These simple devices were fabricated by depositing single-wall CNTs from solution on to oxidized Silicon wafers that had been prepattemed using gold or platinum electrodes that served as source and drain electrodes connected via the nanotube channel ,and the doped Si substrate served as the device gate [19]-[20]. The operating principle of the conventional field effect transistor based on carbon nanotube is very similar to a MOSFET Transistor considering replacing the channel material to take advantage of ballistic transport in the CNTs, where electrons are supplied by source terminal and drain terminal will collect these carriers nevertheless, the arrangement keeps changing in order to improve the performance of the device.

Because of these unique fetures, CNTFETs become devices of special interest. Field effect transistors made of carbon nanotubes so far can be classified into two 2 biggest classes: back-gated CNFETs and top-gated ones [21]. Lately, a new structure has been introduced known as vertical CNFETs.

CNTFETs are also three terminals device like MOSFETs, the difference between these two field effect devices is that CNTFETs employ the CNT as a channel between its source and its drain terminals where as MOSFETs channel is made of doped Si. According to the number of layers in the channel of the CNTFETs, this device can be Single Wall (SW) or Multi Wall (MW).

 CNTFET devices have two modes of operation, the Schottky-Barrier (SB) or MOSFET-Like CNTFETs. The structure between these two CNFET is only slightly different but results in different transistor operation [22]. In the SB-CNTFETs the gate voltage modulates the current which flow in the channel by changing the width of the barrier. But in MOSFET-Like CNTFETs the gate voltage can be controlled in the drain current by changing the height of the barrier.
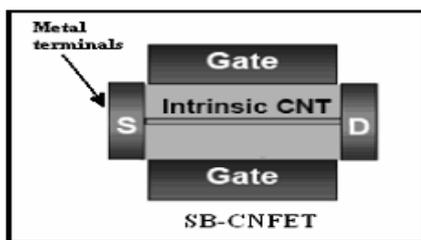

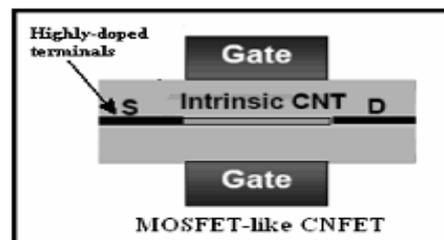Figure 5. Cross sectional view of Schottky-barrier CNFET [21]

Figure 6. Cross sectional view of MOSFET like CNTFET [21]

4.   CNTFETS SIMULATION MODEL

To investigate the chirality effects on our device DC performance, a simple two-dimension alanalytical model for ballistic CNTFET isused and shown in Figure 8. Our simulation study is carried out based on surface potential model described by Rhaman et al. This is an extension of the earlier work already done by K. Natori. This model consists of three capacitors that areattached as terminals of the device. As shown in Figure 8, a charge is placed at the top of the barrier.
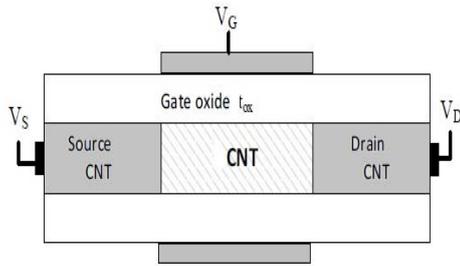
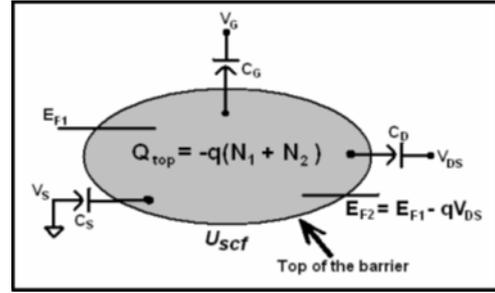Figure 7. Cross sectional view of the CNTFET type

Figure 8. 2D Capacitor model for ballistic transistor N type [23]

The top of the barrier's local density of states noted LDOS indicates the charge by the self-consistent potential. At the top of the barrier, the equilibrium electron density No is given by :

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F) dE \tag{6}$$

where $D(E)$ is the *local* density of state at the top of the barrier and $f(E - E_F)$ represents the equilibrium Fermi distribution function. The positive velocity states N_1 are occupied by the source and the negative velocity states N_2 are occupied by the drain. N_1 and N_2 and are given by [24]:

$$N_1 = \frac{D(E)}{2} \int_{+\infty}^{-\infty} f\left(E + U_{scf} - E_{F1}\right) dE \tag{7}$$

$$N_2 = \frac{D(E)}{2} \int_{+\infty}^{-\infty} f\left(E + U_{scf} - E_{F2}\right) dE \tag{8}$$

E_{F1} and E_{F2} are Fermi levels and U_{scf}. Is the self-consistent potential at the top of the barrier. The Laplace potential U_L at the top of the barrier ignoring mobile charge in given by [18]: Calculate a Laplace potential U_L:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \tag{9}$$

Where: $\alpha_G = \frac{C_G}{C_T}, \alpha_D = \frac{C_D}{C_T}, \alpha_S = \frac{C_S}{C_T}$

C_T is the parallel combination of three capacitors C_G, C_D, C_S. The potential due to mobile charge Up can be expressed by:

$$U_p = \frac{q^2}{C_T}(N_1 + N_2) - N_0 \tag{10}$$

The entire self-consistent potential U_{scf} is given by superposition of U_L and U_P potentials [18]:

$$U_{scf} = U_L + U_P \tag{11}$$

$$U_{scf} = -q(\propto_G V_G + \alpha_D V_D + \alpha_S V_S) + \frac{q^2}{C_T}(N_1 + N_2) - N_0 \tag{12}$$

$$I_D = \frac{4qk_BT}{h}\left[ln\left(1 + exp\left(E_{F1} - U_{scf}\right)\right) - ln\left(1 + exp\left(E_{F2} - U_{scf}\right)\right)\right] \tag{13}$$

k_B: is the Boltzmann constant, T: is an operating temperature, E_F: is the Fermi energy, U_{scf}: surface potential and q the charge electric field.

5. RESULTS AND DISCUSSION

To investigate the performance of scaled carbone nanotube MOSFETs, we simulated a planar CNTFET with a ballistic channel, at room temperature. The device simulated has a 10 nm SiO$_2$ gate oxide thickness. Different diameters, which results in different bandgap allowing different drain current are simulated. We explore various issues by varying two parameters that are the chirality and the oxide thickness.

5.1. Effect of chirality on the electrical device characteristics

In this section, we study the chirality effects on the CNTFETs' characteristics, knowing that the chirality (n, m) of SWNTs determines the diameter of CNT, and the CNT's energy gap. In this work SiO₂ gate insulator (k=3.9) with 10 nm thikness is used, gate and drain control are (0.88 and 0.35) respectively, the source fermi level is equal to -0.32 eVand operating temperature is 300°K. To investigate the influence of the chirality on CNTFET we have simulated four CNTFETs with different diameters and obviously different (n, m) given in Table 1.

Table1. Chirality, diameter and enegy gap

Chirality (n,m)	Diameter (nm)	Energy gap
(5,0)	3.9e-10	2.17
(10,0)	7.8e-10	1.0
(19,0)	1.5e-09	0.5
(26,0)	2.0e-09	0.4

All simulation results allowing observing chirality influence on the drain current of our device are given in Figure 10 – 13:

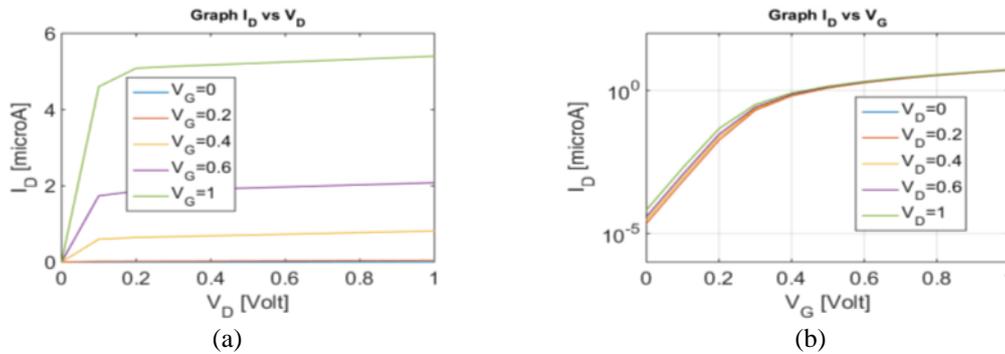(a)   (b)

Figure 9. The I-V characteristics of a (5-0) SWNT : (a) Ids –Vds (b) Ids-Vgs in logarithmic scale

(a)   (b)
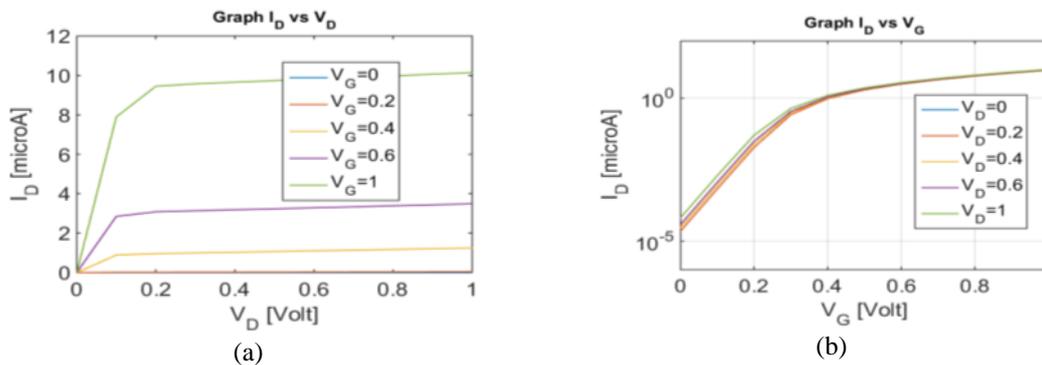
Figure 10. The I-V characteristics of a (10-0) SWNT: (a) Ids –Vds (b) Ids-Vgs in logarithmic scale

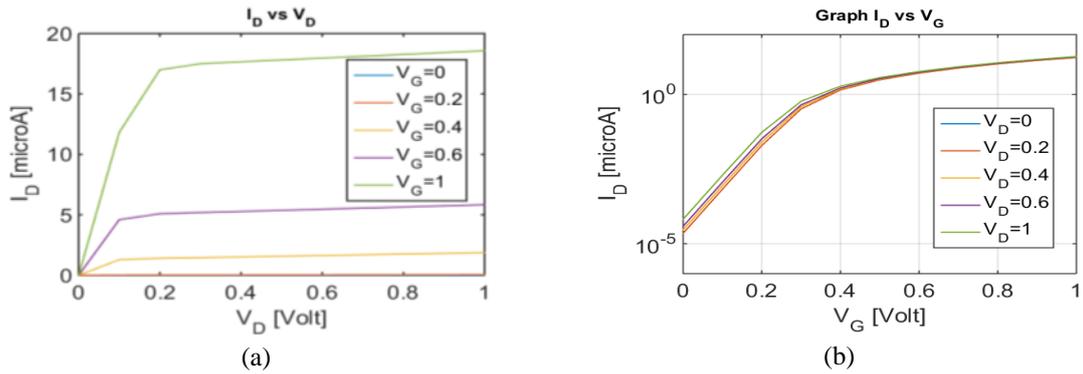Figure 11. The I-V characteristics of a (19-0) SWNT: (a) Ids –Vds (b) Ids-Vgs in logarithmic scale

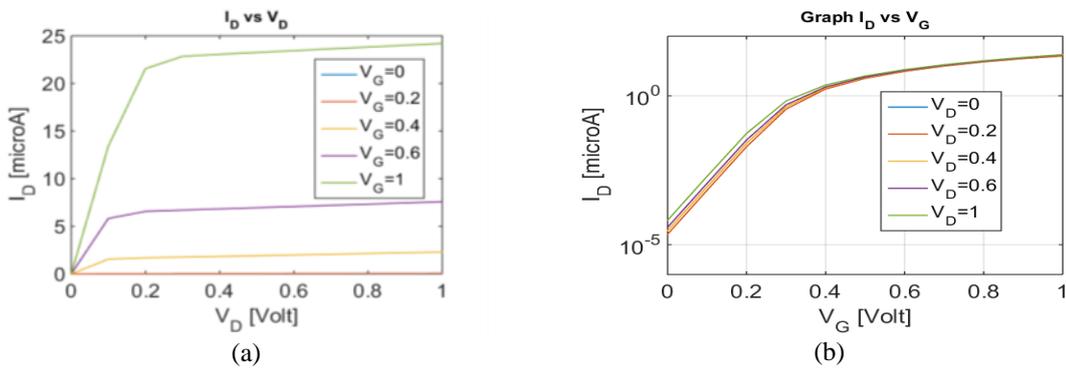Figure 12. The I-V characteristics of a (26-0) SWNT: (a) Ids –Vds (b) Ids-Vgsin logarithmic scale
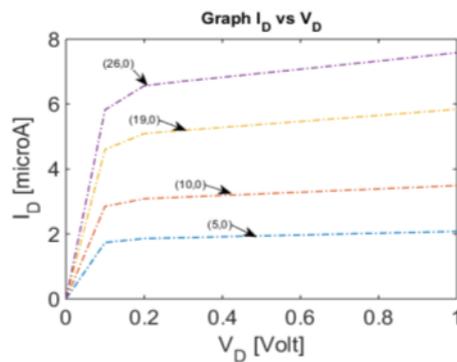

Figure 13. I_{ds}-V_{ds} characteristics of CNTFETs with chiralities of (5, 0), (10, 0), and (19, 0), (26, 0) (V_G=0.6 V)

In this part we will explore the effect of chirality, the Figure 9, 10, 11, 12(a) shows that the chirality is directly related to CNTs' diameter, and the diameter variation has a direct effect on the transistor and this is indicated in equation 5, and the gap is inversely proportional to the diameter of the carbon nanotube. The chirality has an impact on the devivce output current. Indeed, when the chirality increases the drain current increases in Figure 10, for (n,m)= (5, 0) at VG=1V , drain current of 5µA has been obtained and for (n,m)= (26, 0) a drain current of   24 µA has been obtained.It can be seen CNTFETs using carbon nanotube with larger diameter have a higher drain current, I Figure 9, 10, 11, 12(b) the curves is shown in logarithmic scale at gate voltage of 0.6 V the impact of chirality on Off current .

Table 2 gives the value for Ion and Ioff current we remark that when the chirality increase the value of Ion current increase also. The diameter on CNT has specially effect on drain current (on –current), automatically the ratio Ion/Ioff increase for (26,0) chirality.

Table 2. Value of I_{on} and I_{off} current corresponding to chirality

Chirality (n,m)	$I_{on}(\mu A)$	$I_{off}(\mu A)$	I_{on}/I_{off}
(5,0)	2	3.8×10^{-5}	0.5×10^5
(10,0)	3.5	3.8×10^{-5}	0.9×10^5
(19,0)	5.8	3.8×10^{-5}	1.5×10^5
(26,0)	7.8	3.8×10^{-5}	2×10^5

5.2. Effect of oxide thikness

In this section the impact of oxide thikness on the output characteristic of CNTFET performance is sImulated, the nanotube diameter will be fixed at 2 nm and the *t* is varied from 1-5 nm.

The Figure 14, 15, 16(a) show the drain current for differents oxide insulator in linear scale, we observe that when the gate oxide thikness is thin the conductivity increase and the leakage current is not increasing, from higher value from insulaor thikness the height of potential barrier becomes high is controlled by the gate source voltage.

The Figure 14, 15, 16(b) show the drain current for differents oxide insulator in logarithm scale we observe the influence on variance of insulator gate oxide thikness on current I_{on}, I_{ds} (I_{off}) is inchanged, we conclude when the insulator thikness is reduced the ratio I_{on}/I_{off} will increase.
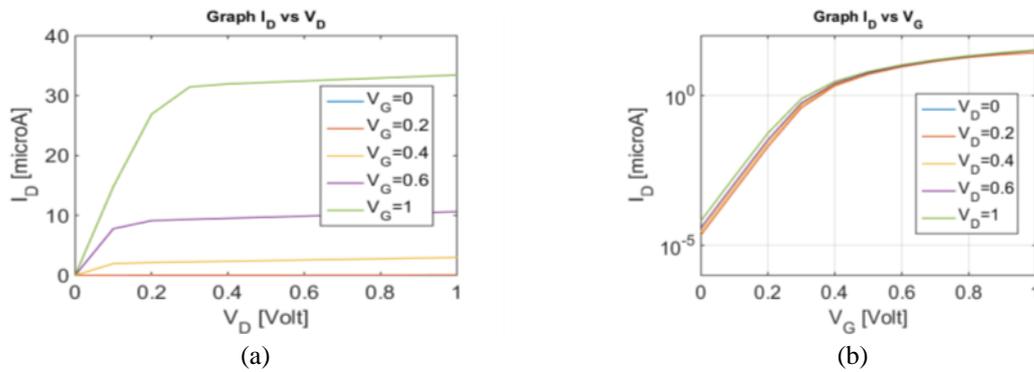

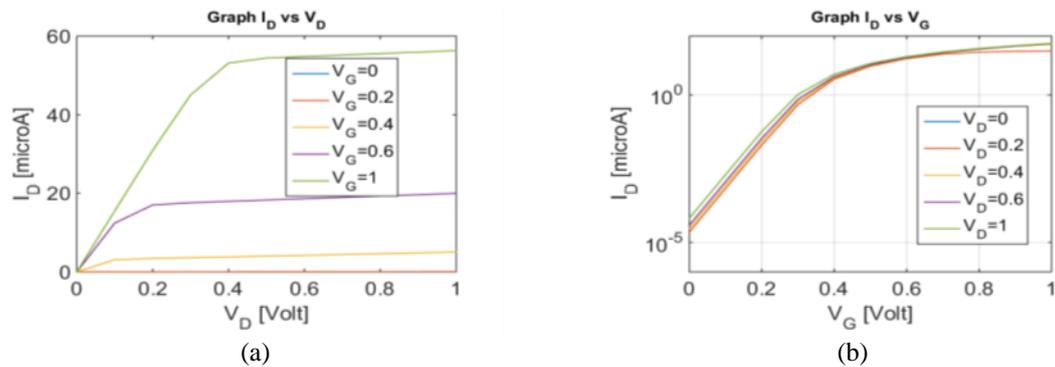Figure 14. The I-V characteristics of oxide thikness t=3nm : (a) Ids –Vds (b) Ids-Vgs in logarithmic scale

Figure 15. The I-V characteristics of oxide thikness t= 2 nm: (a) Ids –Vds (b) Ids-Vgs in logarithmic scale

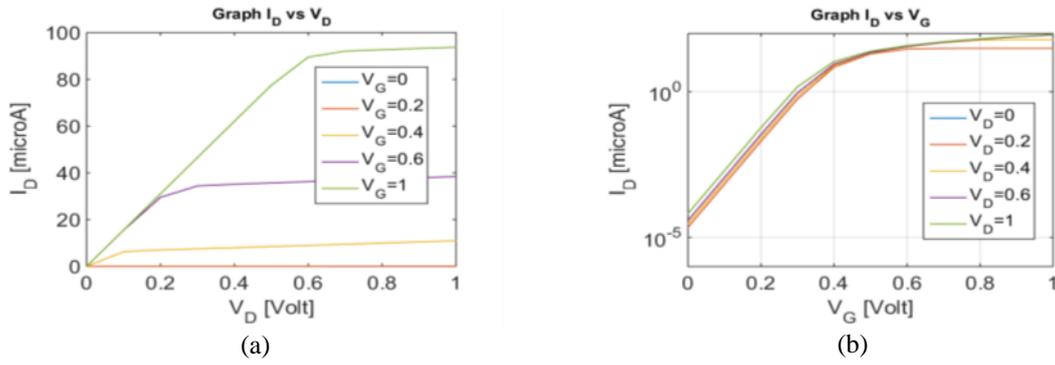(a)   (b)

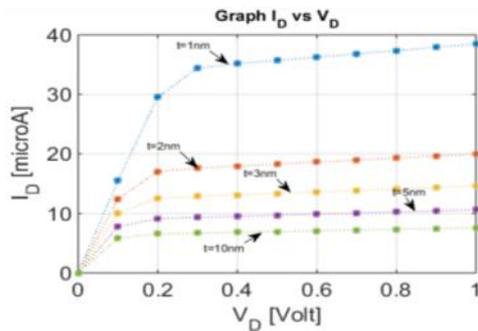Figure 16. The I-V characteristics of oxide thiknesst=1 nm: (a) Ids –Vds (b) Ids-Vgs in logarithmic scale

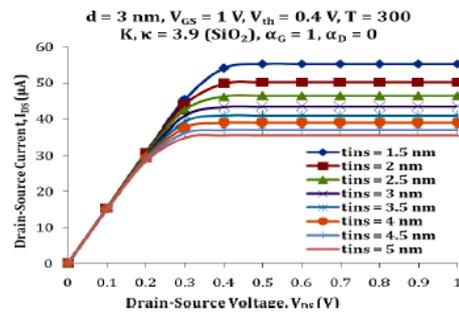Figure 17. Effetct of oxide thikness on I-V characteristics in linear scale

Figure 18. Variation of drain-source current (*IDS*) drainsource voltage (*VDS*) for various gate insulator thicknesses of CNTFET by Devi Dass, Rakesh Prasher, Rakesh Vaid, This result justifies the accuracy of our result [7]

From Table 3 we ramark that the I_{on} current is inversely propotionnel to the insulator thikness and the leakage current is not affected by the gate insulator thiknessbu the ration $I_{on}/I_{off}$is will increase when the value of gate oxide thikness is decrease. Our simulation accuracy can be justified by investigating other simulation result, the result is approximately equal compared with result in Figure 18.

Table 3. Value of I_{on} and I_{off} current for oxyde thikness

Oxyde thikness (nm)	$I_{on}(\mu A)$	$I_{off}(\mu A)$	$I_{on/Ioff}$
1	36	3.8×10^{-5}	9.4×10^5
2	18	3.8×10^{-5}	4.7×10^5
3	13	3.8×10^{-5}	3.4×10^5
5	9	3.8×10^{-5}	2.3×10^5

6.   **CONCLUSION**
        In this paper we have investigate the effect of chiraliy and gate oxide thikness on performance of CNTFET device, I have analyse in the first part the influence of chirality on the output characteristics for carbon nanotube field effect transistor. Through simulation result we have observed that when chirality increases the current value increase and the ratio I_{on}/I_{off} is proportionnel to the chirality.
        From second part we have study the impact of gate oxide thikness on drain current we can observe that the current is affected by the gate insulator thikness, the oxide thikness affects the I_{on} current but the I_{off} current remain stable. The accuracy of our result can be proved by comparing other research group work which is identical. Analysis results conclude that the CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics.

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