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Central Electric Field and Threshold Voltage in Accumulation Mode Junctionless Cylindrical Gate MOSFET

Hakkee Jung
Departement of Electronic Engineering, Kunsan National University, Republic of Korea

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ABSTRACT

Transfer characteristics is presented using analytical potential distribution of accumulation-mode junctionless cylindrical surrounding-gate (JLCSG) MOSFET, and deviation of center electric field at threshold voltage is analyzed for channel length and oxide thickness. Threshold voltages presented in this paper is good agreement with results of other compared papers, and transfer characteristics is agreed with those of two-dimensional simulation. The most important factor to determine threshold voltage is center electric field at source because the greater part of electron flows through center axis of JLCSG MOSFET. As a result of analysis for center electric field at threshold voltage, center electric field is decreased with reduction of channel length due to drain induced barrier lowering. Center electric field is increased with decrease of oxide thickness, and deviation of center electric field for channel length is significantly occurred with decrease of oxide thickness.

Corresponding Author:

Hakkee Jung,
Departement of Electronic Engineering,
Kunsan National University,
558 Daehangro, Gunsan, Chonbuk 54150, Republic of Korea.
Email: hkjung@kunsan.ac.kr

1. INTRODUCTION

Multi-gate MOSFETs are being developed with three dimensional design technology [1], [2] as a three-dimensional structure that reduces the short channel effects that occur in conventional CMOSFETs. The most successful device is FinFET. FinFETs are three-gate MOSFET devices that are designed to fabricate gates on the top and left and right sides, and are currently used for memory devices and mobile CPUs [3]. In particular, it has been shown that the short channel effect is drastically reduced by improving the controllability of carriers in a channel using three gates at 20 nm or less [4]. A device that improves the gate control capability more than the FinFET is a cylindrical MOSFET. This is a transistor structure that maximizes the controllability of the carriers in the channel by forming the gate to surround the channel by configuring the transistor into a cylindrical shape. Cylindrical MOSFETs are nanowire type, which greatly reduces the power consumption due to a sharp decrease in parasitic current, and improves the subthreshold swing characteristics, thus enabling ultra-high integration. In addition, the driving current is also sub-10 μA in the case of single-cylindrical MOSFETs, so it has been actively studied as a next-generation transistor [5-7]. In particular, when a vertical type MOSFET is manufactured, a MOSFET having a cylindrical diameter of 10 nm or less can be fabricated, which is a transistor structure enabling ultra-high integration.

As the transistor size decreases, the transistor developed to overcome the problems of the process due to the rapid doping concentration change in the source / drain doped region and the channel doped region is a junctionless transistor. In the junctionless structure, the source / drain doping type and the channel doping type are made the same and the abrupt change of doping concentration is removed. In this paper, we investigate the relationship between the threshold voltage and the center electric field for a Junctionless Cyrindrical Surrounding Gate (JLCSG) MOSFET operating in an accumulation-mode, and analyze the effect

of oxide thickness and channel length on the subthreshold characteristics. Particularly, the influence of the thickness of the oxide film due to the reduction of the channel length is observed, and the influence of the electric field generated at the central portion of the cylinder where most of the carrier transmission occurs, on the threshold voltage will be examined. To do this, we will derive the current-voltage characteristics below the threshold voltage using the diffusion-drift current equation and use this characteristic to derive the threshold voltage.

In Section 2, the current-voltage characteristics and the threshold voltage derivation process of the JLCSG MOSFET will be described. The relationship between the threshold voltage, oxide film thickness and channel length obtained in Section 3 will be explained using the center field of the JLCSG MOSFET, and On/Off characteristics of the accumulation-mode JLCSG MOSFET will be discussed. Conclusions is made in Section 4

2. ON/OFF CHARACTERISTICS AND THRESHOLD VOLTAGE OF ACCUMULATION MODE JLCSG MOSFET

Figure 1 shows the energy band diagrams of the conduction band for gate voltages at interface of the source and channel of the accumulation-mode JLCSG MOSFET when the channel length is 20 nm and the diameter of the cylinder is 10 nm and the channel doping is $10^{19}/cm^3$. In the case of the JLCSG MOSFET operating in the accumulation mode, the carrier depletion phenomenon occurs not only at the interface between gate oxide and channel but also in the channel when the gate voltage is not applied due to the work function difference between the gate metal and the channel as shown in Figure 1. In this case, when the depletion layer is formed, the transistor maintains the off state. When the gate voltage gradually increases and reaches the flat voltage of Figure 1, the depletion layer becomes the accumulation state and thransistor becomes the on state that flows the current in channel. In this paper, it can be seen in Figure 1 that the flat band voltage ($V_{FB} = \phi_m - \phi_s$) is about 0.935 V as a work function difference between the gate metal and the channel. However, the threshold voltage will become the gate voltage which is generally smaller than the flat voltage, since the current begins to flow as the channel partially begins to generate the neutral region [8]. That is, at the flat band voltage, all the channel regions are switched to the neutral region, and the on-state current will flow. At the gate voltage higher than the flat voltage, only carrier accumulation phenomenon will occur. Therefore, it will not be possible to use the extraction process of threshold voltage in the case of a general inversion-mode MOSFET. Hu et al. [9] compared the ϕ_{min} method of defining the threshold voltage as the gate voltage when the minimum potential in the channel is $-2kT/q$ [9] and the method of defining the threshold voltage as the gate voltage when the value of g_m/I_d is 1/2 of the its maximum value. However, the ϕ_{min} method assumes that the transfer charge becomes zero when the minimum potential is $-2kT/q$, and the g_m/I_d method has a over estimated problem. Therefore, in this paper, we define the threshold voltage as the gate voltage when the logarithmic change, $d^2(logI_d)/dV_g^2$, of transfer characteristics is the most severe. In order to obtain the transfer characteristics, we used the following diffusion-drift current equations of JLCSG MOSFET, which are most commonly used [10].

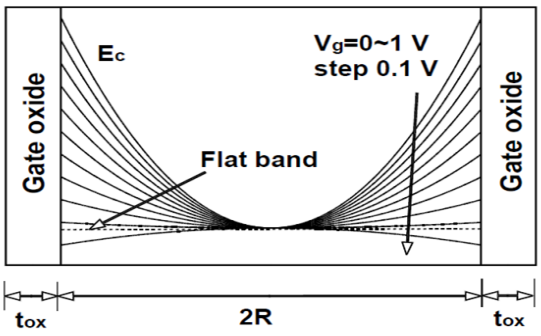

Figure 1. Schematic energy band diagram at interface of source and channel of JLCSG MOSFET

$$I_d = \frac{2\pi N_d \mu_n \left\{1 - exp\left(\frac{-qV_d}{kT}\right)\right\}}{\int_0^{Lg} \frac{1}{\int_0^R r exp\left\{\frac{q\phi(r,z)}{kT}\right\} dr} dz} \quad (1)$$

In Equation (1), the N_d is channel doping concentration, V_d is the drain voltage, the $\phi(r,z)$ potential distribution in the channel obtained using the Poisson equation for the longitudinal direction z and the radial direction r [11], L_g the channel length, R radius and k Boltzmann's constant, T the absolute temperature. Figure 2 shows the transfer characteristic curves obtained using Equation (1). As can be seen in Figure 2, Equation (1) agrees well with the two-dimensional simulation value, so we will use Equation (1) in this paper.

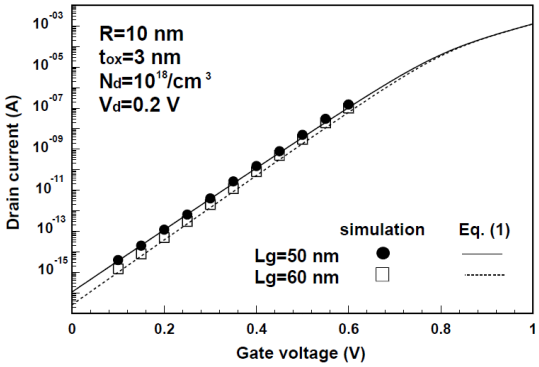

Figure 2. Comparison of transfer characteristics of gate voltage and drain current derived from Equation (1) and ATLAS-3D simulator at channel length of 50 nm and 60 nm

The $d^2(logI_d)/dV_g^2$ of the transfer characteristic curve obtained by using Equation (1) was calculated to obtain the gate voltage with the greatest variation of the drain current with respect to the gate voltage [12]. Figure 3(b) and Figure 3(c) show the comparison of g_m/I_d method and the method used in this paper. The threshold voltage is defined as the gate voltage when the secondary logarithmic derivative of the curve in Figure 3(a) is the minimum as shown in Figure 3(c). Figure 3(a) shows the threshold voltage of about 0.83 V, derived from turning point of transfer curve. Figure 3(b) shows the voltage of about 0.88 V, and the threshold voltage of this method is about 0.83 V. The threshold voltage derived from the g_m/I_d method is over-estimated to be about 0.05 V. Therefore, in this paper, we will consider the variation of the threshold voltage by the electric field and the potential energy distribution according to the oxide thickness and the channel length using the threshold voltage obtained by the method of Figure 3(c).

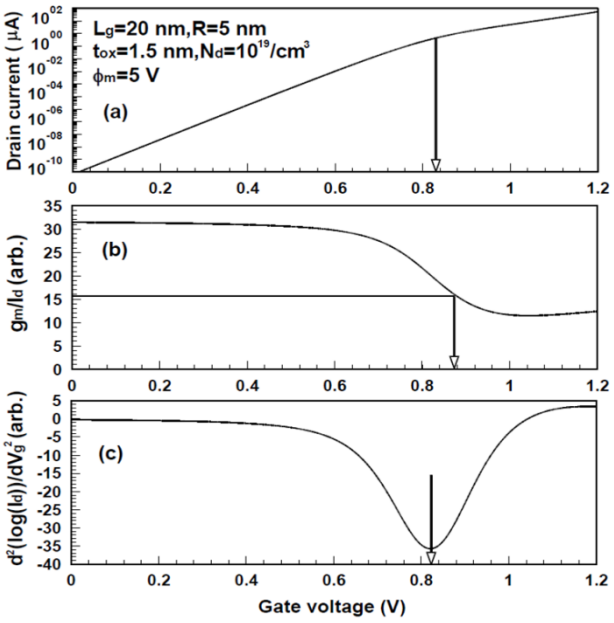

Figure 3. (a) Transfer characteristics under given conditions, (b) g_m/I_d method, and (c) $d^2(logI_d)/dV_g^2$ method

3. CENTER ELECTRIC FIELD AND POTENTIAL DISTRIBUTION AT THRESHOLD VOLTAGE IN JLCSG MOSFET

The threshold voltages derived from the ϕ_{min} method, the Hu's analytical method, and method used in this paper are compared in Figure 4, excluding overestimated g_m/I_d method. It can be seen that the method used in this paper is closer to the ϕ_{min} method. In particular, we can observe that the method used in this paper is close to the ϕ_{min} method in the region where the channel length is 20 nm or less. As described above, the threshold voltage has a value lower than the flat band voltage in the accumulation-mode JLCSG MOSFET and will show a threshold voltage that changes from fully depleted to partially depleted state. However, in accumulation mode JLCSG MOSFET, we cannot define threshold voltage as gate voltage that satisfied the condition of $\phi_s = 2\phi_f$ at interface of Si/SiO_2 like the inversion-mode MOSFET. Therefore it is analyzed how the accumulation mode JLCSG MOSFET changes from off state to on state in accordance with the oxide film thickness and channel length.

The most important potential energy distribution in the accumulation mode JLCSG MOSFET is the source-side center. Because of the nature of the JLCSG MOSFET, all electrons flow to the center of the cylinder and the center field at the source side will be the most important factor in the current flow, since the potential barrier of the source and channel regions is negligible in the JLCSG MOSFET.

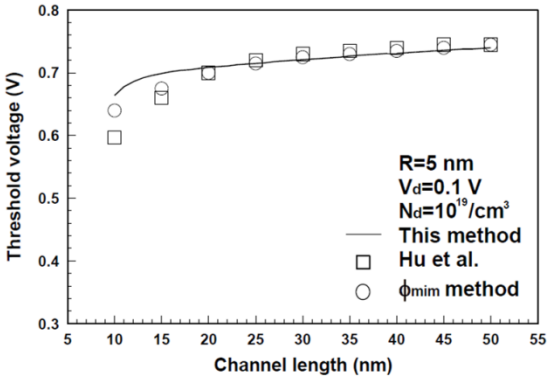

Figure 4. Comparison with threshold voltages under given conditions derived from various methods at $t_{ox} = 2\ nm$

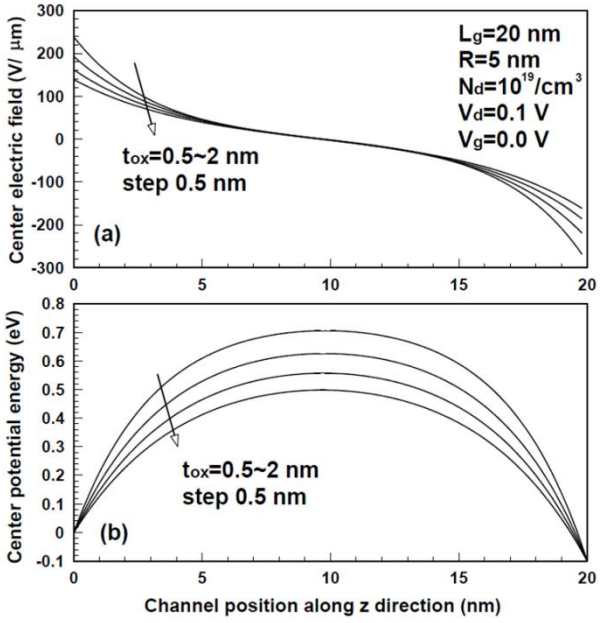

Figure 5. (a) Center electric field (b) center potential energy with gate oxide thicknesses as a parameter under given condition

In the case of $V_g = 0\,V, V_d = 0.1\,V$, the center electric field and the central potential energy change are shown in Figure 5 when the channel length is 20 nm, the radius of the cylinder is 5 nm, and the channel doping concentration is $N_d = 10^{19}/cm^3$ and the oxide thickness is changed from 0.5 nm to 2 nm. As shown in Figure 5(a), as the gate oxide thickness decreases, the center field at the source side becomes very high. Therefore, a larger gate voltage will be required as the thickness of the oxide film decreases to allow electrons to flow from the source side to the channel. That is, it can be seen that the threshold voltage increases as the oxide film thickness decreases. This phenomenon can also be observed in Figure 5(b). When the oxide film thickness is 0.5 nm, the potential energy is high and the thermionic emission current will be greatly reduced. This can predict an increase in the minimum gate voltage for the on current to flow, i.e., the threshold voltage. As the oxide thickness increases, the potential energy distribution at the central axis of the cylinder decreases, so that the on-current can be obtained even at a small gate voltage.

The channel length will be perpendicular to the surface of the wafer in the case of a vertical JLCSG MOSFET and parallel to the surface of the wafer in the horizontal case. In order to observe the change of the threshold voltage according to the channel length, Figure 6 shows a change in the potential energy distribution when the gate voltage changes from 0.6 V to 0.9 V and the channel length is controlled in the range of 10 nm to 50 nm in the case of gate oxide thickness of 2 nm. The other conditions are the same as in Figure 5. As the channel length decreases, the potential energy distribution of the source side is affected by the drain voltage due to the drain induced barrier lowering (DIBL) phenomenon. Therefore, even if the gate voltage is small, potential energy of source-side significantly reduced. This is because, as the channel length becomes smaller, electrons can flow into the channel from the source even at a low gate voltage, so that even if the center field is small, the transistor can be turned on and the threshold voltage will decrease. In particular, if the channel length is as small as about 10 nm, the threshold voltage roll-off phenomenon can be seen by the DIBL phenomenon as shown in Fig 4. However, if the channel length increases to more than 20 nm, as shown in Figure 6, since there is a potential energy barrier at a gate voltage of 0.6 V, a larger threshold voltage will be required to turn-on the transistor. In particular, as the channel length increases beyond 40 nm, the potential energy distribution is almost constant. As can be seen in Figure 4, the threshold voltage is almost the same in this region. As can be seen from the above results, it can be seen that the threshold voltage depends on the the source side center electric field of z-axis direction, that is, the horizontal electric field $E_{\|}$.

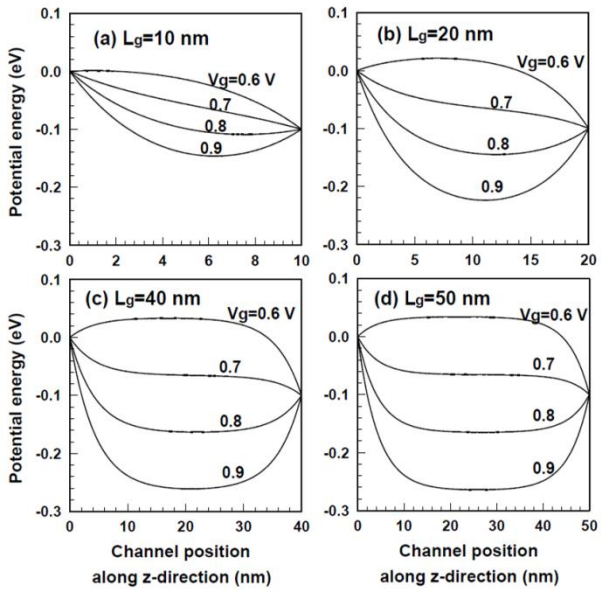

Figure 6. Potential energies for channel position along z-direction at $t_{ox} = 2\ nm$ and (a) $L_g = 10\ \ nm$ (b) $L_g = 10\ \ nm$ (c) $L_g = 10\ \ nm$ (d) $L_g = 10\ \ nm$

In order to investigate the relationship between the center electric field $E_{\|}$ and the threshold voltage in the JLCSG MOSFET, the change of the center electric field at the threshold voltage according to the variation of the gate oxide thickness and channel length is shown in Figure 7. As can be seen in Figure 7, under the condition of JLCSG MOSFET calculated, the gate voltage reaches the threshold voltage when the value of $|E_{\|}|$ is about 0 ~ 40 $V/\mu m$, and the transistor turns on. Also, as can be seen in Figure 7, as the

channel length decreases, the source side electrons move into the channel at a lower $|E_{\parallel}|$, turning the transistor on. In particular, it can be seen from Figure 7 that the rate of change for $|E_{\parallel}|$ increases greatly when the channel length increases from 10 nm to 20 nm, but decreases in channel length of 20 nm above. Compared with the results shown in Figure 6, the threshold voltage and $|E_{\parallel}|$ increase as the channel length increases. Compared with Figure 5, the threshold voltage increases as the gate oxide thickness decreases. In addition, it can be seen that as the gate oxide thickness increases, the change of $|E_{\parallel}|$ for the channel length decreases. This is because the influence of the gate voltage on $|E_{\parallel}|$ decreases as the gate oxide film thickness increases. Note that when the channel length is as small as 10 nm and the oxide film thickness decreases to 0.5 nm, then $|E_{\parallel}|$ decreases to almost zero.

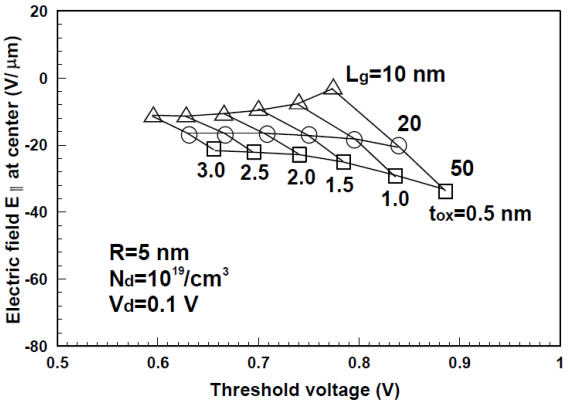

Figure 7. Center electric fields at source with channel length and oxide thickness as parameters under given conditions

4. CONCLUSIONS

In this paper, the change of threshold voltage is analyzed by the center electric field which varies with channel length and oxide film thickness, using the analytical potential distribution and the diffusion-drift current equation of accumulation-mode JLCSG MOSFET. We define the threshold voltage as the gate voltage when the change of the transfer characteristic is the greatest severe, and derive the result which is consistent with the comparison with other papers. As a result of analyzing the change of the threshold voltage according to the channel length using the change of the center electric field, the center electric field decreases as the channel length decreases. This is because electrons that can be sufficiently turned on can be introduced from the source even though the center field is low due to the DIBL effect. Also, it can be seen that as the oxide thickness decreases, the center electric field increases and the potential energy increases and the threshold voltage also increases. As a result, we can observe that the center field varies depending on the thickness of the oxide film and the channel length, which greatly affects on/off state of the accumulation-mode JLCSG MOSFET. This result will be the basis for analyzing the transfer characteristics of the accumulation-mode JLCSG MOSFET.

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BIOGRAPY OF AUTHOR

Prof. Hakkee Jung received the B.S. degree from Ajou University, Korea, in 1983, the M.S. and Ph.D. degrees from Yonsei University, Seoul, Korea, in 1985, 1990, respectively, all in electronic engineering. In 1990, he joined Kunsan National University, Chonbuk, Korea, where he is currently a Professor in department of electronic engineering. From 1995 to 1995, he held a research position with the Electronic Engineering Department, Osaka University, Osaka, Japan. From 2004 to 2005, and 2016 to 2017, he was with the School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia. His research interests include semiconductor device physics and device modeling with a strong emphasis on quantum transport and Monte Carlo simulations.