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A Survey: Space Vector PWM (SVPWM) in 3φ Voltage Source Inverter (VSI)

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ABSTRACT

Since last decades, the pulse width modulation (PWM) techniques have been an intensive research subject. Also, different kinds of methodologies have been presented on inverter switching losses, inverter output current/ voltage total harmonic distortion (THD), inverter maximum output of DC bus voltage. The Sinusoidal PWM is generally used to control the inverter output voltage and it helps to maintains drive performance. The recent years have seen digital modulation mechanisms based on theory of space vector i.e. Space vector PWM (SVPWM). The SVPWM mechanism offers the enhanced amplitude modulation indexes (MI) than sinusoidal PWM along with the reduction in the harmonics of inverter output voltage and reduced communication losses. Currently, the digital control mechanisms have got more attention than the analog counterparts, as the performance and reliability of microprocessors has increased. Most of the SVPWM mechanisms are performed by using the analog or digital circuits like microcontrollers and DSPs. From the recent study, analysis gives that use of Field Programmable Gate Arrays (FPGA) can offer more efficient and faster solutions. This paper discusses the numerous existing research aspects of FPGA realization for voltage source inverter (VSI) along with the future line of research.

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1. INTRODUCTION

The concepts of PWM are turning out to be increasingly prevalent in today's motor drives. In the inverters, PWM makes it conceivable to control both the frequency and magnitude of the current and voltage connected to a motor. Along these lines, PWM for motor drives offers better efficiency and higher performance contrasted with fixed frequency motor drives. PWM systems have been the subject of serious research amid the most recent couple of decades. The PWM techniques have been the intensive research subject. Also, different kinds of methodologies have been presented on inverter switching losses, inverter output current/ voltage THD, inverter maximum output voltage of DC bus voltage [1].

The sinusoidal PWM is utilized to control the output current/voltage of the inverter and keeps up a better performance of the drive in the whole operational range between 0-78percent of the value that would be come to by square operation. In the event that the MIs surpass this value, straight relationship amongst MI and output voltage is not kept up, and the over modulation techniques are required. As of late, a characteristically advanced modulation system known as SVPWM which depends on space vector hypothesis [2]. It has been accounted for that SVPWM mechanisms offers better performance over different methods regarding torque ripple, better DC link utilization, lower THD, switching loss and easier digital system

implementation [3]. The SVPWM systems have been rapidly used, as it allows reducing commutation losses and obtaining higher amplitude MIs if compared with Sinusoidal PWM techniques [4]. Currently, the digital control mechanisms have got more attention than the analog counterparts, as the increased performance and reliability of microprocessors [5]. Most of the SVPWM mechanisms are performed by using the analog or digital circuits like microcontrollers and DSPs [6], [7].

The utilization of FPGA gives more faster and efficient solution, as it can complete parallel processing by hardware mode which involves nothing of CPU, the framework can get a fast level [8]. The field programmable capacity of FPGA's, and the adaptable modification of dead time, the adaptable modification of dead time exchanging frequency makes it reasonable to drive different switching devices in down to earth applications [9].

The SVPWM includes complex computations. In the work of [10] and [11] digital signal processors was utilized to play out the number juggling counts. For this situation, least two processors are needed for implementation of the technique. The every count of processors are done offline and put away in memory. Despite the fact that memory space is vast contrasted with past techniques, it takes least getting to time. It doesn't influence the speed of operation. Memory is additionally modified in FPGA itself and so no need of outside memory. Moreover, there are many preferences because of the fast outline process and re-programmable capacities for FPGA [12]. The FPGA empowers to deliver model pro type logic in a less period. It is conceivable to make, actualize, and perform verification of the new design.

This paper is organized as Section 2 mentions conceptual description of voltage source inverter (VSI), 3φ VSI, space vector PWM (SVPWM), significance of SVPWM, Xilinx FPGA flow, etc. In section 3 existing researches are discussed with their significances. Section 4 states the research gap while Section 5 provides the future line of research in SVPWM. Section 6 gives the conclusion.

2. VOLTAGE SOURCE INVERTER (VSI)

The smallest circuit which used to convert direct-current (DC)-to-alternating-current (AC) is known as the inverter. The battery power is converted into AC power or main voltages and this power used for different electronic appliances such as mobiles, television, computer, etc. The main functionality of inverter is to convert DC to AC (DC-AC), and a step-up transformer is implemented to generate main voltages from AC.

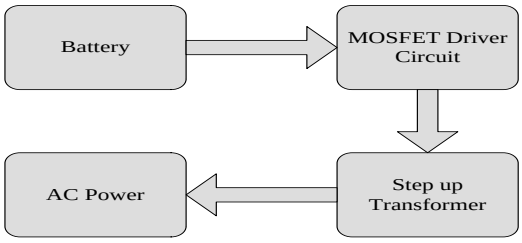

Figure 1. Inverter Block Diagram

In above inverter block diagram, battery supply is fed to MOSFET driver in which DC to AC conversion may take place, and the resulting AC is fed to step up transformer to get original voltage. Inverters can be classified as:

a. If the DC voltage is constant and this inverter is known as Voltage Source/ voltage fed Inverter.
b. If input current is kept constant and is known as Current Source or Current Fed.

2.1. Voltage Source Inverter (VSI)

a. This takes fixed voltage as input from a device and gives AC supply with variable-frequency. The VSI are classified as Square-wave Inverters, 1φ Inverters with Voltage Cancellation, Pulse-width Modulated (PWM) Inverters.
b. Square-wave inverters (SWI): In this input is connected to controlled dc voltage to control the output AC voltage magnitude. The inverter only controls the output frequency with controlled input voltage magnitude. The output voltage has square wave type.

c. Pulse-width modulation (PWM) inverters: This takes constant dc voltage as input, where diode-rectifiers are utilized for line voltage rectification and inverter should control the frequency and magnitude of the AC output voltages. There are different methods to perform the PWM in an inverter to shape output AC voltages to make a sine wave.
d. 1φ Inverters: In this voltage, cancellation is considered as constant dc source and an output square-wave. The output controls both frequency and magnitude but does not use PWM.
e. Switch-mode dc-to-ac (SM dc-ac) inverters: These are utilized for Uninterrupted power supply (UPS) in which a sinusoidal ac output is needed to be provided with controlled frequency and magnitude.

2.2. 3φ VSI

The 3φ VSI creates less harmonic distortion at output voltage used in the phase to phase AC load. A 3φ VSI circuit model is shown in Figure 2, along with six different switch ((TC+ and TC-, TB+ and TB-, or TA+ and TA-)). These switches in 3φ VSI can't be switched on all the while at grounds this may give a short circuit over the voltage supply of dc link. Thus, to move from undefined states in the VSI, the switches of any inverter leg can't be switched off all the while as this will bring about voltages that will rely on the separate polarity of line current.

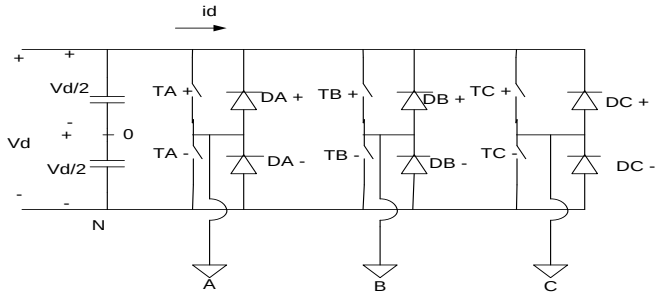

Figure 2. Circuit of 3φ VSI

Numerous applications that require an inverter utilizes 3φ control. Two main cases are AC-motor drive and UPS [3]. This can be obtained by three legs, one of every phase. The inverter output voltage can be balanced. The most cases PWM control utilized within an inverter. The upsides of PWM techniques are specified as:

a. The control of output voltage with PWM can be obtained with fewer components.
b. With the controlling of the output voltage, lower order harmonics can be minimized or erased. PWM inverters are more utilized for industrial applications [4].

2.3. Space-Vector-Pulse-Width-Modulation (SVPWM)

The power circuit topology of a 3φ VSI supplying a star connected 3φ load is given in Figure 1. The circuit consists of six semiconductor switches like IGBTs, MOSFETs, etc., along with anti-parallel diodes are used for protection purpose. The one leg two power switches are used at small dead band among two devices switching. The inverter switching gives eight output-vectors with six being active $V_1, V_2, V_3, V_4, V_5 \, and \, V_6$ or non-zero and two zero-vectors V_0, V_7. The converted diagram of voltage vectors into two axes represented in Figure 2. The non-zero vectors tips are cornered to form a regular hexagon consisting of two zero vectors joining at the origin.

Space vector theory represents the 3φ voltages as voltage space vector rotates in the (d-q) plane. The vector magnitude is related to phase voltages magnitude and the time to cover one revolution is the period of fundamental phase voltages. The inverter power switches are used to obtain voltage vectors according to different switching positions. These voltage vectors represent active vectors that subdivide the plane into equal sectors, and non-active vectors, sometimes call zero vector at an origin. The desired three-phase sinusoidal output voltages correspond to a circle in the (d-q) given in Figure 3.

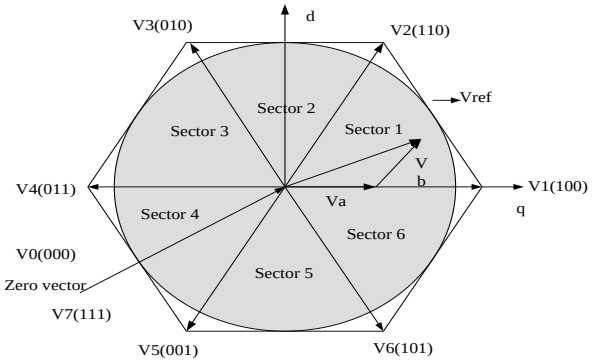

Figure 3. Voltage-vectors in d-q plane

The output line and phase voltages for each space vector are shown in Table 1. The 2φ components can be calculated by using the Equation (1).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (1)$$

Table 1. 3φ Inverter Output Voltages

Voltage vectors	Switching vectors			Line to neutral voltage			Line to Line Voltage		
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

2.4. Role of FPGA over SVPWM

Recently some control systems have been considered to deign using FPGA; FPGA integrated circuit. Implementation of SVPWM by using FPGA has been studied by a few researchers; a novel space SVPWM algorithm for multilevel multiphase voltage source converters is presented in [1]. In work of [3], an efficient SVPWM algorithm is discussed to reduce the resource usage, which evolves reduction in computational overheads and also removes the high sampling time issues for real-time applications.

2.5. Xilinx FPGA Design flow

The FPGA design methodologies include VHDL or Verilog languages, synthesis, map, and place and route scheme. The considerations are pin-pin delays, pipelining and logic levels, and floor planning, etc. FPGAs are now posses logic capacity and sufficient performance to implement a number of DSP algorithms effectively. This is achieved with exploiting parallelism and also by mapping mechanism like distributed arithmetic. At present, a single FPGA platform can replace for multiple applications, including controllers, filters, and interfaces. Efficient FPGA circuits obtained by design techniques, which traditionally relies on the processor hardware together with smart compiler technology. The block diagram for FPGA design flow is as shown in Figure 4. The FPGA design flow is consists of the following stages.

a. Design Entry - In this stage of the hardware description language (HDL), design flow is used for text-based entry, a schematic editor, or both is used to create the design.

b. Design Implementation- Using the design in Xilinx architecture, logic design file format is generated at a stage of design entry is converted to a physical file format. This physical information is existed at native circuit description (NCD) file to use FPGAs. Then a bit stream file is created.
c. Verification of Design- By using Xilinx XChecker cable, gate level simulator or JTAG cable, to ensure that the design meets the timing requirements and functions properly.

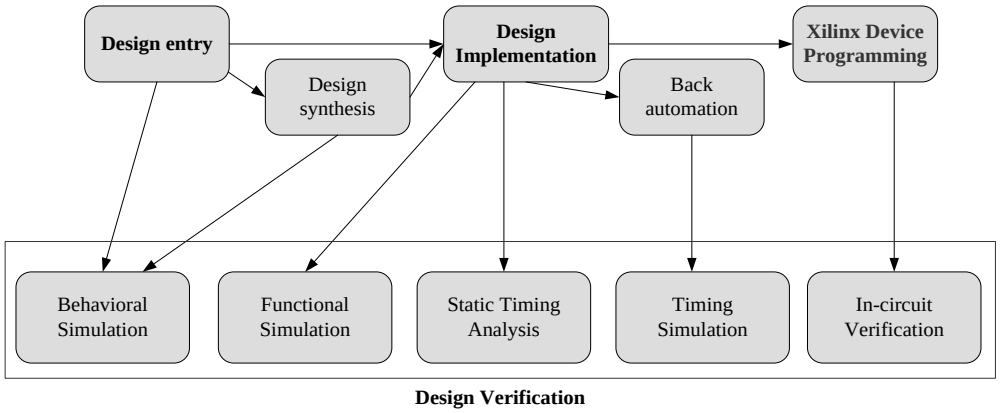

Figure 4. Xilinx flow Design

3. EXISTING RESEARCH

The existing researches in the field of VSI are surveyed and discussed in this section. The survey is categorized as realization with the FPGA and without FPGA, where the researches performed in both the techniques are discussed.

3.1. Researches on SVPWM without FPGA

The works of Shao et al. [13] have given a generalized concept of Discontinuous SVPWM (DSVPWM) for 3φ VSI. The methods consist of six sectors like DSVPWMP, DSVPWMPN0, DSVPWMN, DSVPWMPN1, DSVPWMPN2, and DSVPWMPN3 and are re-divided into twelve 1's based on local over modulation and SVPWM method. The principle of DSVPWMx is developed, and the traditional discontinuous pulse width modulation (DPWM) strategies are studied on the basis of THD and switching loss. The results state DSVPWMx strategies are feasible.

In Badran et al. [14] Digital Implementation of SVPWM Technique Using 8-bit Microcontroller is presented. Authors study is meant to develop a novel inverter design. In this, a 8-bit microcontroller is utilized to generate SVPWM signal needed for triggering the MOSFET bridge gates of the inverter. Here the inverter composed of a low-pass LC-filter to generate the output of sine waveform. In this microcontroller was used for implementation of SVPWM algorithm. Six pins of Port B of the microcontroller were used to send the output pulses. The software that was used for PIC microcontroller programming was MikroC compiler, while WinPIC800. The experimental outcome represents the effectiveness of the system to generate a 3φ sine wave at the better frequency.

The work of Boudouda et al. [15] provided combined random SVPWM using induction motor for variable speed drive. This research work focused on implementing Random space vector modulation. The analysis of the output voltage based on the PSD of random signals clearly shows the obtained spreading of the PSD and the important reduction of the peaks, compared to other simple and dual random techniques and to the conventional deterministic technique, which is the sought EMC advantage. The author method provides the good PSD performance.

Author Choudhari et al. [16] have given the SVPWM on DSP Platform for Utility Grid Synchronizable Tieline Converter between AC-bus and DC-bus of aMicrogrid. The study aims to develop Space vector pulse width modulation on DSP. In this, the PWM modules architecture based on DSP is explained. The presented inverter is simulated using existing microgrid architecture scenarios are discussed.

The design and implementation of SVPWM inverter based on cost effective microcontroller were presented in Gaballah [17]. The study was intended to develop a modulation technique with less THD, wider linear modulation range, and fewer switching losses. The practical outcomes give that the better performance at faster computation time along with less complexity in software implementation is achieved with presented SVPWM than traditional SVPWM.

The combined work of Kassas and Ahmed [18] states the simulation and implementation of SVPWM using the look-up table.This work is meant to use Loop up the table for designing SVPWM. From this SVPWM a Simulink model was introduced to verify the lookup table scheme (LTS) viability and its practical assumptions. The performance was compared among practical and simulated LTS results. The LTS shows the nearest THD to simulation results.

The combined work was performed by Kumar and Singh [19] states the DSP Based IFO Control of HEV fed through Impedance Source Inverter. The intention of the work is to achieve the good performances of speed control of the electric vehicle (induction motor) fed Z-source inverter using DSP controller. This method employs 3φ six sinusoidal reference signals, and one triangular wave of high frequency as carrier signals. In this project, impedance source-inverter with IFOC system will be designed with a single DSP controller using the TMS320F28335, a new kind of DSP chip of Texas Instrument (TI). The reason to use this one is that the integrated and flexible features in the device meet the requirements we need for a control system. The hybrid indirect field oriented controlled induction motor drives speed control with is verified with simulation. The speed control on induction motor is controlled even input DC source voltage changes.

Author Kumar et al. [20] presented the digital control of SVPWM based on shunt active filter. The THD measured a show that using the proposed topology provides better compensation of harmonics and the implementation can be done by TMS320F28027 processor.

Mirazimi et al. [21] presented the SVPWM for Two-Phase Three-Leg Inverters. The study meant to develop a novel SVPWM. This proposed control scheme allows independent control of the magnitude and quadrature phase angle for two output phases. Thus, the presented two-phase inverter and its modulation scheme make the two-phase inverter commensurate with both balanced and unbalanced two-phase loads. Simulation results by using MATLAB/SIMULINK reconfirm the feasibility of the structure based on SVPWM method for the inverter.

Piao and Hung [22] presented a control strategy for balancing dc-link capacitor voltage in multi-level diode clamped VSI based on discontinuous SVPWM. The theoretical analysis and simulation results suggest that the proposed strategy is feasible.

Promkhun and Kinnares [23] have given Speed Control of an Asymmetrical Type Two-Phase Induction Motor Using DiscontinuousSpace Vector Pulse Width Modulation. The proposed DSVPWM can reduce switching losses of the motor side inverter. Single-phase full bridge switched-mode converter is used to improve power quality and allow regenerative power to grid. This system is simulated by MATLAB/Simulink. The results of the motor side show quick response and good performance for the two-phase induction motor control in both steady and dynamic responses.

Sun et al. [24] have presented the 3φ dual Buck Inverter based on unified PWMs. The work aims to design three-phase four leg inverter based on dual-buck power cell. The Efficiency measurement of PWMs is conducted, and the inverter achieves 98.8% of peak efficiency.

3.2. Research on VSI with FPGA

Author Castro et al. [25] have given the variable-clock-phase shifting based high-resolution FPGA Digital PWM. The current FPGA exhibit above feature thus allows small and introduces programmable delays between input and output clocks. The experimental outcome gives a 19.5ps time resolution using Virtex-5 FPGA.

The work of Orithi and Julian [26] have expressed the 3φ VSI with FPGA-based multi-sampled SVPWM. The modulator and the inverter controller are used using an FPGA platform, and bandwidth is increased with respect to a digital signal processor (DSP) or with the microprocessor controller. This bandwidth results from low output voltage THD. The experimental results are represented by state space model of a VSI with an output LC filter.

Pan et al. [27] illustrated a shifted SVPWM mechanism for controlling the DC-Link Resonant Inverters FPGA Realization. The mechanism exhibit same effective vectors. A shifted SVPWM mechanism for dc-link inverters results show that the method is feasible for shifted SVPWM mechanism.

A concept to attain FPGA realization was performed by Rajendran et al. [28] using FPGA. In this FPGA is employed to realize PWM strategies and meets the high-switching-frequency and reconfigurable-structure issues for various applications. The realization and analysis of SVPWM were performed under variable-speed-control of ac motor drives by using Xilinx. The complete execution time of SVPWM direct torque controller achieved was 3.5μs.

Rohit et al. [29] an FPGA Implementation of SVPWM mechanism for 3φ Induction Motor using a Fixed Point Realization. The design a high performance and low powered VHDL based SVPWM controller for 3φ Induction Motor drive on FPGA. The SVPWM technique is an important PWM generation mechanism for 3φ VSI to generate PWM signals to control different AC Motors. In this work the software part is implemented with proposed fixed point realization which increases the accuracy; also since there are

no subroutines, it reduces the total area on FPGA board. The density of the code is less, which reduces execution time and power consumption. The effectiveness of the method was analyzed with integer realization.

Rashidi and Sabahi [30] have expressed the high-Performance FPGA-Based Digital SVPWM (DSVPWM) 3φ VSI. The study aims to design a high performance based low power DSVPWM controller using FPGA for 3φ VSI. This method is proposed to accurate and high performance based DSVPWM technique of FPGA with fewer resources and minimum execution time. The authors DSVPWM algorithm was synthesized to implement over FPGA. In this controller's total power consumption is minimized at the clock frequency of 100MHz.

The work performed by Renukadevi and Rajambal [31] gives FPGA implementation of SVPWM technique for five-phase VSI. The SVPWM algorithm was presented as the high speed circuit for hardware coding and used over XILINX FPGA processor. The relationship of SVPWM with large, medium, and the combinations of both space vectors for five-phase VSI is analyzed. The experiment is performed over 1-hp 5φ induction motor under different SVPWM mechanisms. Later, the prominent SVPWM is identified with THD and output voltage.

Guzman et al. [32] have expressed the mechanism of load sharing in AC Micro-grids by using FPGA. This is based on frequency-locked-loop (FLL) and adaptive-linear-neuron (ADALINE). The experimental outcome mentions that the each VSI-control is used by implementing FPGA in micro-grid for proposition validity.

4. RESEARCH GAP

The analysis outcome of the existing and recent researches idealizes that the realization mechanisms for VSI using various PWM mechanisms are more but failed to provide better performance and low hardware compatibility. The technique called SVPWM mechanisms offers better performance over different methods regarding torque ripple, better DC link utilization, lower THD, switching loss and easier digital system implementation. The SVPWM systems have been rapidly used, as it allows reducing commutation losses and output voltage harmonics, and obtaining higher amplitude MIs if compared with Sinusoidal PWM techniques. Currently, the digital control mechanisms have got more attention than the analog counterparts, as the increased performance and reliability of microprocessors. Most of the SVPWM mechanisms are performed by using the analog or digital circuits like microcontrollers and DSP. The studies which performed using digital mechanisms are rare and need a futuristic research towards the SVPWM using digital methods.

5. CONCLUSION

In this paper, the various aspects of the SVPWM in VSI are discussed. The SVPWM based mechanism offers the enhanced amplitude modulation indexes (MI) than sinusoidal PWM along with harmonics reduction and reduced communication losses. The existing SVPWM mechanisms are performed by the analog or digital circuits and FPGA. The FPGA SVPWM can offer more efficient and faster solution to tackle inverter related issues by functioning as analog and digital circuit and through which better realization can be achieved. This paper gives a prominent research survey in the SVPWM for 3φ voltage source inverter (VSI) that includes the concept of VSI, SVPWM. The research survey represents the most recent researches in SVPWM and highlights the existing unresolved/research gap.

Also, the future line of researches for better realization of FPGA is described along with the order of future research. The future research can be followed with the following steps:-

a. Perform the survey of existing researches for VSI, FPGA realization, and SVPWM techniques.
b. Formulate the existing issues in the existing researches
c. Design an FPGA-based system for realization of SVPWM in VSI.
d. Perform the performance analysis of the system and compare with the other techniques

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