Effect of Chirality and Oxide Thickness on the Performance of a Ballistic CNTFET

Asma Laribi, Ahlam Guen Bouazza
Unit of Research Materials and Renewable Energies, Department of Electronics, Faculty of Technology, University Abou-Bakr Belkaid, Algeria

ABSTRACT
Since the discovery of 1D nano-object, they are constantly revealing significant physical properties. In this regard, carbon nanotube (CNT) is considered as a promising candidate for application in future nanoelectronics devices like carbon nanotube field effect transistor (CNTFET). In this work, the impact of chirality and gate oxide thickness on the electrical characteristics of a CNTFET are studied. The chiralities used are (5, 0), (10, 0), (19, 0), (26, 0), and the gate oxide thickness varied from 1 to 5 nm. This work is based on a numerical simulation program based on surface potential model. CNTFET Modeling is useful for semiconductor industries for nano scale devices manufacturing. From our results we have observed that the output current increases with chirality increasing. We have also highlighted the importance of the gate oxide thickness on the drain current that increases when gate oxide is thin.

1. INTRODUCTION
The progress in silicon technology continues to outpace the historic pace of Moore's Law, but the end of device scaling now seems to be only 10-15 years away [1]. A new alternative appears to overcome all these limitations. One of the most promising areas of research in the improvement of transistors performance is the use of carbon nanotubes (CNTs) that is considered today as the most important new materials with excellent properties [2] beyond the 11-nm technology node due to its superior electrical properties of CNTs [3] and the feasibility of using these devices to build FET transistors with geometrically excellent electrostatic control. The progress of CNTFET technology and the understanding of its device physics has been very active this last decade.

Carbon nanotubes were first discovered in 1991, and became rapidly the focus of much research activity, due to their exceptional electrical, mechanical, and thermal properties [4]. These devices, ideal elementary components for the realization of nano-devices, have the possibility of being able to be semiconductors or metal. This unique property makes the carbon nanotube an interesting candidate for the manufacture of a new electronic component based on nanotubes, such as Carbon NanoTube Field Effect Transistor called CNTFET [5]. CNTFET technology can clubbed with bulk CMOS technology on a single chip and uses the same infrastructure allowing to provide improvements in electrostatics over CMOS technology. CNTFET transistors allow moore’s Law sustaining to ensure further improvement in MOSFET performance. It is indispensable to look for alternatives such as CNTFETs that give assurance to deliver much better performance than existing MOSFETs [6].
It is also important to recall that each new node has witnessed the integration of new materials and process steps that will achieve the objectives of the ITRS roadmap of SC industries. We quote among other the integration of high-κ dielectrics that can reduces significantly the gate leakage. Mechanical strain applied in the channel and substrate orientation also allow carrier mobility improvement, as well as the use of alternative device geometries, such as double-gated devices. Of the several structures studied so far, CNTs have shown particular promise due to their size and unique electronic properties. Lately CNTFETs have been fabricated successfully [6].

In this paper, we have discussed the various simulation results [7] we have study the influence of chirality and gate insulator thickness on (I-V) characteristics of CNTFET, and observes the parameter changing effect on it. Besides, further analysis has been done through the comparison of the other group to justify result.

2. CARBON NANOTUBE

Carbon nanotubes (CNTs) have attracted extensive attention because of their unique properties [8], Carbon Nanotubes were discovered in 1991 by Sumio Iijima [9]. CNTs are made from cylindrical carbon molecules [10]. CNTs owning remarkable physical properties, are large macromolecules that are unique for their size and shape. They are allotropes of carbon that are members of the fullerene structural family, which includes the spherical bucky balls. These cylinders of carbon atoms arranged on a honeycomb lattice, as a single layer of graphite and with almost the same nearest-neighbor C-C spacing that is ac-c = 1.44 Å. CNTs are, in fact, made by rolling up of sheet of graphene into a cylinder. A carbon nanotube is composed of one or more graphene sheets rolled up on itself, describing a tubular geometry as shown in Figure 1. These nanostructures are constructed with length-to-diameter ratio of up to 1.32 × 108, their diameter is in the order of few nanometers [11]-[12]. CNTs are considered as very promising candidates in the field of nanoelectronics, such as CNT-MOSFETs devices.

Depending on the number of concentrically rolled-up graphene sheets, carbon nanotubes are classified to single-walled (SWNT), and multiwalled CNTs (MWNT), which consist of a single layer of graphene sheet wrapped up to form a seamless tube [13], as presented in Figure 1.

![Figure 1. Basic structures of (a) single-walled, and (b) multi-walled CNTs](image)

SWNTs, presented here, are more pliable than MWNTs and can be, flattened, twisted and bent into small circles or around sharp bends without breaking. SWNTs consist of a single layer of graphene sheet wrapped up to form a seamless tube. The diameter and the helicity of a SWNT are defined by the roll-up vector called chiral vector [14] given by:

\[
\overrightarrow{C}_h = n\overrightarrow{a}_1 + m\overrightarrow{a}_2
\]  

This roll-up vector connects crystallographically equivalent sites on this sheet, it defines the circumference on the surface of the tube connecting two equivalent carbon atoms as shown in Figure 2, \(a_1\) and \(a_2\) are the graphene lattice vectors. These unit vectors of the hexagonal lattice can be [15]:

\[
a_1 = (3/2a_{c-c}\sqrt{3/2a_{c-c}})
\]

\[
a_2 = (3/2a_{c-c}\sqrt{3/2a_{c-c}})
\]
n and m are integers, they determine if a SWNT will be a metal or a semiconductor. They are also called indexes also allow to determine the chiral angle that is given by:

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}n}{2m+n}\right)$$

(4)

The chiral angle $\theta$ is used to separate carbon nanotubes into three classes differentiated by their electronic properties: zig-zag ($m = 0$, $n > 0$, $\theta = 0^\circ$), armchair ($n = m$, $\theta = 30^\circ$), and chiral ($0 < |m| < n$, $0 < \theta < 30^\circ$) can see in Figure 3.

Armchair carbon nanotubes are metallic. Zig-zag and chiral nanotubes can be semi-metals with a finite band gap if $n - m/3 = \text{integer}$ and $m \neq n$ or semiconductors in all other cases. The band gap for the semi-metallic and semiconductor nanotubes scales in the order of the inverse of the CNT diameter giving each nanotube a distinctive electronic behavior. Each nanotube can be uniquely specified by its diameter $d'$ and its chiral angle $\theta$. The diameter of the nanotube can be expressed as:

$$d = Ch/\pi = \sqrt{3}.a_c(m^2 + mn + n^2)^{1/2}/\pi$$

(5)

3. **CNTFET STRUCTURE**

The first CNTFETs were conceived in a very easiest way, as only a proof of concept and a basic understand were the goals of these new devices. The first CNTFETs were reported in 1998. The first generation of CNTs are given in Figure 4.
CNFETs are considered as a potential candidate to replace MOSFETS beyond the 11nm technology node because of the good electrical transport properties of carbone nanotubes and also the feasibility of using CNTs to conceive CNTFETs with a very good electrostatic control [18].

These simple devices were fabricated by depositing single-wall CNTs from solution on to oxidized Silicon wafers that had been prepattemed using gold or platinum electrodes that served as source and drain electrodes connected via the nanotube channel, and the doped Si substrate served as the device gate [19]-[20]. The operating principle of the conventional field effect transistor based on carbon nanotube is very similar to a MOSFET Transistor considering replacing the channel material to take advantage of ballistic transport in the CNTs, where electrons are supplied by source terminal and drain terminal will collect these carriers nevertheless, the arrangement keeps changing in order to improve the performance of the device.

Because of these unique fetures, CNTFETs become devices of special interest. Field effect transistors made of carbon nanotubes so far can be classified into two 2 biggest classes: back-gated CNFETs and top-gated ones [21]. Lately, a new structure has been introduced known as vertical CNTFETs.

CNTFETs are also three terminals device like MOSFETS, the difference between these two field effect devices is that CNTFETs employ the CNT as a channel between its source and its drain terminals where as MOSFETs channel is made of doped Si. According to the number of layers in the channel of the CNTFETs, this device can be Single Wall (SW) or Multi Wall (MW).

CNTFET devices have two modes of operation, the Schottky-Barrier (SB) or MOSFET-Like CNTFETs. The structure between these two CNFET is only slightly different but results in different transistor operation [22]. In the SB-CNTFETs the gate voltage modulates the current which flow in the channel by changing the width of the barrier. But in MOSFET-Like CNTFETs the gate voltage can be controlled in the drain current by changing the height of the barrier.

4. CNTFETS SIMULATION MODEL

To investigate the chirality effects on our device DC performance, a simple two-dimension alanalytical model for ballistic CNTFET issued and shown in Figure 8. Our simulation study is carried out based on surface potential model described by Rhaman et al. This is an extension of the earlier work already done by K. Natori. This model consists of three capacitors that are attached as terminals of the device. As shown in Figure 8, a charge is placed at the top of the barrier.
The top of the barrier’s local density of states noted LDOS indicates the charge by the self-consistent potential. At the top of the barrier, the equilibrium electron density $N_0$ is given by:

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F) dE$$

(6)

where $D(E)$ is the local density of state at the top of the barrier and $f(E - E_F)$ represents the equilibrium Fermi distribution function. The positive velocity states $N_1$ are occupied by the source and the negative velocity states $N_2$ are occupied by the drain. $N_1$ and $N_2$ are given by [24]:

$$N_1 = \frac{d(E)}{2} \int_{-\infty}^{+\infty} f(E + U_{scf} - E_{F1}) dE$$

(7)

$$N_2 = \frac{d(E)}{2} \int_{-\infty}^{+\infty} f(E + U_{scf} - E_{F2}) dE$$

(8)

$E_{F1}$ and $E_{F2}$ are Fermi levels and $U_{scf}$ is the self-consistent potential at the top of the barrier. The Laplace potential $U_L$ at the top of the barrier ignoring mobile charge is given by [18]: Calculate a Laplace potential $U_L$:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S)$$

(9)

Where: $\alpha_G = \frac{C_G}{C_T}, \alpha_D = \frac{C_D}{C_T}, \alpha_S = \frac{C_S}{C_T}$

$C_T$ is the parallel combination of three capacitors $C_G, C_D, C_S$. The potential due to mobile charge $U_p$ can be expressed by:

$$U_p = \frac{q^2}{C_T}(N_1 + N_2) - N_0$$

(10)

The entire self-consistent potential $U_{scf}$ is given by superposition of $U_L$ and $U_P$ potentials [18]:

$$U_{scf} = U_L + U_P$$

(11)

$$U_{scf} = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + \frac{q^2}{C_T}(N_1 + N_2) - N_0$$

(12)

$$I_D = \frac{4e\beta T}{h} \left[ \ln \left( 1 + \exp\left( E_{F1} - U_{scf} \right) \right) - \ln \left( 1 + \exp\left( E_{F2} - U_{scf} \right) \right) \right]$$

(13)

$k_B$ is the Boltzmann constant, $T$: the operating temperature, $E_F$: the Fermi energy, $U_{scf}$: surface potential and $q$ the charge electric field.

5. RESULTS AND DISCUSSION

To investigate the performance of scaled carbon nanotube MOSFETs, we simulated a planar CNTFET with a ballistic channel, at room temperature. The device simulated has a 10 nm SiO$_2$ gate oxide thickness. Different diameters, which results in different bandgap allowing different drain current are simulated. We explore various issues by varying two parameters that are the chirality and the oxide thickness.

*Effect of Chirality and Oxide Thickness on the Performance of a Ballistic CNTFET (Asma Laribi)*
5.1. Effect of chirality on the electrical device characteristics

In this section, we study the chirality effects on the CNTFETs’ characteristics, knowing that the chirality \((n, m)\) of SWNTs determines the diameter of CNT, and the CNT’s energy gap. In this work SiO\(_2\) gate insulator \((k=3.9)\) with 10 nm thickness is used, gate and drain control are \((0.88 \text{ and } 0.35)\) respectively, the source fermi level is equal to \(-0.32\) eV and operating temperature is 300°K. To investigate the influence of the chirality on CNTFET we have simulated four CNTFETs with different diameters and obviously different \((n, m)\) given in Table 1.

<table>
<thead>
<tr>
<th>Chirality ((n,m))</th>
<th>Diameter (nm)</th>
<th>Energy gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>((5,0))</td>
<td>3.9e-10</td>
<td>2.17</td>
</tr>
<tr>
<td>((10,0))</td>
<td>7.8e-10</td>
<td>1.0</td>
</tr>
<tr>
<td>((19,0))</td>
<td>1.5e-09</td>
<td>0.5</td>
</tr>
<tr>
<td>((26,0))</td>
<td>2.0e-09</td>
<td>0.4</td>
</tr>
</tbody>
</table>

All simulation results allowing observing chirality influence on the drain current of our device are given in Figure 10 – 13:

(a)

Figure 9. The I-V characteristics of a \((5-0)\) SWNT : (a) \(I_d-V_d\) (b) \(I_d-V_g\) in logarithmic scale

(b)

(a)

(b)

Figure 10. The I-V characteristics of a \((10-0)\) SWNT: (a) \(I_d-V_d\) (b) \(I_d-V_g\) in logarithmic scale
Effect of Chirality and Oxide Thickness on the Performance of a Ballistic CNTFET (Asma Laribi)

In this part we will explore the effect of chirality, the figure 9, 10, 11, 12(a) shows that the chirality is directly related to CNTs’ diameter, and the diameter variation has a direct effect on the transistor and this is indicated in equation 5, and the gap is inversely proportional to the diameter of the carbon nanotube. The chirality has an impact on the device output current. Indeed, when the chirality increases the drain current increases in Figure 10, for (n,m)=(5, 0) at VG=1V, drain current of 5µA has been obtained and for (n,m)=(26, 0) a drain current of 24 µA has been obtained. It can be seen CNTFETs using carbon nanotube with larger diameter have a higher drain current, Figure 9, 10, 11, 12(b) the curves is shown in logarithmic scale at gate voltage of 0.6 V the impact of chirality on Off current.

Table 2 gives the value for Ion and Ioff current we remark that when the chirality increase the value of Ion current increase also. The diameter on CNT has specially effect on drain current (on –current), automatically the ratio Ion/Ioff increase for (26,0) chirality.
5.2. Effect of oxide thickness

In this section the impact of oxide thickness on the output characteristic of CNTFET performance is simulated, the nanotube diameter will be fixed at 2 nm and the \( t \) is varied from 1-5 nm.

The Figure 14, 15, 16(a) show the drain current for different oxide insulator in linear scale, we observe that when the gate oxide thickness is thin the conductivity increase and the leakage current is not increasing, from higher value from insulator thickness the height of potential barrier becomes high is controlled by the gate source voltage.

The Figure 14, 15, 16(b) show the drain current for different oxide insulator in logarithm scale we observe the influence on variance of insulator gate oxide thickness on current \( I_{on} \). \( I_{ds} \) (\( I_{off} \)) is unchanged, we conclude when the insulator thickness is reduced the ratio \( I_{on}/I_{off} \) will increase.

<table>
<thead>
<tr>
<th>Chirality (n,m)</th>
<th>( I_{on} )(( \mu A ))</th>
<th>( I_{off} )(( \mu A ))</th>
<th>( I_{on}/I_{off} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(5,0)</td>
<td>2</td>
<td>3.8 x 10^{-5}</td>
<td>0.5 x 10^{7}</td>
</tr>
<tr>
<td>(10,0)</td>
<td>3.5</td>
<td>3.8 x 10^{-5}</td>
<td>0.9 x 10^{7}</td>
</tr>
<tr>
<td>(19,0)</td>
<td>5.8</td>
<td>3.8 x 10^{-5}</td>
<td>1.5 x 10^{7}</td>
</tr>
<tr>
<td>(26,0)</td>
<td>7.8</td>
<td>3.8 x 10^{-5}</td>
<td>2 x 10^{7}</td>
</tr>
</tbody>
</table>

Figure 14. The I-V characteristics of oxide thickness \( t=3 \)nm: (a) \( I_{ds} - V_{ds} \) (b) \( I_{ds} - V_{gs} \) in logarithmic scale

Figure 15. The I-V characteristics of oxide thickness \( t=2 \) nm: (a) \( I_{ds} - V_{ds} \) (b) \( I_{ds} - V_{gs} \) in logarithmic scale
Effect of Chirality and Oxide Thickness on the Performance of a Ballistic CNTFET (Asma Laribi)

6. CONCLUSION

In this paper we have investigated the effect of chirality and gate oxide thickness on performance of CNTFET device, I have analyse in the first part the influence of chirality on the output characteristics for carbon nanotube field effect transistor. Through simulation result we have observed that when chirality increases the current value increase and the ratio Io/Ioff is proportionnel to the chirality.

From second part we have study the impact of gate oxide thickness on drain current we can observe that the current is affected by the gate insulator thickness, the oxide thickness affects the Ion current but the Ioff current remain stable. The accuracy of our result can be proved by comparing other research group work which is identical. Analysis results conclude that the CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics.

Table 3. Value of Ion and Ioff current for oxide thickness

<table>
<thead>
<tr>
<th>Oxide thickness (nm)</th>
<th>Ion(μA)</th>
<th>Ioff(μA)</th>
<th>Ion/Ioff</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>36</td>
<td>3.8x10^4</td>
<td>9.4 x 10^5</td>
</tr>
<tr>
<td>2</td>
<td>18</td>
<td>3.8x10^4</td>
<td>4.7 x 10^4</td>
</tr>
<tr>
<td>3</td>
<td>13</td>
<td>3.8x10^4</td>
<td>3.4 x 10^3</td>
</tr>
<tr>
<td>5</td>
<td>9</td>
<td>3.8x10^5</td>
<td>2.3 x 10^5</td>
</tr>
</tbody>
</table>

From Table 3 we remark that the Ion current is inversely proportional to the insulator thickness and the leakage current is not affected by the gate insulator thickness but the ratio Ion/Ioff will increase when the value of gate oxide thickness is decrease. Our simulation accuracy can be justified by investigating other simulation result, the result is approximately equal compared with result in Figure 18.
REFERENCES


