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Performance analysis and small signal modeling of DMG AlGaN/GaN HFET

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ABSTRACT

This article reports 20-elements based small signal model for unique and enhanced asymmetric dual material gate (DMG) AlGaN/GaN HFET first time. Enhanced device structure incorporates field plate and dual material gate engineering for suppressing short channel effects, thereby, improving carrier transport efficiency in the device. Extraction of extrinsic and intrinsic parameters of the device and modeling of important microwave figure of merits are cenral points of this research article. The model elements are extracted from s-parameters as a cold FET structure under pinch-off biasing using direct extraction method. Extrinsic elements are extracted deliberately using low frequency band at which parameters generally attain good linearity, thus assuring extraction accuracy. After de-embedding extrinsic elements, intrinsic Y-parameters are obtained for extraction of intrinsic elements of the model. Paper also models important figure of merits of device such as transconductance, drain conductance, current gain , transducer power gain, available power gain, maximum stable gain, maximum frequency of oscillation, cut-off frequency, stability factor and time delay for microwave performance analysis. Reported results are compared with published and simulated results and found to be within the permissible range of tolerances.

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1. INTRODUCTION

Due to unique properties of GaN material, it is possible to obtain large current densities in GaN-based HEMTs [1] [2]. GaN based devices are also very useful for high frequency high temperature microwave applications such as radar systems [3] [4]. In the recent past, scientists have successfully fabricated dual material gate AlGaAs/GaAs HEMTs structure using two metals of different work functions [4] . Since analytical models help us to understand internal solid state device physics thus expected to be consistent with physical behavior of device. An accurate small signal model of HFET is extremely valuable for designing of important active circuits generally used for high frequency applications [6] [7] [8].

These small signal compact models define physical characteristics and various limitations of active devices accurately [9], thus used for design of low noise power amplifiers by electronics and microwave engineers in industry. Small signal models are also very useful for CAD based simulations [10] targeted for analysis of newly developed device structures [11]. In present scenario, analytical models are much exploited for getting true feedback about optimization of fabrication process in semiconductor industries [12] [13] . In past a number of small signal models were developed based on various approaches of modelling scientists [14] [15]. One of initial kind of detailed small signal model that describe extraction procedure of FET structures, was proposed in 1988 by Dambrine, et al [16]. In recent past many researchers have developed variety of techniques and methods according to their used material system and device structures [17] [18]. It is possible to classify some existing modeling methods in three broad categories: whole optimization, partial optimization [19] and direct extraction methods [20] [21]. We used direct extraction method for our model as

it is clear that the direct parameter extraction technique provides better consistency between parameter values and their physical meanings in the device structure. It also facilitates extraction process to run faster than other techniques. This approach is also more compatible as it considers important frequency points and its different coefficients during used in extraction process are determined by device structure itself [22].

2. MODEL FORMULATIONS

2.1 Device description:

Self explanatory schematic view of device structure of dual channel dual material gate $Al_{0.3}Ga_{0.7}N$/ GaN HFET is shown in Fig.1. In the figure metals M_1 (Au) and M_2 (Ni) of work functions ϕ_{M1} and ϕ_{M2} respectively are used to form tied dual metal gate of device [5] [23]. Gate forms Schottky junctions with unintentionally doped (UID) $Al_{0.3}Ga_{0.7}N$ cap layer of 3nm thickness. A field plate is used over DMG gate with Si_3N_4 passivation layer in between. AlGaN cap layer forms interface between n-$Al_{0.3}Ga_{0.7}N$ layer of 18 nm thickness that followed by UID AlGaN spacer layer of 3 nm thickness. Purpose of introducing UID AlGaN spacer layer is to reduce ionized impurity scattering. A 2µm thick GaN channel layer is used to form hetro-interface that creates 2-DEG conductive channel in the device. Sapphire substrate is used for device structure as it can withstand higher operating temperature.

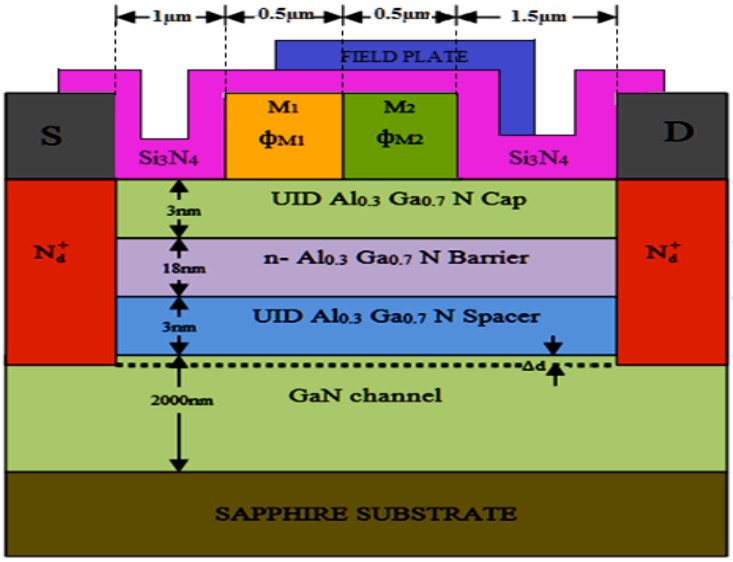

Figure 1 Cross sectional schematic of asymmetric DMG $Al_{0.3}Ga_{0.7}N$/GaN HFET with dual metal gate regions work function (ϕ_{M1})=5.3eV and (ϕ_{M2}) =4..4 eV, gate width (W)=100µm, Δd represents distance of 2DEG

2.2 Model description:

Fig.2 represents small signal equivalent model of device. R_g, R_s and R_d represent parasitic resistances of gate, source and drain respectively. L_s, L_d , L_g represent source, drain, gate electrodes inductances respectively. C_{pd} and C_{pg} and C_{pgd} represent device contact pad capacitances between drain-source, gate-source and gate drain respectively. C_{pdi} and C_{pgdi} and C_{pgi} are inter-electrodes capacitances between drain-source, gate-drain and gate-source respectively. R_{gs} and R_{gd} represent input and output channel region resistances. C_{ds} C_{gs} and C_{gd} represent intrinsic capacitances between drain-source, gate-source and gate-drain respectively. g_{ds} and g_m represents drain conductance and transconductance of device. The g_mV_{gs} in small signal model represent current generator in the output circuit, where V_{gs} represents as gate to source voltage. Gate capacitances with a phase shift of $e^{-j\omega\tau}$ represent transit time (τ) through the velocity saturated region of the 2DEG-channel. The ω is angular frequency in rad/sec of the applied small RF signal at gate terminal.

2.3 Parameters extraction method:

Parameter extraction is performed by using direct method as suggested by Minasian [24] and later modified by Dambrine et al [16]. and Berroth and Bosch [25]. Initially S-parameter extraction is carried out for shunt and series extrinsic elements of device under pinch off mode of biasing keeping frequency with in 5GHz range. These measured s-parameters are then successively transformed into Z-parameters and Y-parameters in order to obtain values of all the series and shunt parasitic elements. Again after de-embedding of all the parasitic elements, the intrinsic Y-parameters are determined. At the end intrinsic elements are derived by separating real and imaginary parts of intrinsic Y-parameters.

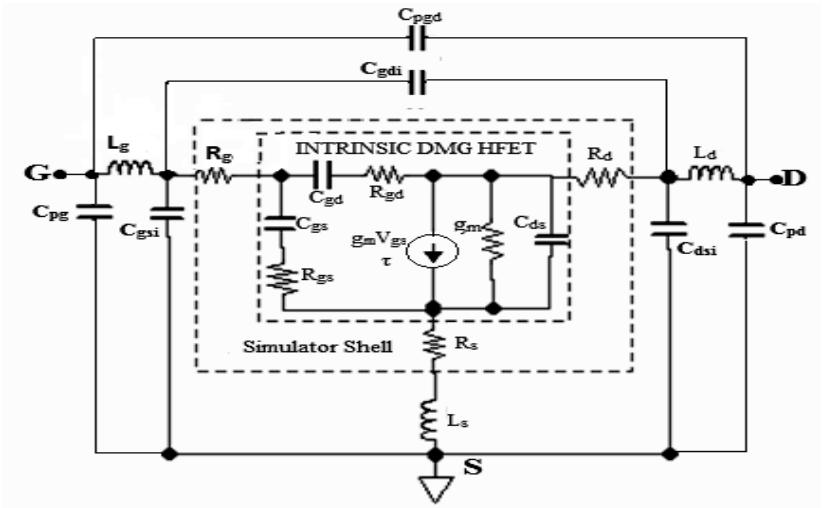

Figure **2** Small signal equivalent circuit model of DMG AlGaN/GaN HFET

Fig.3 shows block diagram for extraction of s-parameters by using two port matching lossless output and input network. Circuit shows E_s, Z_s and Z_L as excitation source, source impedance and load impedances respectively. P_i , P_A, P_L and P_{avo} represent input power, available input power, power delivered to load and available power at output respectively.

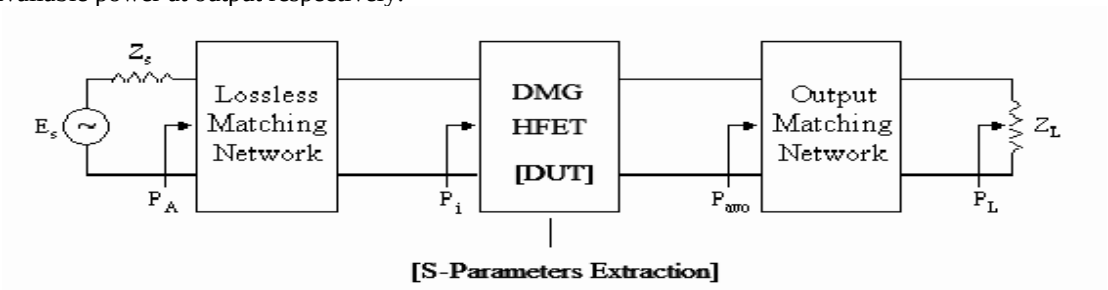

Figure 3 Matching impedance network for s-parameters measurement

2.4 Extrinsic parameters extraction:

The extrinsic elements are extracted from imaginary Y-parameters under pinch-off condition $V_{pinch\text{-}off}$ (V_{gs}< -V_p and V_{ds}=0V). Now the equivalent voltage controlled current source forming intrinsic part of device is disabled. In case of low frequency in the range of 5 Ghz, the whole circuit can be treated as a capacitive network as shown in Fig.4. Now following equations appropriately describe the relationship between extrinsic capacitances and imaginary parts of the Y-parameters as

$$\mathrm{Im}(Y_{11}) = j\omega\left(C_{pg} + C_{gsi} + C_{gsp} + C_{gdp} + C_{gdi} + C_{pgd}\right) \quad (1)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega(C_{gdp} + C_{gdi} + C_{pgd}) \quad (2)$$

$$\mathrm{Im}(Y_{22}) = j\omega\left(C_{dsp} + C_{pd} + C_{dsi} + C_{gdp} + C_{gdi} + C_{pgd}\right) \quad (3)$$

Fig.5 shows imaginary Y-parameter curves with in frequency range of 5GHz as it is clear that Y-parameters have sufficient linearity at low frequency range. Therefore, the parasitic capacitances can be safely extracted from the slop of imaginary y-parameter curves.

Here, C_{gsp}, C_{gdp} and C_{dsp} provide intrinsic substitute of pinched of cold FET part of circuit. Assumption is made as

$$C_{dsp} = 12C_{pd} \quad (4)$$

Due to asymmetric device structure ratio of gate-drain spacing with that of gate-source spacing is 1.5. So the relationship of its capacitance can be expressed as

$$C_{gsp} = 1.5C_{gdp} \quad (5)$$

Since size and shape of all pads are same so these capacitances can be treated as equal in value as

$$C_{pg} = C_{pd} = C_{pgd} \quad (6)$$

Considering device structure C_{dsi} is larger than pad capacitances. An assumption made as

$$C_{gdp} = C_{gdi} \quad (7)$$

Under high frequency small input signal with gate forward biased (V_{gs}≥0) drain at zero potential (V_{ds}=0V), small signal equivalent circuit is reduced as in Fig.6. In this condition gate leakage current (I_g) flows and

internal device capacitances are shunted with conductance open circuited. Since all inter electrodes capacitances are inside of parasitic resistance so no approximation needed by keeping precision of compact model as intact. At this specific bias point, the following simplified equations of Z-parameters are valid:

$$Z_{11} = R_s + R_g + \frac{R_c}{1+r} + \frac{\eta KT}{qI_g} + j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{gf}} + \frac{1}{j\omega C_{sf}} \quad (8)$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{r} + j\omega L_s + \frac{1}{j\omega C_{sf}} \quad (9)$$

$$Z_{22} = R_s + R_d + R_c + j\omega\left(L_s + L_d\right) + \frac{1}{j\omega C_{df}} + \frac{1}{j\omega C_{sf}} \quad (10)$$

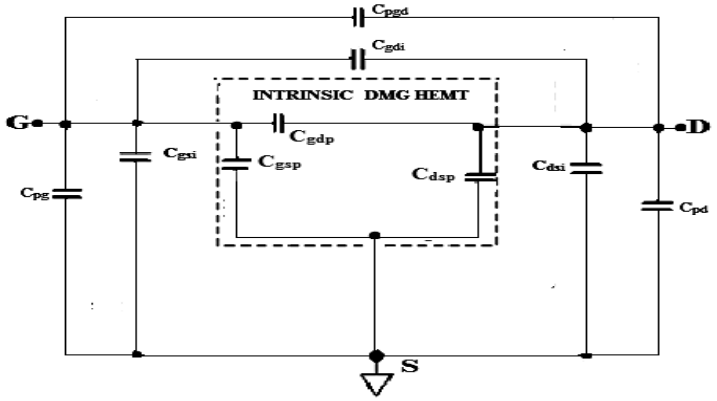

Figure 4 Small signal cold pinch off equivalent circuit at low frequency

Where R_c represents channel resistance and r determines ratio of channel resistance between gate to drain and gate to source i.e ($r=R_{cgd}/ R_{cgs}$). As per our proposed asymmetric device structure value of r is 1.5 considering source and drain separation from gate. C_{df} , C_{gf} and C_{sf} represent fringing capacitances resulting at drain, gate and source terminals respectively in cold FET high frequency equivalent circuit shown in Fig.6. Also $\eta kT/qI_g$ in equation (8) gives the differential resistance of the Schottky diode. In this expression η, K and T represent ideality factor of diode, Boltzmann constant and absolute ambient temperature respectively. Now by transforming Y-parameters to Z-parameters, R_g, R_s and R_d can be extracted from the Re (Z_{ij}) curves. By multiplying ω by imaginary parts of impedances, following expressions are obtained

$$\mathrm{Im}(\omega Z_{11}) = \omega^2(L_s + L_g) - \frac{1}{C_{gf}} - \frac{1}{C_{sf}} \quad (11)$$

$$\mathrm{Im}(\omega Z_{12}) = \omega^2 L_s - \frac{1}{C_{sf}} \quad (12)$$

$$\mathrm{Im}(\omega Z_{22}) = \omega^2(L_s + L_d) - \frac{1}{C_{df}} + \frac{1}{C_{sf}} \quad (13)$$

The $\omega\mathrm{Im}(Z_{ij})$ versus ω^2 plot is shown in Fig.7. Slop of these curves can be used to extract values of L_g, L_d and L_s respectively. The imaginary part of the Z-parameters increases linearly with frequency but real part is independent from frequency variations. The value of R_c is determined by forming following equations by using pinch off Z-parameters as follows

$$\mathrm{Re}(Z_{22\,pinch\text{-}off}) = R_s + R_d \quad (14)$$

Also, from equation (10) it is noted that

$$\mathrm{Re}(Z_{22}) = R_c + R_d + R_c \quad (15)$$

$$R_c = \mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{22\,pinch\text{-}off}) \quad (16)$$

2.5 Intrinsic parameters extraction:

The intrinsic part of our device can be described by the following Y-parameters,

$$Y_{11\mathrm{int}} = \frac{\omega^2 C_{gs}{}^2 R_{gs}}{\delta} + \frac{\omega^2 C_{gd}{}^2 R_{gd}}{\theta} + j\omega\left(\frac{C_{gs}}{\delta} + \frac{C_{gd}}{\theta}\right) \quad (17)$$

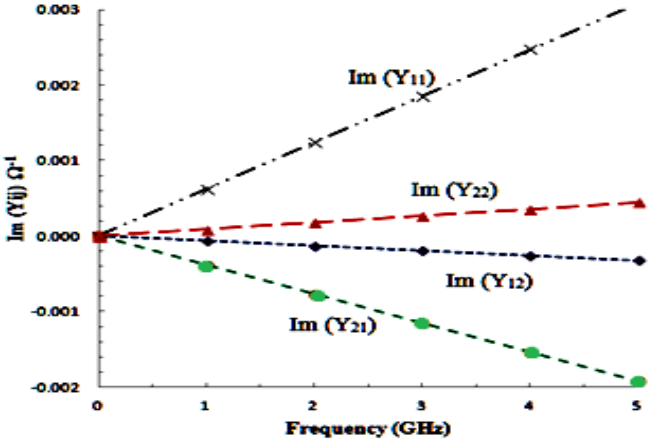

Figure 5 Variation of imaginary Y-parameters with frequency

$$Y_{12\text{int}} = -\frac{\omega^2 C_{gd}{}^2 R_{gd}}{\theta} - j\omega\frac{C_{gd}}{\theta} \tag{18}$$

$$Y_{21\text{int}} = g_m e^{-j\omega\tau} - \frac{\omega^2 C_{gd}{}^2 R_{gd}}{\theta} - j\omega\frac{C_{gd}}{\theta} \tag{19}$$

$$Y_{22\text{int}} = g_{ds} + \frac{\omega^2 C_{gd}{}^2 R_{gd}}{\theta} + j\omega\left(C_{ds} + \frac{C_{gd}}{\theta}\right) \tag{20}$$

Where

$$\delta = 1 + u^2 \tag{21}$$

$$u = \omega C_{gs} R_{gs} \tag{22}$$

$$\theta = 1 + v^2 \tag{23}$$

$$v = \omega C_{gd} R_{gd} \tag{24}$$

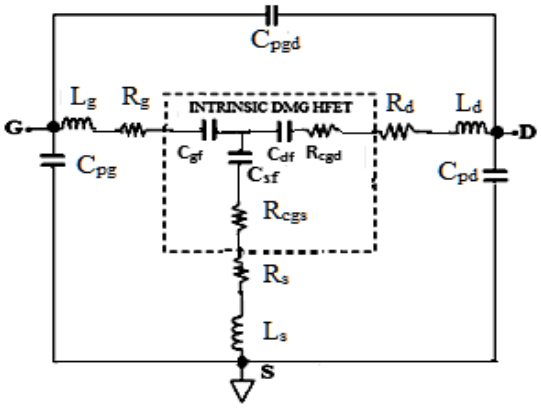

Figure 6 Small signal equivalent circuit under cold FET pinch-off biasing

Therefore, the value of individual intrinsic parameter can be derived from equations (17) to (20) by separating real and imaginary parts of $Y_{11\text{int}}$, $Y_{12\text{int}}$, $Y_{21\text{int}}$ and $Y_{22\text{int}}$ and using following expressions

$$C_{gd} = -(1-v^2)\frac{\text{Im}(Y_{12\text{int}})}{\omega} \tag{25}$$

$$R_{gd} = \frac{v}{(1+v^2)\text{Im}(Y_{12\text{int}})} \tag{26}$$

$$C_{gs} = (1+u^2)\frac{\text{Im}(Y_{11\text{int}}) + \text{Im}(Y_{12\text{int}})}{\omega} \tag{27}$$

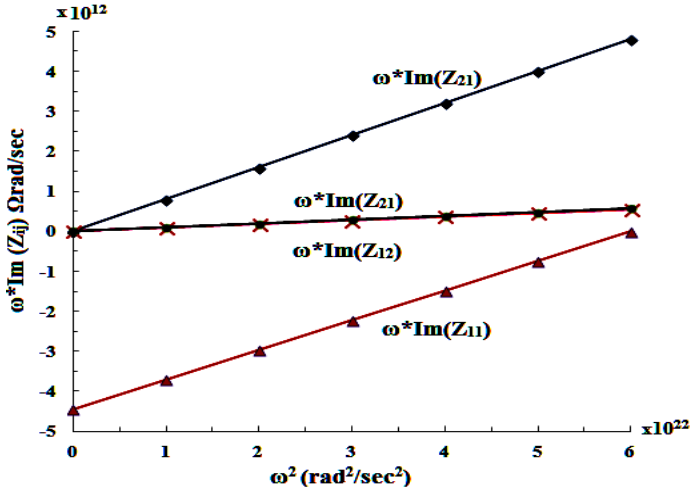

Figure 7 Variation of ω.Im(Z_{ij}) with ω^2

$$R_{gs} = \frac{u}{1-u^2}\mathrm{Im}\left(Y_{11\mathrm{int}} + Y_{12\mathrm{int}}\right) \tag{28}$$

$$g_m = \left|Y_{21\mathrm{int}} - Y_{12\mathrm{int}}\right| \tag{29}$$

$$\tau = -\frac{1}{\omega}\arctan\left(\frac{\mathrm{Im}\left(Y_{21\mathrm{int}} - Y_{12\mathrm{int}}\right)}{\mathrm{Re}\left(Y_{21\mathrm{int}} - Y_{12\mathrm{int}}\right)}\right) \tag{30}$$

$$C_{ds} = \frac{\mathrm{Im}\left(Y_{22\mathrm{int}} + Y_{12\mathrm{int}}\right)}{\omega} \tag{31}$$

$$g_{ds} = \mathrm{Re}\left(Y_{22\mathrm{int}} + Y_{12\mathrm{int}}\right) \tag{32}$$

2.6 Modeling device gains and important figures of merits:

Paper models following figure of merits for proposed unique device

Transducer power gain (G_{TP})

$$G_{TP} = \frac{P_L}{P_A} \tag{33}$$

For S_{12}=0 values unilateral transducer power gain (G_{UTP}) is obtained as

$$G_{UTP} = \frac{P_L}{P_{AS_{12}=0}} \tag{34}$$

Available power gain (G_{AP})

$$G_{AP} = \frac{P_{avo}}{P_A} \tag{35}$$

Since $P_{avo} \leq P_A$, thus power gain $G_{AP} \geq G_{TP}$

Maximum available gain (G_{MAX}) occurs for the simultaneous conjugate match at the input and output port if the transistor is unconditionally stable i.e. (k>1) and given as

$$G_{MAX} = \frac{\left|S_{21}\right|}{\left|S_{12}\right|}\left(k \pm \sqrt{k^2 - 1}\right) \tag{36}$$

Where *k* represents stability factor of device and obtained as

$$k = \frac{1 + \left|S_{11}S_{22} - S_{21}S_{12}\right|^2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2}{2\left|S_{12}S_{21}\right|} \tag{37}$$

Maximum stable gain (G_{MS}) occurs when the two port are resistively loaded till stability factor becomes unity i.e. (k = 1), G_{MAX} of the two port of equation (36) becomes maximum stable gain and obtained as

$$G_{MS} = \frac{\left|S_{21}\right|}{\left|S_{12}\right|} \tag{38}$$

Maximum unilateral transducer power gain (G_{UTPM}) is obtained when the transistor becomes unconditionally stable and obtained as

$$G_{UTPM} = \frac{\left|S_{21}\right|^2}{\left(1-\left|S_{11}\right|^2\right)\left(1-\left|S_{22}\right|^2\right)} \tag{39}$$

Maximum unilateral power gain (G_{UPM}) is largest gain and obtained as

$$G_{UPM} = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}}-1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)} \tag{40}$$

Current gain|H_{21}| *is* important and used to obtain cut off frequency of device

$$\left|H_{21}\right| = \frac{2S_{12}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \tag{41}$$

Cut off frequency (f_t) for DCDMG AlGaN HEMT at which short circuit current gain rolls off to 0 dB can be obtained as

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})[1+(R_s+R_d)g_{ds}]+C_{gd}g_m(R_s+R_d)} \tag{42}$$

Maximum oscillation frequency (f_{max}) can be determined by using intrinsic and extrinsic components of device as

$$f_{\max} = \frac{f_t}{2\sqrt{((R_g+R_s+R_{gs})g_{ds}+2\pi f_t C_{gd}R_g)}} \tag{43}$$

Evaluated parameters are listed as follows:

Table 1 Extracted parameters values at V_{ds}=24V and V_{gs}=-1V for gate size100μm^2

Parameter	**Value**	**Parameter**	**Value**
g_m	800mS/mm	R_d	11.2Ω
C_{gs}	1.23fF	L_s	0.6pH
C_{gd}	2.22fF	L_g	42.4pH
C_{ds}	2.12fF	L_d	52.5pH
g_{ds}	500mS/mm	C_{pg}	18fF
R_{gs}	3.1Ω	C_{pd}	23fF
R_{gd}	1.8KΩ	C_{pgd}	13fF
τ	0.91pS	C_{gdi}	18fF
R_s	4.2Ω	C_{gsi}	18fF
R_g	6.5Ω	C_{dsi}	5fF

3. RESULTS AND DISCUSSIONS

Fig.8 shows simulated and experimental [26] output current voltage characteristics of device for various gate-to-source voltages (V_{gs}). Fig.9 shows simulated and experimental [26] input characteristics of DMG AlGaN/GaN HFET. It is evident from graph that gate voltage has effective control on drain current in DE mode of operation.The device stability analysis has been done with the help of Smith plots. The model and experimental [27] S_{11} and S_{22} are shown in Fig.10 and Fig.11 respectively. Smith plots analysis reveals that proposed device capacitance increases with frequency. At the lowest input frequency the input reflection coefficient S_{11}=+1 and represents maximum reflection and open circuit. But with the rise in frequency, the input reflection coefficient moves towards clockwise direction in the circle of capacitance and approaches to the matching point at S_{11}=0. Since, at the matching point no reflections would occur because of the impedance matching and confirms better functionality of device at higher frequency range. These model results and experimental results are also compared in the smith chart and are matching with the experimental data of similar size AlGaN/GaN HFET devices.

In Fig. 12 and Fig.13, values of the transmission coefficients (S_{21}) and (S_{12}) for a gate bias of -1 V are plotted on smith chart, with that of experimental data [27] and found to be trending with reported experimental. Graphs show that with rise in frequency, both the transmission coefficients move towards clockwise direction in the circle of inductances.

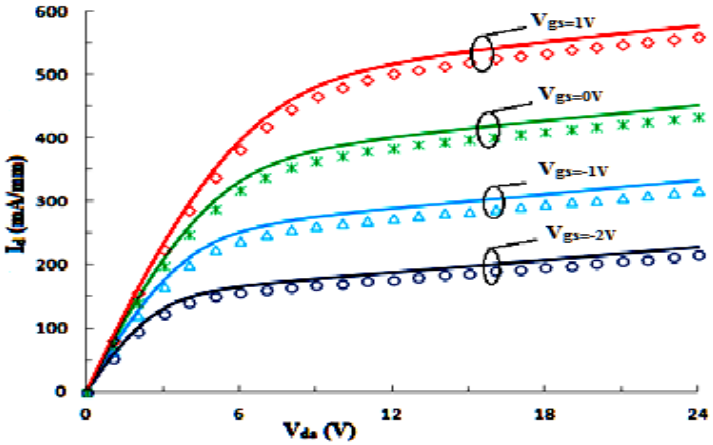

Figure 8 Output current voltage (I_d-V_{ds}) characteristics simulated (lines) experimental (symbols)

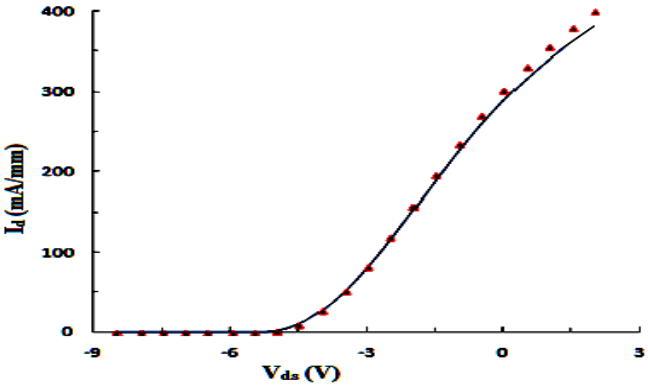

Figure 9 Input (I_d .V_{gs}) characteristics at V_{ds}=5V simulated (lines) experimental (symbols)

The device gains are plotted as a function of frequency at a gate bias of V_{gs}=-1V in Fig. 14.The gain are also compared with experimental [17] [26] results and found to be within the limit of tolerance (±.5%). Graph clearly demonstrates that the gains decrease with the rise in frequency and the cut-off frequency (f_t) occurs at 68 GHz and maximum oscillation (f_{max}) occurs at 178GHz. In Fig. 15, the variation of capacitances i.e. C_{gd}, C_{gs} and C_{ds} are demonstrated with the frequency. The capacitive elements values are found to be almost constant within the desired frequency range as shown thus assuring high extraction precision.

Fig.16 demonstrates the variation of cutoff frequency with V_{gs} at the V_{ds} =24 V. Fig.17 shows variation of transconductance with V_{gs}. Similarly variation of drain conductance with V_{ds} is shown by Fig.18. These plots also show comparison of model with experimental results [26] [28]and found to be in good agreement.

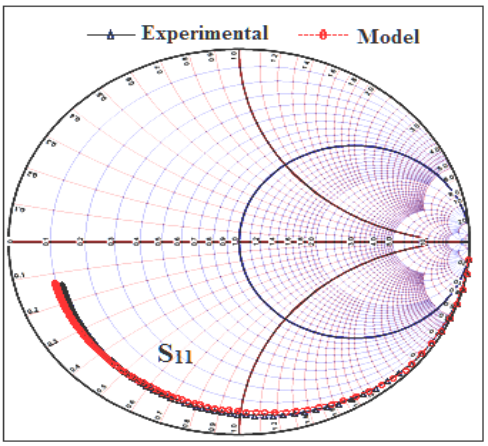

Figure 10 S_{11} smith plot at bias V_{ds}=24V and V_{gs}= -1V, between f_{start}=1GHz and f_{stop}=200 GHz

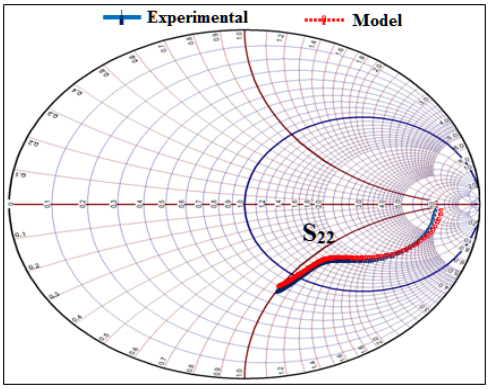

Figure 11 S_{22}-smith plot at bias V_{ds}=24V and V_{gs}= -1V, between f_{start}=1GHz and f_{stop}=200 GHz

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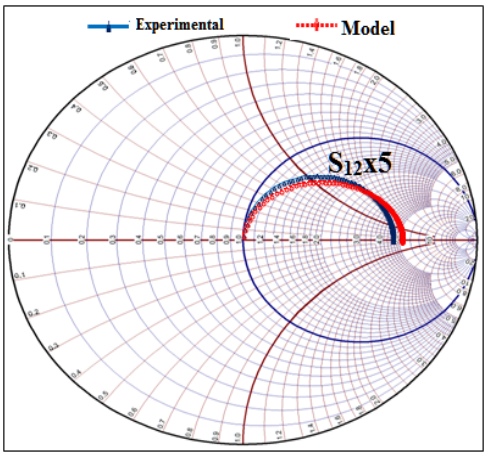

Figure 12 S_{12} on smith chart at bias V_{ds}=24V and V_{gs}= -1V, between f_{start}=1GHz and f_{stop}=200 GHz

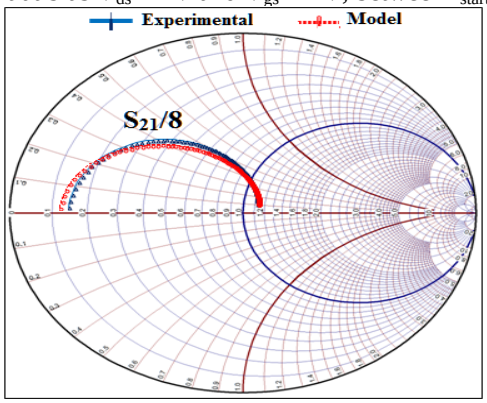

Figure 13 S_{21} on smith chart at bias V_{ds}=24V and V_{gs}= -1V, between f_{start}=1GHz and f_{stop}=200 GHz

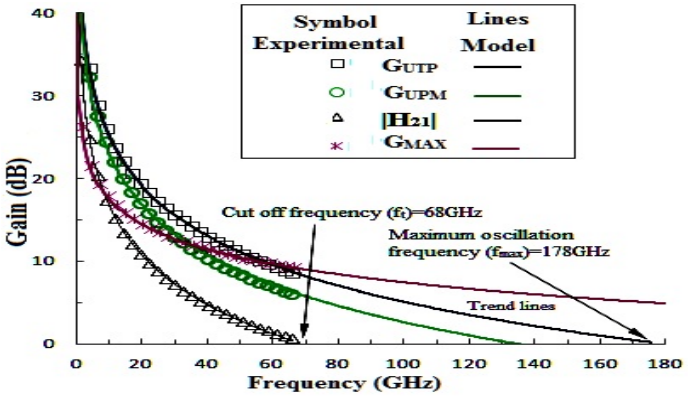

Figure 14 Variation of gains with frequency at V_{ds}=24V and V_{gs}= -1V

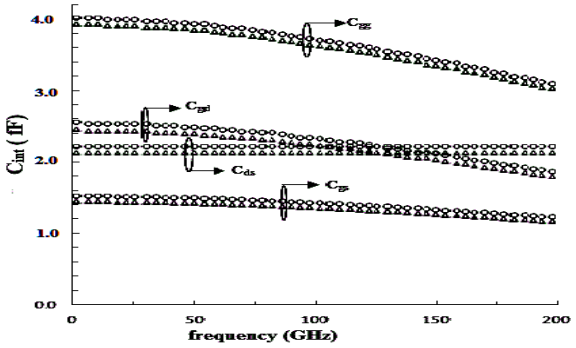

Figure 15 Intrinsic capacitances versus frequency plot model (circles) experimental (triangles) at V_{ds}=24V V_{gs}= -1V

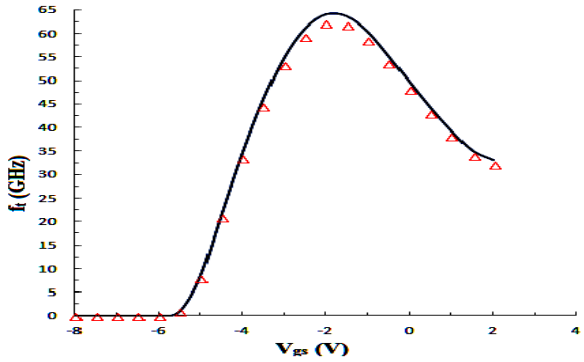

Figure 16 Variation of cutoff frequency with V_{gs} model (line) simulation (symbol) at V_{ds}=5V

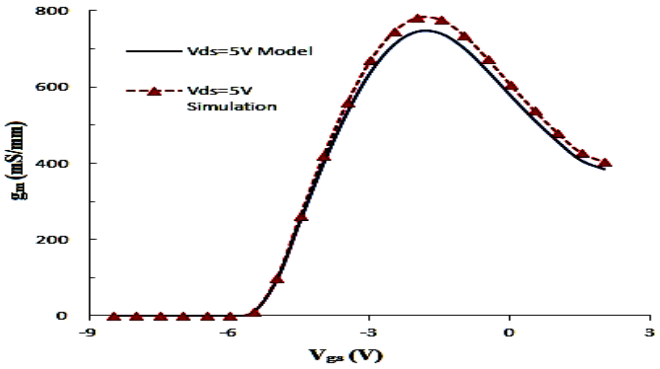

Figure 17 Transconductance (g_d) versus V_{gs} plot

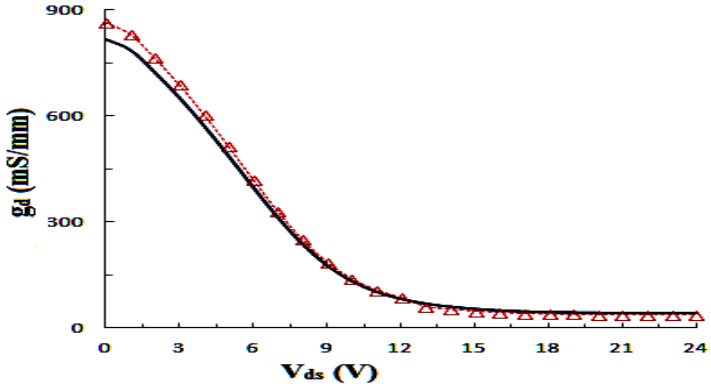

Figure 18 Variation of drain conductance (g_d) with V_{ds} at V_{gs} = -1 model (line) and experimental (dashed line with triangles)

4. CONCLUSIONS

Finally it can be concluded that the extracted 20-elements based small signal model of dual material gate $Al_{0.3}Ga_{0.7}N$ /GaN HFET structure is accurate and predict device behavior correctly for microwave range of frequencies. Parameters extracted using direct extraction method as a cold FET structure using low frequency signal to ensures extraction accuracy for the model. Device structure also simulated for input and output characteristics and results are compared with experimental data to analyze overall device behavior after optimization and due calibration process. The small signal model predicts maximum oscillation frequency (f_{max}) of 178 GHz and cut-off frequency (f_t) of 68 GHz. Some important figure of merits are also modeled and compared these include current gain $|H_{21}|$, transducer power gain (G_{TP}) , maximum stable gain (G_{MS}) , transconductance (g_m) , drain conductance (g_d) , stern stability factor (k), available power gain (G_{AP}) and time delay (τ) to assess overall microwave performance of enhanced device. All the extracted results are checked for consistency and accuracy keeping in mind permissible tolerances (±5%) during comparison with experimental data.

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