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Mr. Editor-in-Chief Prof. nzw. dr hab. inz. Lech M. Grzesiak

International Journal of Electrical and Computer Engineering (IJECE).

April 22, 2018

Dear Editor Prof. nzw. dr hab. inz. Lech M. Grzesiak,

I am pleased to submit an original research article entitled "Area & power efficient VLSI architecture of mode decision in Integer Motion estimation for HEVC video coding standard " EL ANSARI Abdessamad, Nejmeddine Bahri, MANSOURI Anass, AHAITOUF Ali, MASMOUDI Nouri for consideration for publication in the journal of *International Journal of Electrical and Computer Engineering (IJECE)*.

In this manuscript, we propose new parallel hardware architecture for mode decision the Sum Absolute of the Difference (SAD) for integer motion estimation (IME) in The High Efficiency Video coding (HEVC) encoder standard. Our architecture hardware is fully parallel and allows acceleration of motion estimation without any modification in the estimation algorithm itself. The experiment studies show that the proposed hardware architecture performs better that than the proposed design in the literature. The experiment results also show that our hardware design reaches a real time processing for 30 frames of ultra-high resolution 4k (3840×2160) at 115.15MHz.

We believe that this manuscript is appropriate for publication by the Journal of *Advances in Multimedia*. because it is included in the subjects namely Components, Circuits, Devices and Systems. Our manuscript creates a paradigm for future studies of HEVC extensions.

This manuscript is containing original research and has not been submitted / published earlier in any journal and is not being considered for publication elsewhere. All authors have seen and approved the manuscript and have contributed significantly for the paper. We have no conflicts of interest to disclose.

Thank you for your consideration of this manuscript.

Sincerely,

EL ANSARI Abdessamad

Signature