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A new high speed charge and high efficiency Li-Ion battery charger interface using pulse control technique

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ABSTRACT

A new Li-Ion battery charger interface (BCI) using pulse control (PC) technique is designed and analyzed in this paper. Thanks to the use of PC technique, the main standards of the Li-Ion battery charger, i.e. fast charge, small surface area and high efficiency, are achieved. The proposed charger achieves full charge in forty-one minutes passing by the constant current (CC) charging mode which also included the start-up and the constant voltage mode (CV) charging mode. It designed, simulated and layouted which occupies a small size area 0.1 mm^2 by using Taiwan Semiconductor Manufacturing Company 180 nm complementary metal oxide semi-conductor technology (TSMC 180 nm CMOS) technology in Cadence Virtuoso software. The battery voltage V_{BAT} varies between 2.9 V to 4.35 V and the maximum battery current I_{BAT} is 2.1 A in CC charging mode, according to a maximum input voltage V_{IN} equal 5 V. The maximum charging efficiency reaches 98%.

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1. INTRODUCTION

Battery is an assembly of electrochemical accumulators that are reversible generators. The electrical energy is stored as chemical form in the accumulator to be restored at any time on demand thanks to the reversibility of the transformation. An oxidation-reduction reaction is activated when a load is connected to the terminals of an elementary cell between two electrodes bathed in an electrolyte.

Li-Ion batteries are more usable in mobile electrical devices that require a powerful and light battery, as it produces a high storage density based on the low density. It can be divided into several types $LiFePO_4$, $LiCoO_2$, $LiNiMnCoO_2$ and $LiMn_2O_4$ exist according to their application such as telecommunications, laptops, electric bicycles and electric vehicles, respectively. This advantage makes it possible to choose the right technology or type for the particular application required. In today's automotive industry, Li-ion batteries are the best alternative to automotive fuel because they have the potential to be the answer to the challenges faced by automakers to provide solutions to the growing oil shortage and reduce the environmental impact of vehicles. Despite still significant constraints (recharging time, energy density, cost), the competitiveness of these batteries has already revived interest in electric vehicles.

The well-known charger solutions are essentially classified into two types: Low-drop-out (LDO) based charger and the switching-power-supply (SPS) based charger [1]. The choice of the technique to be used depends on the application to which it will be integrated. Table 1 provides a comparison between the two most popular types of charger solutions.

Table 1. The LDO-based charger versus the SPS-based

Performances	SPS-based charger	LDO-based charger
Input voltage range	Large	Low
Complexity	Medium	Low
Efficiency	High	Low
Size	Lower at high power	Small-medium

The use of the SPS technique with a low-pass filter to lower the input voltage, lower losses can be achieved than with LDO-based chargers [2], [3]. It gives a wide input/output voltage range [4] and also requires an advanced circuit design to achieve high efficiency. In addition, the maximum charging battery current is ranging from 300 mA to 2 A. Furthermore, the SPS chargers cost a lot of disadvantages, such as worse noise repudiation upon ripple at a SPS rate, and increased power consumption [5]. The size chip of the SPS-based chargers is smaller at high power. The several implementations of the SPS-based chargers are exposed in [6]–[12].

On the other hand, LDO-based chargers are based on a pass transistor to drop the excess input voltage in order to obtain an output regulation by modulating its resistance. Simplicity at the trouble of a poor efficiency and small size (for low to medium power) are the main advantages of it. The LDO-based charger meets these requirements due to its low ripple current and can be inserted into the chip without a descriptive component [13]. In addition, the maximum charging battery current is ranging from 350 mA to 1 A. Among the big problems for it is the low efficiency. Therefore the integration of a power-MOS is a solution to its low efficiency and also to minimize its loss [14]. The several implementations of the LDO-based chargers are exposed in [15]–[18]. To minimize the complexity of circuit design through CMOS technology improvements, LDO-based chargers and SPS-based chargers are usually inserted on a single chip. Subsequently, to reduce the noise and ripple effect, the battery charger interface (BCI) is merged into a system-on-chip (SoC) [4].

The three-step Li-Ion battery charging modes are shown in Figure 1. The first one is the start-up, the second one is the constant current (CC) charge and the last one is the constant voltage (CV) charge [19]. In the first step start-up, the battery current (I_{BAT}) is maintained at a constant low value when the battery voltage (V_{BAT}) is lower than the low voltage (V_L), this helps protect the battery from damage caused by overheating. Also in the second step CC, the battery is charged with a strong constant current (which minimizes the charging time) when V_{BAT} is between V_L and high voltage (V_H). Finally in the last step CV, the I_{BAT} drops at the cut-off (the charging process ends) when the V_{BAT} rises to the specification value of the V_H.

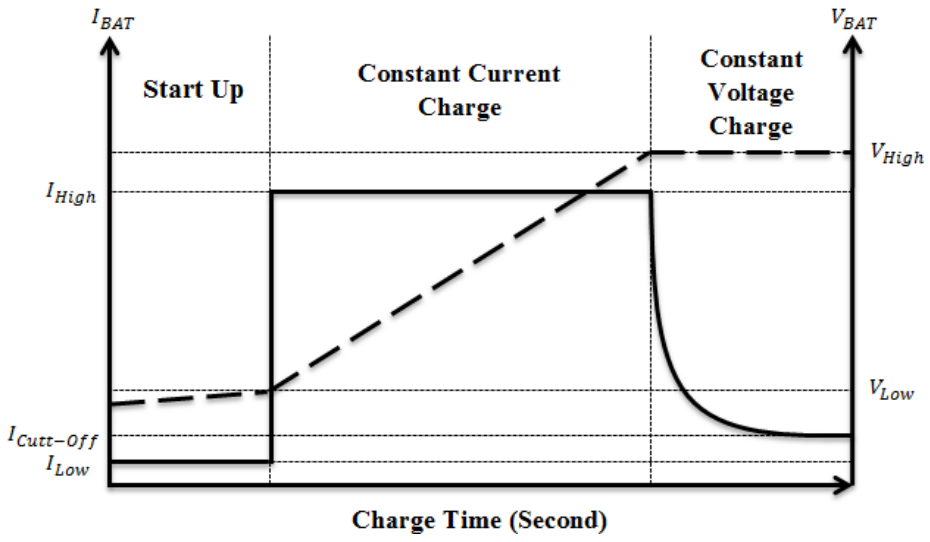


Figure 1. Li-Ion battery charging modes using the PC technique

This paper focuses on the design of a SPS-based charger (mass charger), which is well suited for operation between CC mode and CV mode by the pulse control (PC) technique to achieve high efficiency and to ensure that the battery is quickly fully charged. We presented this article at the following: section 2 presents our proposed charger design using the PC technique; section 3 presents the simulation results of our charging circuit; and we conclude in section 4.

2. PROPOSED CHARGER DESIGN USING THE PULSE CONTROL TECHNIQUE

The high efficiency, the large output current and also the constant output supply voltage are the most important results to be achieved in the design and modelling of a Li-Ion BCI using Taiwan Semiconductor Manufacturing Company 180 nm complementary metal oxide semi-conductor technology (TSMC 180 nm CMOS) technology. To achieve a solution of the low efficiency, low output current and an instable output supply voltage that is the big problem for many researchers in this field, we proposed a new charger design using the PC technique illustrated in Figure 2. It depends of pulse width modulation (S_{CC}) signal who is acting in CC charge mode and pulse frequency modulation (S_{CV}) signal who is acting in CV charge mode. That makes balancing the efficiency between the batteries charging procedure. Also the automatic selection between S_{CC} and S_{CV} is ensured by the use of logic circuits with the reduction of the conversion loss and ensuring the average efficiency.

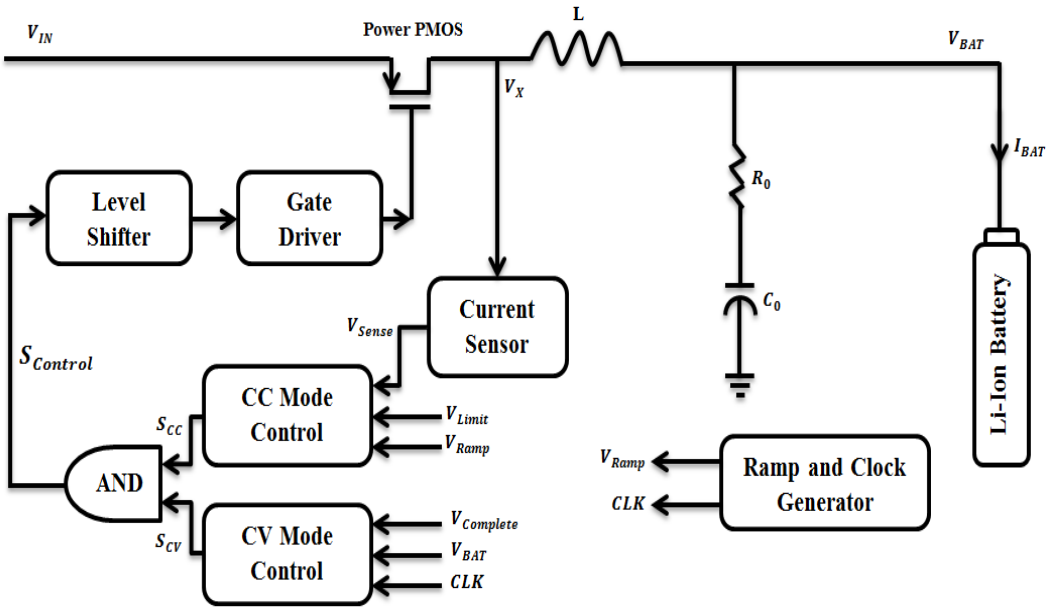


Figure 2. The proposed design of the Li-Ion BCI using PC technique

At startup, the S_{CV} signal is initially set to its maximum charge ratio to ensure that the charger operates in CC charging mode and not in CV charging mode. When the battery is empty, the I_{BAT} increases rapidly with the increasing S_{CC} signal until the I_{BAT} reaches the current limit I_{Limit} as shown in Figure 3. The I_{BAT} will gradually decrease if the S_{CC} signal is maintained at the same level due to the gradual increase in the V_{BAT} as shown in Figure 4. Therefore, the I_{BAT} remains stable, depending on the slow increase of the S_{CC} signal.

The duty-cycle of the CC-CV begins to reduce whenever the V_{BAT} approximates the V_{Limit} as shown in Figure 5. V_{BAT} and I_{BAT} reach V_{Limit} and I_{Limit}, respectively, when the S_{CV} is exactly the same as the S_{CC}. The duty-ratio of S_{CV} remains the same to keep the VBAT constant, while the I_{BAT} gradually decreases and also the duty-ratio of S_{CC} continues to increase and eventually saturates as illustrated in Figure 6. The proposed charger design of Li-Ion BCI using PC Technique is illustrated in Figure 2 which includes six sub-circuits: the CC mode-control block, the CV mode-control block, the current-sensor, the level-shifter, the gate-driver and the Ramp-clock generator.

The CC mode is activated to set the signal S_{CC} by the comparison between the predefined limit voltage V_{Limit} and the sensing voltage V_{Sense} which is generated by the current sensor block. In addition The

CV mode is activated to set the signal S_{CV} by the comparison between the V_{BAT} and the predefined complete voltage $V_{Complete}$, it ensures the regulating of the V_{BAT}. To select either the S_{CC} or the S_{CV} as the $S_{Control}$ signal, an AND logic gate is used. The operating principle of each block has been described.

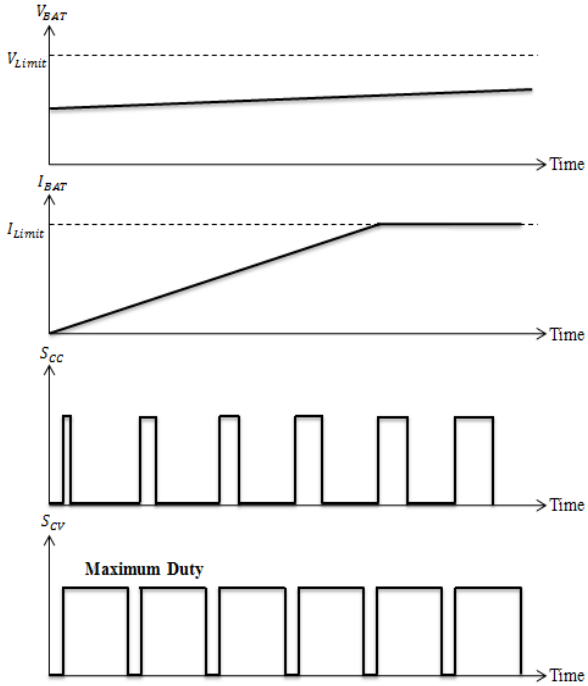


Figure 3. Curve forms of the V_{BAT}, I_{BAT}, S_{CC} signal and S_{CV} signal in start-up charge mode

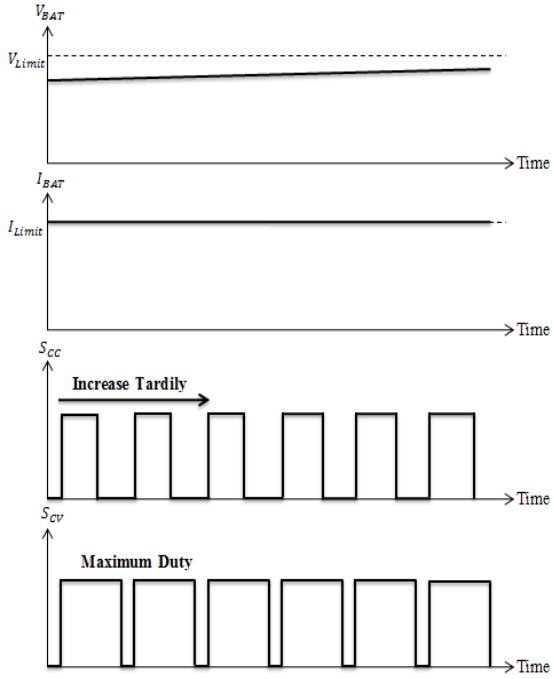


Figure 4. Curve forms of the V_{BAT}, I_{BAT}, S_{CC} signal and S_{CV} signal in CC charge mode

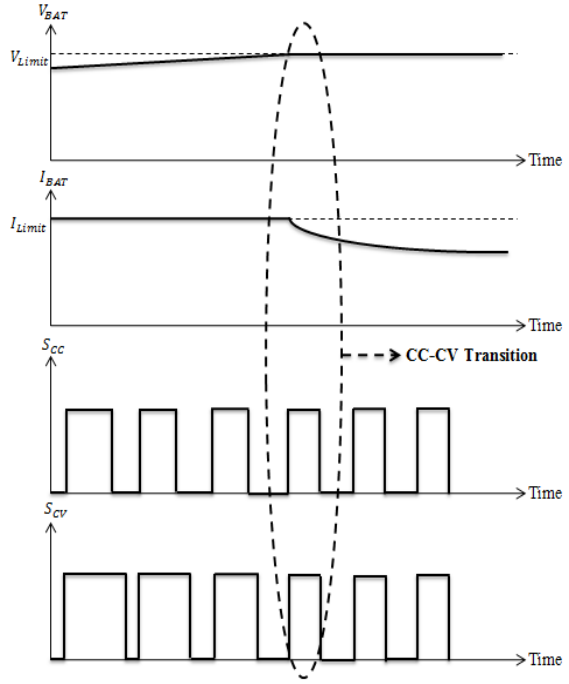


Figure 5. Curve forms of the V_{BAT}, I_{BAT}, S_{CC} signal and S_{CV} signal in transition between CC and CV charge modes

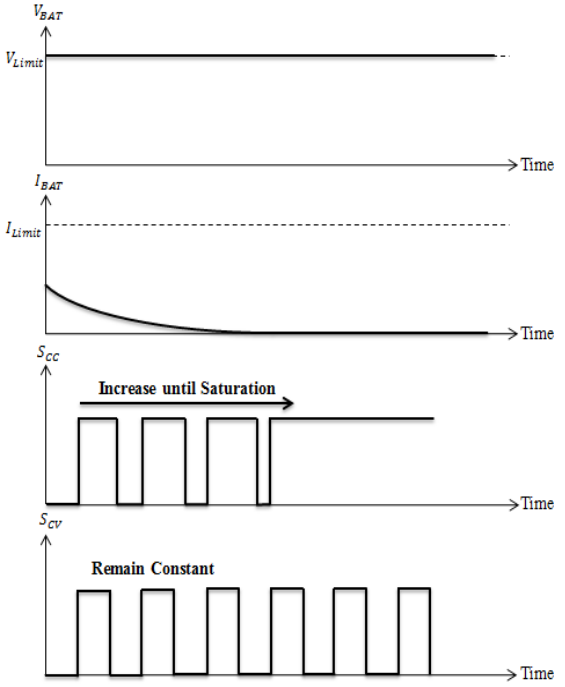


Figure 6. Curve forms of the V_{BAT}, I_{BAT}, S_{CC} signal and S_{CV} signal in CV charge modes

2.1. The CC mode control block

Figure 7 shows the schematic of the CC mode control block. The high speed comparator used in the input of the block to compare between V_{Sense} and V_{Limit}. Then, the Bascul-D uses as input the high-speed comparator and the descending fronts of the $S_{Control}$ signal to trigger it. The proper comparison results are assured by the use of the Bascul-D logic gate. The charging or discharging the C_{CC} capacitor is provided by a pair of current-source and sink-pairs that are controlled by Q and NOT Q which are the outputs of the Bascul-D logic gate.

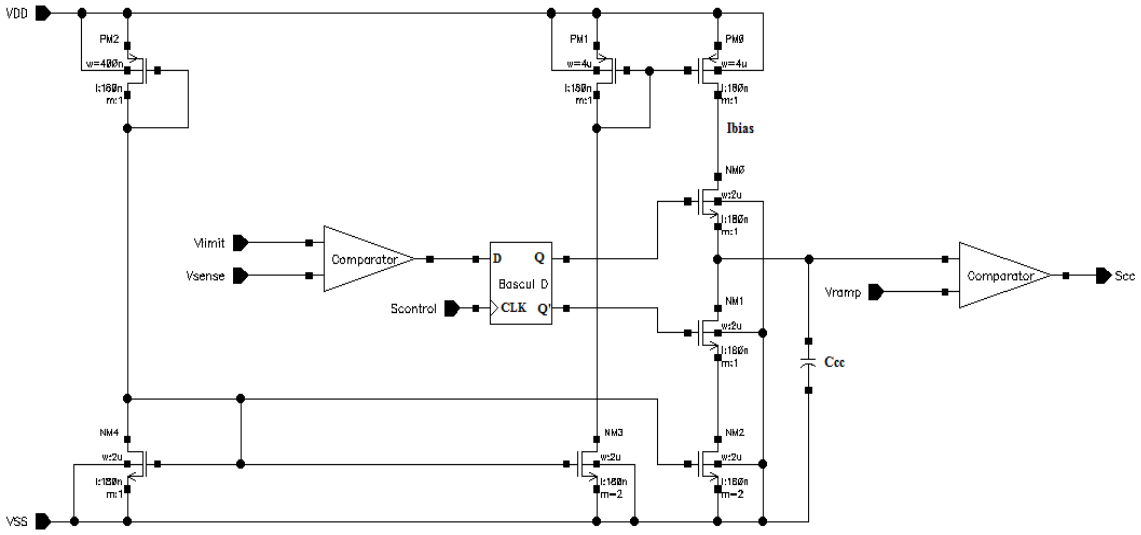


Figure 7. Schematic of the CC mode control block

Also, the use of a second high-speed comparator in the output of the CC mode control block allows determining the duty cycle of the S_{CC} signal by comparing the C_{CC} capacitor voltage V_{CC} with a sawtooth waveform V_{Ramp}. Finally, the start-up function is also performed by the control unit in CC mode control block, because the V_{CC} is charged by the I_{Bias} from zero, so that it also gradually increases from zero, for that, the increase of the C_{CC} or the decrease of I_{Bias} makes the prolongation of the start-up time. The increase rate of V_{CC} can be expressed by the (1):

$$\frac{dV_{CC}}{dt} = \frac{I_B}{C_{CC}} \quad (1)$$

2.2. The CV mode control block

Figure 8 illustrates the circuit of the CV mode block. The charger is confronted with a light charging scenario when the V_{BAT} is about equal to the value of the $V_{Complete}$. However, the S_{CV} will be selected in front of the S_{CC} by using an AND logic gate as illustrated in Figure 2, this allows to maintain the light load efficiency. The high speed comparator used in the circuit to produce a low and high logic level. It produces a low logic level when either S_{CV} equals the clock signal (CLK) in case the V_{BAT} does not reach the $V_{Complete}$. On the other hand, it produces a high logic level when the V_{BAT} and the $V_{Complete}$ are equal to cover CLK by S_{CV}. The power p-channel metal-oxide semiconductor (power-PMOS) is turned off due to the long operating cycle of the high-signal S_{CV}.

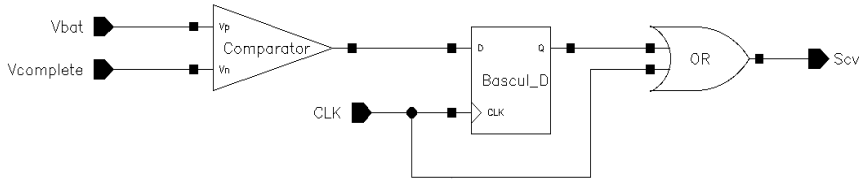
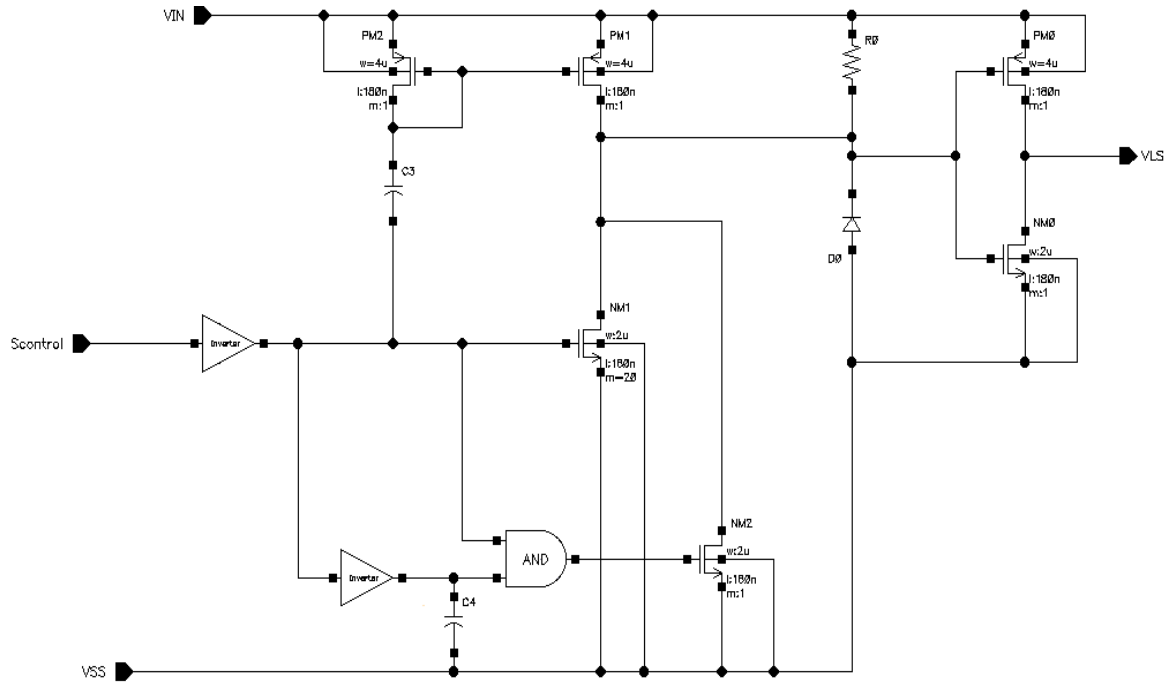


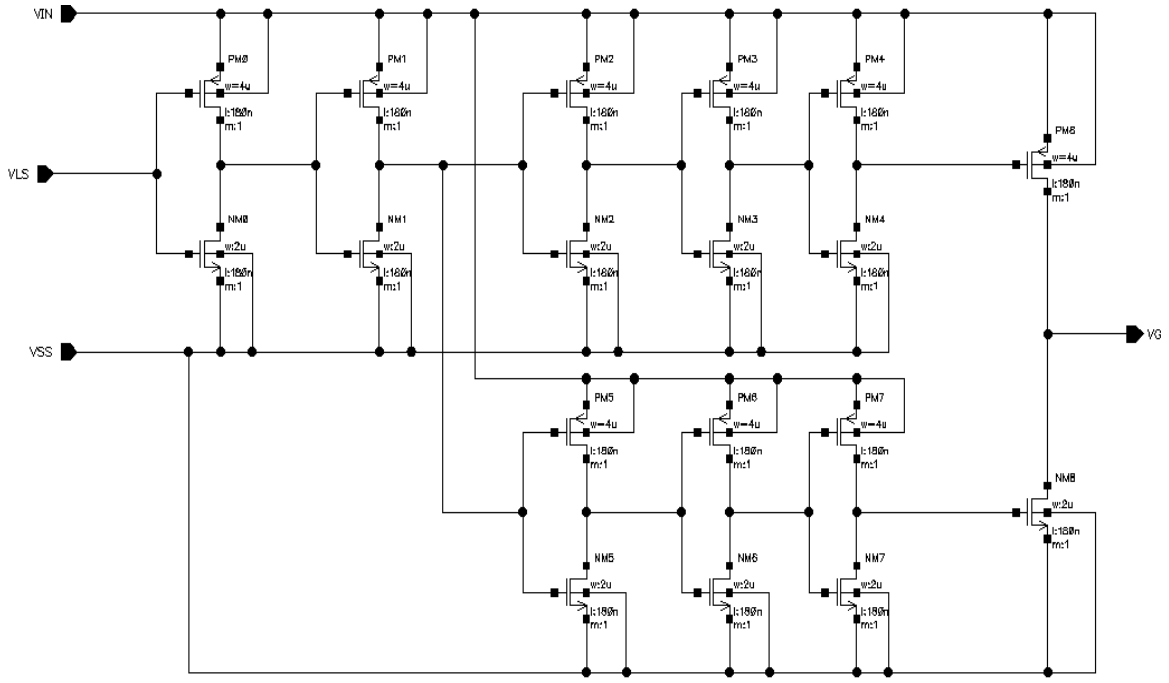
Figure 8. Schematic of the CV mode control block

2.3. The level shifter and gate driver blocks

The level-shifter block is used to switch from the low-voltage of the $S_{Control}$ to a higher-voltage to drive the power-PMOS. Its circuit is illustrated in Figure 9(a). In addition, the gate-driver block is attached to the gate of the power-PMOS which feeds the battery charge through the switching action and the convenient value of current is then regulated in the battery. Its circuit is illustrated in Figure 9(b). The level-shifter, in combination with the gate-driver, provides an ascent time of about 36 picoseconds, a descent time of about 36 picoseconds, and a propagation time of about 0.25 nanoseconds [20].



(a)



(b)

Figure 9. Circuit illustration: (a) schematic of the level-shifter block and (b) schematic of the gate-driver block

2.4. The current sensor block

The OpAmp is used in the circuit as illustrated in Figure 10 to maintain the drain-voltage (V_D) of the PMOS-transistor (PM0) constant and equal to the V_{BAT}. In addition, the PMOS transistor (PM0) used in the design as a load current-sensor. This block is used to generate the V_{Sense} which is always proportional to the V_{BAT}.

2.5. The ramp and clock block

The circuit of the Ramp and Clock block is illustrated in Figure 11. When the PMOS-transistor (PM0) initialized correctly, the I_{Bias1} loads C_{Ramp}. The high speed comparator in the up of circuit provided a low logic to pull up S_{CLK} when V_{Ramp} reaches the V_H. The NMOS-transistor (NM1) turned "On" when S_{CLK} equal "1" to discharge C_{Ramp}.

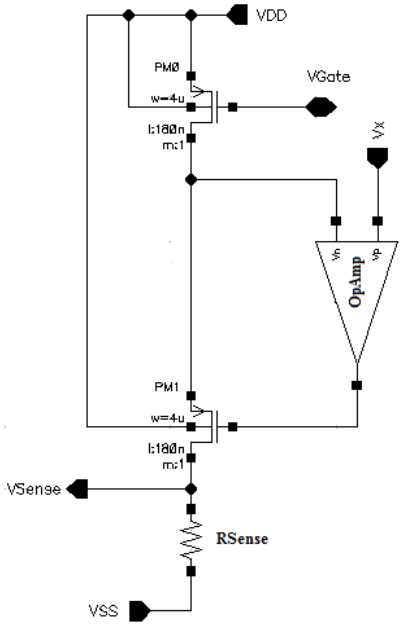


Figure 10. Schematic of the current-sensor block

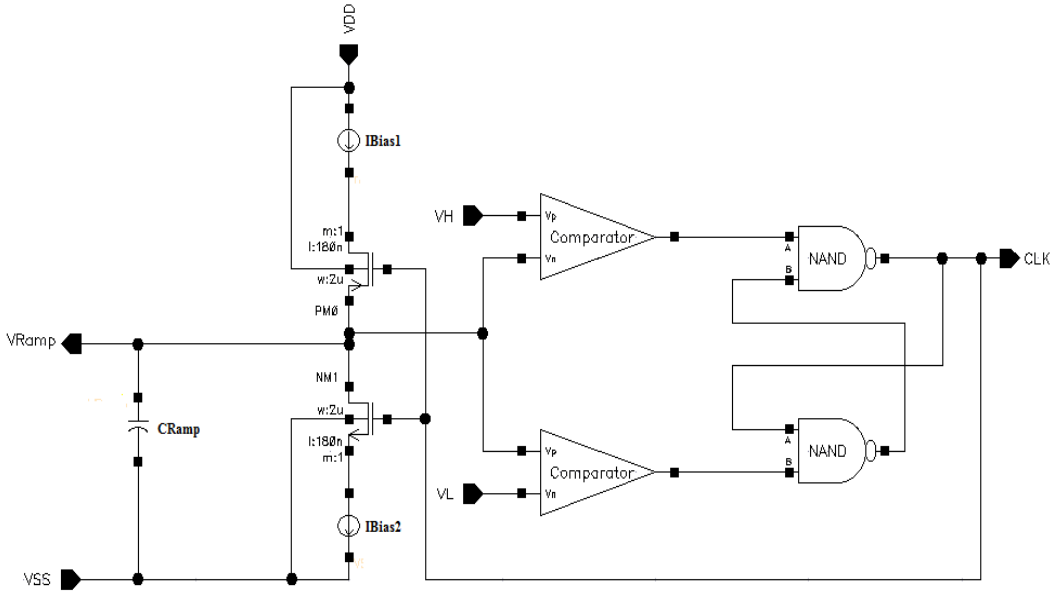


Figure 11. Shematic of the ramp and clock block

Also, the high speed comparator in the down of circuit provided low logic for descent S_{CLK} when V_{Ramp} higher than C_{Ramp} which is also lower than another V_L. So, the Ramp signal S_{Ramp} is desired for the S_{CC} and S_{CV} controls mechanism. The operating cycles are repeated to provide the S_{Ramp} and S_{CLK} signals pending the system is sealed.

3. SIMULATION RESULTS AND LAYOUT

3.1. Simulation

The proposed design of a Li-Ion battery charger interface using the pulse control technique is realized by the TSMC 180 nm CMOS technology under the Cadence Virtuoso software. The selected battery capacity is 5000 mAh in this simulation. The supply voltage V_{IN} is equal to 5 V. The simulation results of the V_{BAT} and the I_{BAT} in each charging mode (start-up, CC and CV) of the proposed charger using PC technique are presented in Figure 12. Also, we can observe from the simulation that the battery charges rapidly in forty-one minutes (2.5 kilo-second).

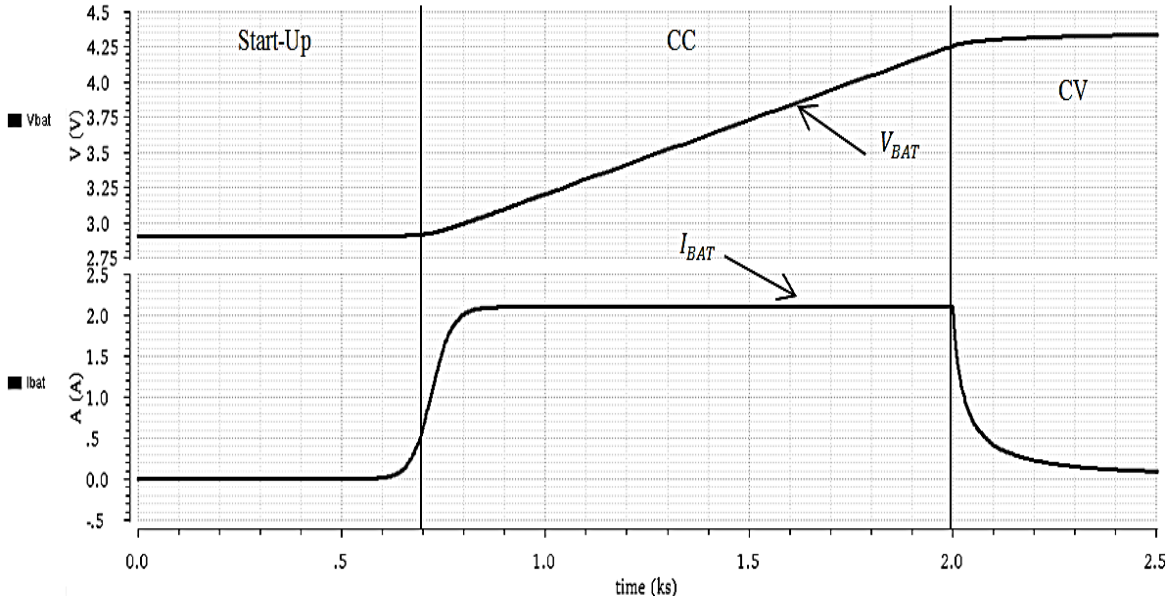


Figure 12. The waveforms of the V_{BAT} and the I_{BAT}

The variable value of the V_{BAT} is about 2.9 V to 4.35 V as illustrated in Figure 13. The I_{BAT} is equal 2.1 A in the CC control mode as illustrated in Figure 14. And also it reaches the $I_{Cut\text{-}off}$ value that equals about 56 mA to terminate the charging procedure. The power efficiency of the proposed Li-Ion BCI using PC technique achieving an efficiency equal 98% of the load current 2.1 A as illustrated in Figure 15. It is determined by (2):

$$\%\text{Efficiency} = \frac{P_{Out}}{P_{In}} \text{ X } 100 \quad (2)$$

with:
P_{Out} : the output power in Watts.
P_{In} : the input power consumption in watts.

3.2. Layout

The layout of the proposed fast charger is shown in Figure 16. A double layer guard ring is used in all circuits susceptible to electromagnetic interference. It is made by respecting the design rules (density, design rule manual (DRM) and mask rule checker (MRC)) and the designer constraint information (cat match, text and constraint manager). It is occupying a total area of 0.1 mm^2. The comparative analysis between the results found and other works/references are summarized in Table 2.

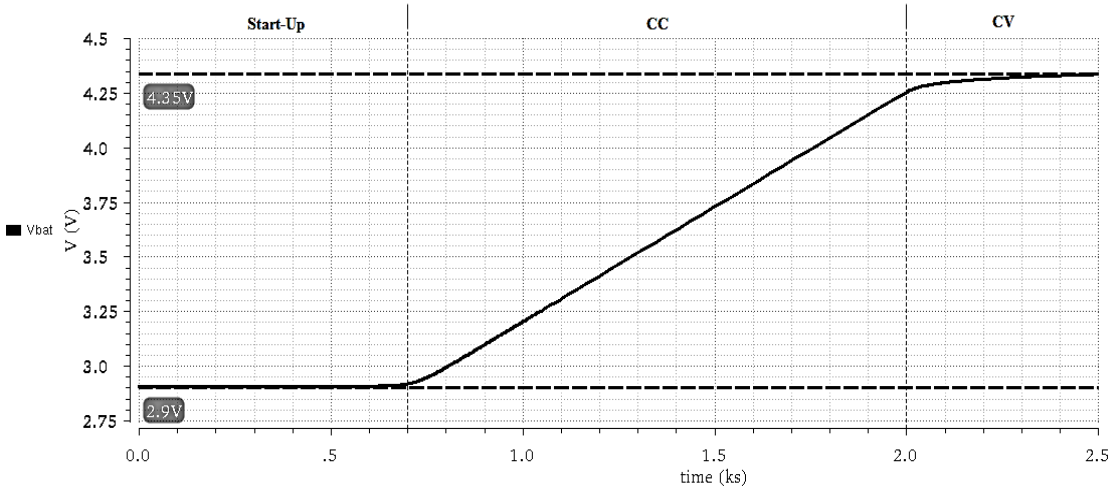


Figure 13. The waveform of the V_{BAT}

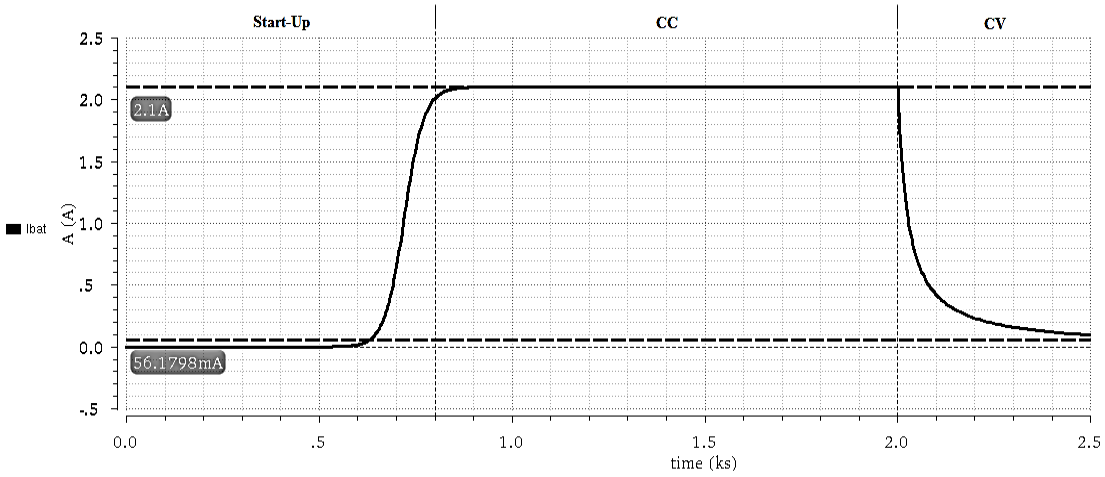


Figure 14. The waveform of the I_{BAT}

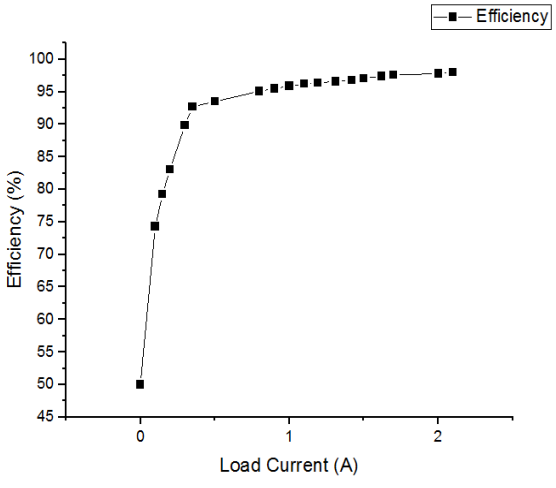


Figure 15. The resulting curve of the power efficiency

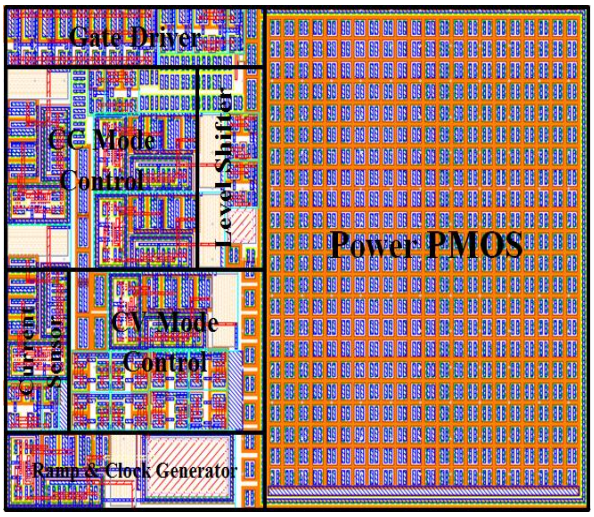


Figure 16. Layout of the proposed Li-Ion BCI using PC technique

Table 2. Comparative analysis

Variable	[2] (2021)	[3] (2021)	[11] (2017)	[21] (2019)	[22] (2015)	[23] (2017)	[24] (2016)	[25] (2017)	This Work
Topology	Switching Based	Switching Based	Switching +LDO	Switching Based	Adaptive LDO	LDO	Switching Based	Switching Based	Switching Based
Technology	TSMC 180 nm CMOS	TSMC 180 nm CMOS	180 nm CMOS	500 nm CMOS	180 nm CMOS	130 nm BICMOS	130 nm BICMOS	350 nm CMOS	TSMC 180 nm CMOS
$V_{IN(max)}$ (V)	4.5	4.2	5.5	8.0-10.0	5	5	16	5.5	5
Output Range V_{BAT} (V)	2.7-4.2	2.7-4.5	2.8-4.2	2.5-4.2	2.5–4.2	3-4.3	2.5-4.2	2.3-4.2	2.9-4.35
$I_{BAT(max)}$ (A)	1.7	1	0.5	1.5	0.448	0.495	1.5	0.6	2.1
Peak Efficiency (%)	97	90.9	87.6	87.4 (CC) 88.6 (CV)	84	83.9	90	92.5	98
Die Size (mm^2)	0.3	1.5	1.62	7.29	1.62	1.41	12.25	2.7126	0.1

4. CONCLUSION

A Li-Ion battery charger interface using the pulse control technique was favorably created and realized in TSMC 180 nm CMOS technology using the Cadence Virtuoso software. The proposed charger provides a battery voltage V_{BAT} ranging from 2.9 V to 4.35 V and a maximum battery current I_{BAT} of 2.1 A at a maximum input voltage V_{IN} of 5 V. The proposed charger provides a full charge in forty-one minutes. The maximum charging efficiency is also 98% and the total area occupies a small size of 0.1 mm^2.

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