# Characterization of electrostatic discharge threshold voltage of phase-shift mask reticle

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# ABSTRACT

A reticle is a stencil used in lithography process for forming integrated circuit (IC) on silicon substrate. It consists of a thin (100 nm) coating of masking metallic patterned (features) with critical dimension (CD) of nanometers on a thicker quartz substrate. The features can be damaged by electrostatic discharge (ESD) when exposed to the environment electrostatic charge and caused deformed IC and eventually device difunctional. Semiconductor equipment materials industry (SEMI) standard established the allowable electrostatic charge on reticle based on the characterization of ESD threshold voltage on binary reticle. However, there is another type of reticle which is phase-shift mask (PSM), has not been characterized for its ESD threshold voltage. A direct current (DC) voltage is applied directly to the structures with CD of 80 nm, 110 nm, and 160 nm. The surface current is recorded at all levels of stress from 1 to 100 V. The current-voltage (IV) curve and physical inspection results for each cell are then reviewed and classified. The results yielded which no electric field induced migration (EFM) defect and breakdown voltage occurred at any of the structures. The cathode's metal work function has been identified as the factor that influences the PSM reticle ESD threshold voltage.

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# 1. INTRODUCTION

A reticle is like a template or stencil which is used in a photolithography process to project a desired pattern onto the wafer surface. There are various types of reticles used during a semiconductor device fabrication such as poly, metal, via, contact, trench, and each reticle has distinctive features for patterning each layer on a wafer surface. A conventional reticle such as a Binary reticle is constructed of a high-purity quartz substrate with thickness approximately 6.35 mm that has a nanometer layer (100 nm) of chromium on the surface which has been etched into patterns called features. For complementary metal–oxide–semiconductor (CMOS) at the technology node of 150 to >250 nm, the process of lithography utilizes a low-resolution optic projector and a Binary reticle to pattern features of 150 nm to >250 nm critical dimension (CD) on the wafer substrate. However, a high resolution optic projector and phase-shift mask (PSM) reticle are used for patterning features of <150 nm CD on a wafer substrate [1]. The reticle is an extremely electrostatic sensitive device and easily damaged by electrostatic discharge (ESD) at low voltage [2]–[4]. Semiconductor equipment materials industry (SEMI) have established guideline for protecting reticle from ESD damaged by tabulating electrostatic charge permissible limit on reticle surface according to technology

node [5], [6]. However, the characterization of ESD threshold voltage by SEMI was performed on Binary reticle of 1000 nm CD. It is important to perform the characterization of ESD threshold voltage on PSM reticle because of different feature's material and lower technology node than Binary reticle. The Binary reticle's features, alignment mark, seal ring, and guard ring are made of chromium or chromium dioxide (Cr/CrO<sub>2</sub>) whereas only the features are made of molybdenum silicide (MoSi<sub>2</sub>) for a PSM reticle [7]. The difference of material in PSM reticle might influence the breakdown voltage and thus the ESD threshold voltage. A breakdown voltage or spark (corona discharged) is a process when the electric field between electrodes is high enough to ionize the insulator, for example air, to become a conducting path and electric current flows through it [8], [9]. However, the breakdown voltage which caused damage to reticle of nanometer CD is at low voltage [10].

Paschen's law and Townsend field emission (corona discharged) are theories that define electrical breakdown voltage between two parallel conductors. Paschen's law defines the breakdown voltage as a simple function of the gas pressure and the electrode spacing of a natural gaseous matter under a constant electric field [11]–[13]. The formula for Paschen's breakdown voltage is,

$$V_b = \frac{Bpd}{\ln[Apd/\ln(1+1/\gamma)]}$$

where p is pressure, d is gap spacing, and  $\gamma$  is the secondary ionization coefficient. The A and B are the coefficients that are associated with the ionization coefficient  $\alpha$ , which is in a molecular gaseous form, and E is the electric field [13].

$$\alpha = Ape^{\left(\frac{-Bp}{E}\right)}$$

In short, the breakdown voltage  $V_b$  is exclusively dependent on the product of pressure (*p*) and electrode gap distance (*d*) [14], [15]. Paschen's law pointed out that at constant pressure, the voltage needed to cause an arc reduces linearly with the gap. Figure 1(a) and 1(b) the Paschen curve voltage breakdown of various gaseous and electrode gap distance.

Figure 1(a) and 1(b) shows the left side curve of Paschen's law where there is a non-linear relationship between breakdown voltage with pd for oxygen and synthetic air. The left side curve is observed to be parabolic as the gap distance gets smaller. With a small electrode gap spacing, the breakdown voltage is influenced by a secondary ionization rather than a gap spacing at constant electrostatic field and pressure [11], [16]. Secondary ionization processes, by which secondary electrons are produced, are the ones which can sustain a discharge after it is established due to ionization by collision and photo-ionization [11]. The main factors that promote secondary ionization are electrostatic field strength and electrode metal work function [17].



Figure 1. The experimental Paschen curve for DC breakdown for several electrode gaps in (a) oxygen and (b) synthetic air [11]

The Townsend field emission is determined by electrostatic field strength and electrode metal work function. The cathode requires a sufficient electrostatic field to ionize the air, and a gap space between electrodes long enough for an avalanche to build up. However, as the gap reduces the excitation energy of the

cathode influences more to cause a breakdown voltage rather than because of the electrostatic field strength. The excitation energy of the electrode is directly proportional to the work function of a metal [17]–[19].

$$E = \frac{\pi\epsilon_0 \Phi^2}{e^3} / \frac{1}{e^3}$$

Where E is the electric field, e is electron charge,  $\mathcal{E}_0$  is the permittivity of the vacuum and  $\phi$  is the work function of metal (nickel electrodes,  $\phi = 4.6 \text{ eV}$  and aluminum,  $\phi = 3 \text{ eV}$ ). Previous findings presented Townsend field emission and vapor arc for electrode gap spacing of <0.1 cm with aluminum electrodes [20]. Similar findings are determined by Dhariwal et al. [17], but the breakdown voltage occurs at smaller gap spacing at approximately <4 um. Hourdakis et al. [18] obtained the breakdown voltage below 10 um electrode gap spacing. The electrodes are a thermally deposited thin film of gold (Au). The work function of gold is 5.0 eV. Strong et al. [19] observed sidewall damages at parallel gold-coated electrodes resulting from extensive breakdown voltage. The electrode gap spacing is evaluated at 40 and 100 um. In conclusion, the breakdown voltage for smaller gap spacing <4 to 10 um is dependent on the electrode material. Electrode with low metal work function requires less energy to produce field emission and influence to cause low breakdown voltage. The Binary reticle's feature is made of chromium (Cr). The Cr work function is 4.5 eV [21]. The PSM reticle's feature is made of molybdenum silicide (MoSi<sub>2</sub>) [21]. The MoSi<sub>2</sub> work function is 4.6 eV [22]. It is expected for the Binary reticle's breakdown voltage to be lower than the PSM reticle since the breakdown voltage is directly proportional to the work function of a metal. In other words, Cr requires less energy to create field emission than MoSi<sub>2</sub>. Therefore, a separate table of permissible limit of electrostatic on reticle surface shall be established for PSM which can be complemented with SEMI current standard.

#### 2. RESEARCH METHOD

There were 2 reticle test plates were prepared for the purpose of characterizing ESD threshold voltage for PSM reticle. One of the reticles (binary reticle) will be used as control of the experiment. The gap width between the spur and border represents the technology node. Gap width is a variable factor which determines reticle ESD threshold voltage measurements. The feature's design for the reticle test plate is shown in Figure 2. The feature design is similar to other researcher design but different dimension of gap distance between spur and border [23]. The body and border size are fixed at 25,000 nm (c, d, and e). The body and border will be used size are wide enough as a test pad for probing. The spur width (b) is fixed at 250 nm to ensure the same corona effect [9]. The gap distance (a) between the spur and Cr border varies according to technology nodes of 80, 110 and 160 nm.



Figure 2. Feature's design for reticle test plate

The feature's parameter of each cell is shown in Table 1. Each cell is separated at 2 mm to avoid induction from stray field generated during probing. The cell is also 2 cm from the edge of reticle which is the reticle contact point to ground.

The reticle test feature design modelling is then transferred into an integrated circuit (IC) layout in graphic database system (GDS) format [24] and later fractured (mask data preparation procedure) into manufacturing electron beam exposure (MEBES) format [24]. Once the MEBES file is ready, it is sent to the reticle manufacturer to print the IC layout onto a quartz substrate to make the reticle. Both reticle test plates were inspected by standard incoming quality before carried out the experiment. The reticle will be subjected to electrostatic direct discharge [25], [26]. The electrostatic direct discharge test procedure is shown in Table 2.

	Column			
Location	A (nm)	B (nm)	C (nm)	
а	80	110	160	R1
b	250	250	250	
с	25000	25000	25000	
d	25000	25000	25000	
e	25000	25000	25000	

Table 1. Cell orientation and dimension of metal lines for reticle test plate

The schematic diagram of the electrostatic direct discharge is shown in Figure 3. An inspection was carried out before and after the electrostatic direct discharge test. The purpose of the inspection was to verify for any defects at the spur and border. A microscope is used to inspect each cell at 100x magnification [25], [26].

Table 2. The test procedures of electrostatic direct discharge test

Step	Procedure
1	Setup the direct discharge tester.
2	Connect positive and negative voltages from HP 4145B semiconductor parameter analyzer to the test probes.
3	Setup HP 4145B Semiconductor Parameter Analyzer with constant current at 100 mA and 0.5 Volts per trigger.
4	Place the reticle test plate on the stage.
5	Move the reticle test plate and put right under the test probe.
6	Align the negative test probe using the positioner jig and microscope. Place it on the border. Then place the positive probe on the body.
7	Ramp voltage from $0 - 100$ Volts at 0.5 Volts step increment.
8	Measure current after each voltage ramp.



Figure 3. The schematic representation of electrostatic direct discharge test

## 3. RESULTS AND DISCUSSION

The R1A cell of the PSM reticle showed a single line structure with 80 nm gap width between spur and border with a spur width of 250 nm. This cell had the smallest gap width from line to chrome border. The images of the pre-inspection for the R1A cell are shown in Figure 4. DC voltages were applied to the body from 0 to 100 V at an incremental step of 500 mV. There was no breakdown voltage that occurred at the R1A cell and also no ESD defects observed after completing the electrostatic discharges up to 100 V. Further tests were continued for R1B and R1C cells and the results yielded similar to R1A cell. A breakdown voltage is observed as current spike at current–voltage (IV) curve. The IV curves for all three cells are shown in Figure 5. Also, the results yielded no ESD defects for R1B and R1C cells which similar to R1A cell. The inspection images for all three cells are shown in Figure 6.







Figure 5. IV Curve of R1A, R1B and R1C cells after completed 100 V electrostatic direct discharge



Figure 6. Post-inspection image of R1A, R1B and R1C cells of PSM reticle

The PSM reticle with  $MoSi_2$  features has influenced the breakdown voltage result because of its metal work function higher than Cr of Binary reticle [13]. Similar tests were then conducted on the R1A, R1B and R1C cells using the Binary reticle test plate (control) to validate the results obtained at the PSM reticle. The IV curve results and ESD defects of cell R1A are shown in Figure 7.

There were 3 stages of ESD defect transformations seen. The first ESD defect was the metal diffusion stage (electric field induced migration (EFM) Type 1) which occurred at ~48.5 V [23]. The metal from the cathode (spur) started to diffuse after the breakdown voltage. The metal diffusion stage is shown as

a linear curve as the current increases proportionally to the input voltage. The second ESD defect (EFM Type 2) was transformed at ~77.5 V [23]. The cathode's metal completely diffused into the border and formed a metal bridge (EFM Type 2). It is represented as the tip of the curve. The third ESD defect was transformed at ~78.5 V when the metal bridge vaporized [27]. After completing the electrostatic discharge test, the R1A cell was re-inspected by using a microscope at multiple magnifications ranging from 50x to 500x to verify the ESD defects at the spur and border. The ESD defect image showed there were 3 locations in which vaporized metal occurred. The rainbow of colors emerged at these locations because the photoresist layer has peeled off due to the excessive heat after the high current passed through the metal and vaporized it thus resulting in multicolor depositions. The highest degree of vaporized metal was between spur and border. The fuse formation took place at this location before it later became vaporized after high current flew through the fuse. The next test was conducted on a R1B cell. The gap width in between the spur and chrome border was 110 nm with a spur width of 250 nm. The input voltage and output current data during ESD defect transformation were plotted as IV curve as shown in Figure 8.



Figure 7. IV Curve and ESD defects of R1A cell of binary reticle during ESD defect transformation



Figure 8. IV Curve and ESD defects of R1B cell during ESD defect transformation

The current sustained at zero amperes during input voltage which was then ramped up from 0 to <74.5 V, indicated that the spur and border were still at their original conditions at that point. However, when the input voltage reached 75.0 V, the current shot-up occurred from zero to 0.17 uA. The sudden shot-up indicated that the R1B cell breakdown voltage threshold was at 75.0 V. When the input voltage continuously increased above 75.0 V, the spur's chrome metal started to diffuse gradually towards the border. The metal diffusion stage occurred when the input voltage continued from 75.5 to 86.5 V until a metal bridge was formed at ~87.5 to 88.0 V. When the input voltage increased beyond 88.0 V, a higher current flew through the fuse formation and burnt it. Based on the IV curve, the fuse was blown at an input voltage of 88.5 V and the current flow stopped. Based on the ESD defect image, the level of metal vaporization was similar to the R1A cell but occurred at 4 locations. The metal vaporized simultaneously since the current started to flow

when a fuse between spur and border was formed. The spur was broken which explained the reason for the output current returning to zero after the metal vaporization occurred after 88.5 V. The last test was conducted on the R1C cell. There was no breakdown voltage after completing electrostatic discharge up to 100 V as expected. It requires a higher input voltage to cause a spark for a 160 nm gap between the spur and border. The voltage breakdown for 160 nm gap width was somewhere in between 100 to 113 V according to recent studies [25]. The electrostatic charge permissible limit on reticle surface for Binary and PSM reticle were extrapolated based on the experiments result and showed in Table 3.

Technology node (nm)	Maximum allowable static charge on binary reticle (V)	Maximum allowable static charger on PSM reticle (V)
30	8	100
40	16	
50	24	
60	32	
70	40	
80	48	
90	55	
100	63	
110	71	
120	79	
130	87	
140	95	
150	103	
160	111	
170	119	NA
180	126	
190	134	
200	142	
210	150	
220	158	
230	166	
240	174	
250	182	

Table 3. The electrostatic charge permissible limit on reticle surface

# 4. CONCLUSION

A review of the literature and experimental data both show that the breakdown voltage across submicron air gaps is influenced by secondary ionization processes. Electrode with low metal work function requires less energy to produce field emission and influence on low breakdown voltage. The IV curves result revealed the breakdown voltage for PSM reticle of 80, 110, and 160 nm metal-metal gap width is above 100 V and it is higher than binary reticle for the same metal-to-metal gap width. Further studies can be carried out to determine PSM reticle ESD threshold voltage by applying direct discharge at higher input voltages. A new separate electrostatic field permissible limit for PSM needs to be established to compliment the readily available guidelines from SEMI which have established the electrostatic field permissible limits for Binary reticles. A revised guideline will help industries to set up production facilities in a more cost-effective manner by implementing appropriate controls based on reticle types and technology node. Apart from this, it will help the industry to prevent losses from remakes or making new sets of reticles due to EFM damages.

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#### REFERENCES

- Q. Wu, Y. Li, Y. Yang, S. Chen, and Y. Zhao, "The law that guides the development of photolithography technology and the methodology in the design of photolithographic process," in 2020 China Semiconductor Technology International Conference (CSTIC), Jun. 2020, pp. 1–6, doi: 10.1109/CSTIC49141.2020.9282436.
- J. Smallwood, "ESD in industry Present and future," *Journal of Physics: Conference Series*, vol. 646, no. 1, Oct. 2015, Art. no. 12018, doi: 10.1088/1742-6596/646/1/012018.
- [3] G. C. Rider, "Current understanding of the electrostatic risk to reticles used in microelectronics and similar manufacturing processes," *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 17, no. 2, Apr. 2018, doi: 10.1117/1.jmm.17.2.020901.

- [4] G. C. Rider, "Why SEMI standard E163 should be followed for the protection of extremely electrostatic-sensitive semiconductors and similar devices during manufacturing, packaging and handling," *Global Journal of Researches in Engineering*, pp. 5–19, Aug. 2020, doi: 10.34257/gjrefvol20is3pg5.
- [5] SEMI, "SEMI: Guide to assess and control electrostatic charge in a semiconductor manufacturing facility E129-0706." pp. 1–39, 2009.
- [6] SEMI E163-0212, "SEMI E163-0212 guide for the handling of reticles and other extremely electrostatic sensitive (EES) Items within specially designated areas," *SEMI Standards*, p. 26, 2012.
- [7] W. Xie, Y. Chen, S. Yu, and Y. Zhang, "Evaluating the process performances of binary, PSM and OMOG masks in advanced technology node," in 2020 International Workshop on Advanced Patterning Solutions (IWAPS), Nov. 2020, pp. 1–3, doi: 10.1109/IWAPS51164.2020.9286801.
- [8] C. Li, T. Lu, Y. Zhang, B. Bai, and X. Li, "Breakdown characteristics of rod-plate electrode under composite AC and DC voltage," in 2020 IEEE International Conference on High Voltage Engineering and Application (ICHVE), Sep. 2020, pp. 1–4, doi: 10.1109/ICHVE49031.2020.9279581.
- [9] T. Y. Wen and J. L. Su, "Corona discharge characteristics of cylindrical electrodes in a two-stage electrostatic precipitator," *Heliyon*, vol. 6, no. 2, Art. no. e03334, Feb. 2020, doi: 10.1016/j.heliyon.2020.e03334.
- [10] J. Montoya, L. Levit, and A. Englisch, "A study of the mechanisms for ESD damage to reticles," IEEE Transactions on Electronics Packaging Manufacturing, vol. 24, no. 2, pp. 78–85, Apr. 2001, doi: 10.1109/6104.930957.
- [11] M. Klas and Š. Matejčík, "DC breakdown in air, oxygen and nitrogen at micrometer separations," in HAKONE 2010 12th International Symposium on High Pressure Low Temperature Plasma Chemistry, 2010, pp. 112–116.
- [12] M. L. Lipham, "Electrical breakdown studies of partial pressure argon under khz range pulse voltages," A thesis submitted to the Graduate Faculty of Auburn University, Auburn, Alabama May 14, 2010.
- [13] A. Peschot, C. Poulain, N. Bonifaci, and O. Lesaint, "Electrical breakdown voltage in micro- and submicrometer contact gaps (100nm - 10μm) in air and nitrogen," *Electrical Contacts, Proceedings of the Annual Holm Conference on Electrical Contacts,* vol. 2015-December, pp. 280–286, 2015, doi: 10.1109/HOLM.2015.7355110.
- [14] J. Knaster and R. Penco, "Paschen tests in superconducting coils: Why and how," *IEEE Transactions on Applied Superconductivity*, vol. 22, no. 3, Art. No. 9002904, Jun. 2012, doi: 10.1109/TASC.2011.2175475.
- [15] K. M. Tofani, N. I. Sinisuka, J.-P. Cambronne, K. Makasheva, and S. Dinculescu, "Methodology for analysis of electrical breakdown in micrometer gaps in tip-to-plane configuration," in 2018 IEEE 13th Nanotechnology Materials and Devices Conference (NMDC), Oct. 2018, pp. 1–4, doi: 10.1109/NMDC.2018.8605855.
- [16] W. J. Carey, A. J. Wiebe, R. D. Nord, and L. L. Altgilbers, "Characterization of Paschen curve anomolies at high P\*D values," in Digest of Technical Papers-IEEE International Pulsed Power Conference, Jun. 2011, pp. 741–744, doi: 10.1109/PPC.2011.6191503.
- [17] J.-M. Torres, M. P. Y. Desmulliez, and R. S. Dhariwal, "Electric field breakdown at micrometre separations in air and nitrogen at atmospheric pressure," *IEE Proceedings - Science, Measurement and Technology*, vol. 147, no. 5, pp. 261–265, Sep. 2000, doi: 10.1049/ip-smt:20000506.
- [18] E. Hourdakis, G. W. Bryant, and N. M. Zimmerman, "Electrical breakdown in the microscale: Testing the standard theory," *Journal of Applied Physics*, vol. 100, no. 12, Art. No. 123306, Dec. 2006, doi: 10.1063/1.2400103.
  [19] F. W. Strong, J. L. Skinner, P. M. Dentinger, and N. C. Tien, "Electrical breakdown across micron scale gaps in MEMS
- [19] F. W. Strong, J. L. Skinner, P. M. Dentinger, and N. C. Tien, "Electrical breakdown across micron scale gaps in MEMS structures," in *Reliability, Packaging, Testing, and Characterization of MEMS/MOEMS V*, Jan. 2006, vol. 6111, Art. No. 611103, doi: 10.1117/12.646508.
- [20] E. Husain and R. S. Nema, "Analysis of paschen curves for air, N2 and SF6 using the townsend breakdown equation," *IEEE Transactions on Electrical Insulation*, vol. EI-17, no. 4, pp. 350–353, Aug. 1982, doi: 10.1109/TEI.1982.298506.
- [21] C. M. Doland, "Molybdenum silicide formation on single crystal, polycrystaline and amorphous silicon: growth, structure and properties," University Of Houston, 1988.
- [22] E. Sugawara and H. Nikaido, "Properties of AdeABC and AdeJJK efflux systems of Acinetobacter baumannii compared with those of the AcrAB-TolC system of Escherichia coli," *Antimicrobial Agents and Chemotherapy*, vol. 58, no. 12, pp. 7250–7257, 2014, doi: 10.1128/AAC.03728-14.
- [23] G. Rider, "Estimation of the field induced damage thresholds in reticles," *ResearchGate*, pp. 1–9, 2004, doi: 10.13140/RG.2.1.2599.6321.
- [24] N. Yao and Z. L. Wang, Eds., Handbook of Microscopy for Nanotechnology. Boston: Kluwer Academic Publishers, 2005.
- [25] A. J. Wallash and L. Levit, "Electrical breakdown and ESD phenomena for devices with nanometer-to-micron gaps," in *Reliability, Testing, and Characterization of MEMS/MOEMS II*, Jan. 2003, vol. 4980, doi: 10.1117/12.478191.
- [26] G. C. Rider and T. S. Kalkur, "Experimental quantification of reticle electrostatic damage below the threshold for ESD," in *Metrology, Inspection, and Process Control for Microlithography XXII*, Mar. 2008, vol. 6922, Art. no. 69221Y, doi: 10.1117/12.760480.
- [27] A. C. Rudack, M. Pendley, P. Gagnon, and L. Levit, "Creating and measuring photomask damage," in *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, 2003, vol. 2003-January, pp. 1–6.

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