International Journal of Electrical and Computer Engineering (IJECE)
Vol. 9, No. 5, October 2019, pp. 4417~4422
ISSN: 2088-8708, DOI: 10.11591/ijece.v9i5.pp4417-4422

Modeling of digital converter for GSM signals with MATLAB

Metodi Traykov[1], Radoslav Mavrevski[2], Ivan Trenchev[3]
[1]Department of Informatics, South-West University "Neofit Rilski", Bulgaria
[2]Department of Electrical Engineering, Electronics and Automatics, South-West University "Neofit Rilski", Bulgaria
[3]University of Library Studies and Information Technologies Sofia, Bulgaria

Article Info

Article history:

Received Mar 18, 2019
Revised Apr 16, 2019
Accepted Apr 25, 2019

Keywords:

Digital converter
GSM signal
MATLAB
Simulation

ABSTRACT

In this study will simulate steady state of Digital Down Convertor (DDC) for GSM signal with a narrow frequency range. The MATLAB model that is described in this article simulates the work of the TIGC4016 Quad Digital Down Converter. This converter is used for digital mixing (down conversion) of signals, narrow band low-pass filtering and decimation. To implementation of the model, we use high sample-rate (69,333 MSPS) bandpass signal. The result contains low sample-rate (270.83 KSPS) baseband signal, thus facilitating the demodulation process.

Corresponding Author:

Radoslav Mavrevski,
Department of Informatics,
South-West University "Neofit Rilski",
66 Ivan Michailov st, 2700 Blagoevgrad, Bulgaria.
Email: mavrevski@swu.bg

1. INTRODUCTION

Digital Down Convertor (DDC) technology is widely used in the telecommunication industry (https://www.mathworks.com/help/dsp/examples/gsm-digital-down-converter.html). DDC converters are often used in cellular phones [1-4]. Generally, the cell phone chip consists of variable frequency amplifiers, a high speed (12 or 14 bits) Analog-to-Digital converter (ADC), and a DDC. These parts are designed for frequencies of 50 MHz to 65 MHz with oscillations, which allow parts of signal to be used at signal frequencies up to 300 MHz. Also, DDC allows program flexibility of frequency and bandwidth in the conversion process. The process of conversion and filtering is digital and linear. Most often DDC is used in a digital I / Q demodulator with a programmable frequency. On Figure 1 we show a block scheme of a digital converter [5-8].

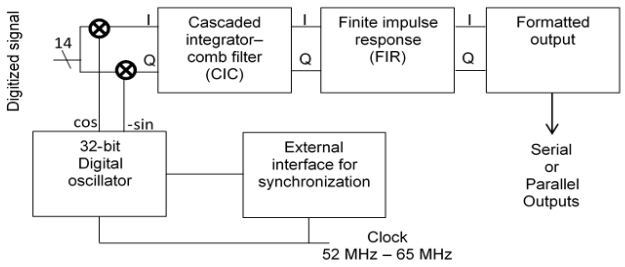


Figure 1. Block scheme of digital converter

2. MATHEMATICAL MODEL

The mathematical model behind the I/Q demodulator is as follows [3, 4, 9-11]:

$$I = F(t)\cos\omega_0 t, \tag{1}$$

$$Q = -F(t)\sin\omega_0 t, \tag{2}$$

Let

$$F(t) = A(t)\,cos(\omega_1 t + \varphi) \tag{3}$$

where A is function of t and the bandwidth is less than ω_0. We substitute equation (3) into the equations (1) and (2) and after simplification, we get the following:

$$I = \frac{A(t)}{2}\{\cos[(\omega_1 - \omega_0)t + \varphi] + \cos[(\omega_1 + \omega_0)t + \varphi]\} \tag{4}$$

and

$$Q = \frac{A(t)}{2}\{\sin[(\omega_1 - \omega_0)t + \varphi] + \sin[(\omega_1 + \omega_0)t + \varphi]\} \tag{5}$$

To remove the frequency component that is due to sum of ω_1 and ω_0, we need to use appropriate digital low-pass filters. The obtained result is as follow [3, 5]:

$$I = \frac{A(t)}{2}\{\cos[(\omega_1 - \omega_0)t + \varphi]\} \tag{6}$$

and

$$Q = \frac{A(t)}{2}\{\sin[(\omega_1 - \omega_0)t + \varphi]\} \tag{7}$$

If $\omega_1 = \omega_0$ in equations (8) and (9), which are the solution for a synchronous I/Q demodulator, we get the following:

$$I = \frac{A(t)}{2}\{\cos[\varphi]\} \tag{8}$$

and

$$Q = \frac{A(t)}{2}\{\sin[\varphi]\} \tag{9}$$

When we calculating the output size, which is a critical parameter for the measurement intensity, we get the following:

$$Mag^2 = I^2 + Q^2 = \frac{A^2(t)}{4}\{\cos^2[(\omega_1 - \omega_0)t + \varphi] + \sin^2[(\omega_1 - \omega_0)t + \varphi]\} \tag{10}$$

which, we can simplify to

$$Mag^2 = \frac{A^2(t)}{4} \tag{11}$$

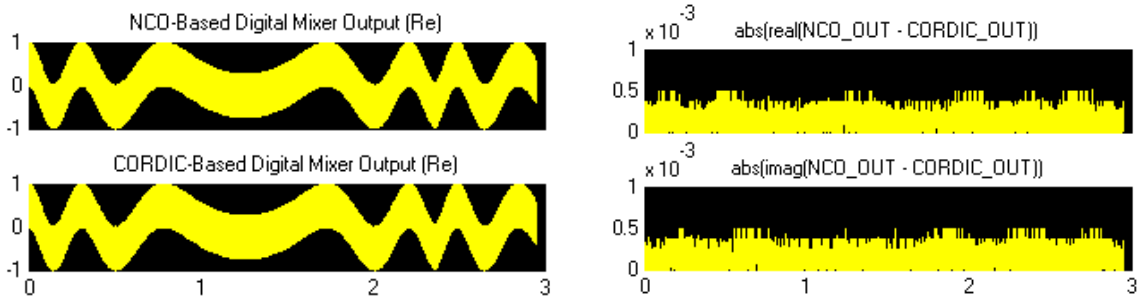
Thus, we can see each small error in the frequency only using the calculations associated with the I and Q, where the frequencies of the I and Q represent the errors frequencies [3, 5, 12-16].

3. RESULTS

For greater accuracy of our simulation we must be sure that the initial (input) and mixed signal contain minimal error. For this purpose we should adjust the values of the normalized frequency registers and registers for normalized phase shift. The values for the normalized frequency registers must be two-component 32-bit integers that represent the normalized range between 0 and the discretization frequency. So we use positive frequency values. The values for the normalized phase shift registers must be 16-bit integers, which also represent the normalized range.

3.1. Comparing the mixer implementations based on numerically controlled oscillator and volder's algorithm

The Mixer Implementations based on Numerically Controlled Oscillator (NCO) and Volder's algorithm generate similarly output values. The Volder's algorithm is also known as COordinate Rotation DIgital Computer (CORDIC). Largely, the choice of Mixer Implementation is based on the available hardware resources. On Figure 2 we show obtained outputs from NCO-based as shown in Figure 2(a) and CORDIC-based as shown in Figure 2(b) Mixer Implementations. NCO-based Mixer works faster but requires more memory, while CORDIC-based Mixer works slower but requires less memory, based on the number of necessary iterations of the CORDIC core.



(a) (b)

Figure 2. Comparing the NCO-based (a) and CORDIC-based (b) Mixer

3.2. Oscillation

To dispel unnecessary frequencies within the available bandwidth, we add the signal oscillations to the accumulator phase values. In our simulation, a signal oscillation is generated by a PN sequences generator that contain shift registers and exclusive OR. When we increase the number of oscillating bits outside the optimum value, the lower bound of noise starts to rise. When we reduce the number of oscillating bits below the optimum value, occur false frequencies that reduce the free dynamic range of the NCO system's false signal as shown in Figure 3.

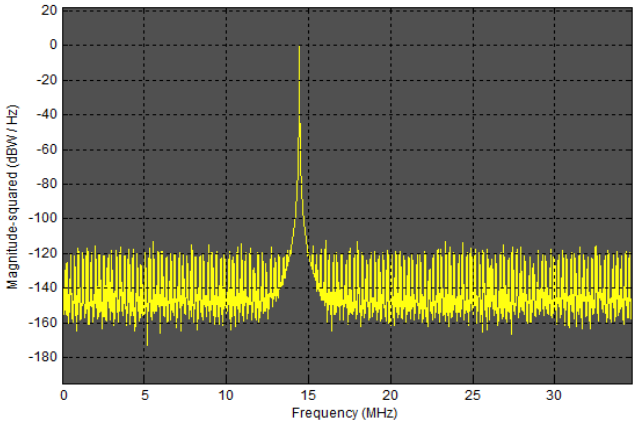


Figure 3. Configuring the NCO-based mixer

3.3. Phase accumulator with oscillator

The phase accumulator with subsystem, which contain oscillator, calculates the input angle θ of the complex rotation function in the CORDIC Mixer as shown in Figure 4. As in the NCO-based mixer, we add an oscillating signal to the value of the phase accumulator in order to dispel the false frequencies within the bandwidth. The oscillating signal is generated by PN generator that contains binary registers for shift and exclusive OR. We choose the number of oscillating bits to be 15 to be as close as possible to the cosine spectrum of an NCO-based Mixer. The complex rotation function in the CORDIC-based Mixer calculates u exp (jθ) using the CORDIC rotation algorithm.

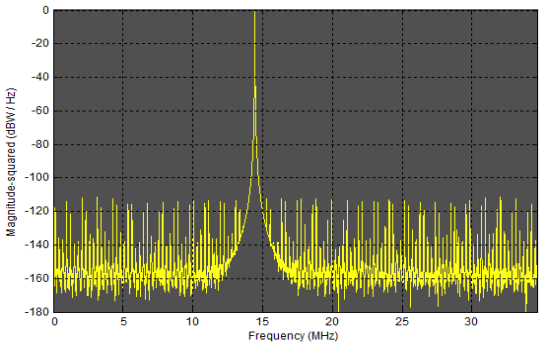


Figure 4. Configuring the CORDIC-based mixer

3.4. Decimation filter

By using integer programing, we realize a decimation filter to perform deciphered filtering within cascading structures. On Figure 5 we show the result, obtained by the realized filter. We use a balancing FIR filter as shown in Figure 6(a) to set the Cascaded Integrated Comb (CIC) filter for bandwidth and a Programmable Finite Impulse Response (PFIR) filter as shown in Figure 6(b) to filter the signal.

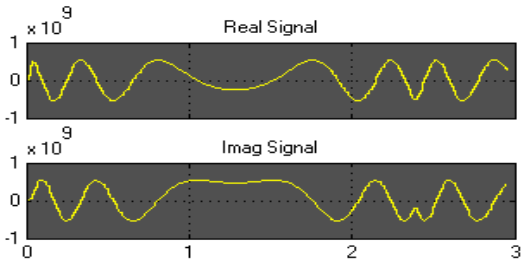
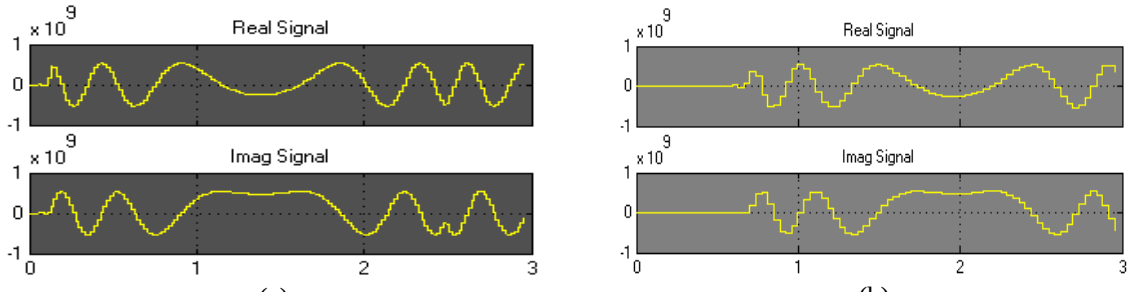


Figure 5. Filtration with decimation filter



(a) (b)

Figure 6. Obtained result by using balancing FIR filter (a) and programmable FIR filter (b)

4. CONCLUSION

When we processing the GSM signal using decomposition with a three-stage filter, we can extract a 200 kHz bandwidth from a 5 MHz input signal and to lower sample rate to the 270.833 Kbps (original sample rate). The first step in this decomposition is a CIC filter with a drop down factor of 64 to introduce 270,833 kHz. At a later stage of filtration we use Compensating Finite Impulse Response (CFIR) to reduce the sample rate to 200 kHz. Thus we satisfy the requirements for GSM. Finally, we use a PFIR to form the frequency of the GSM mask. The methodology, used to design the uniform pulses of a FIR filter is simple and leads to good optimal FIR filters with respect to other methods. The described above technique allows designers to explicitly control the bandwidth edges and the magnitude of relative pulsations for each band.

REFERENCES

[1] T. Powers et. al., "Design, Commissioning and Operational Results of Wide Dynamic Range BPM Switched Electrode Electronics," *Proceedings of the Beam Instrumentation Workshop*, pp. 257-265, 1998.

[2] M. Dehler, et. al., "Digital BPM System for the Swiss Light Source – First Operational Results," *Proceedings of the Beam Instrumentation Workshop*, 1998.

[3] T. Powers, et. al., "Two applications of direct digital down converters in beam diagnostics," *AIP Conf. Proc.* vol. 546, pp. 275, 2000.

[4] J. Gerhardt, et. al., "Digital down Converter optimization," *IEEE 56th International Midwest Symposium on Circuits and Systems*, pp. 1015-1018, 2013.

[5] S. Jasmine and R. Latha, "Design of Digital Down Converter (DDC) for GSM," *IJISET - International Journal of Innovative Science, Engineering & Technology*, vol. 2(10), pp. 860-865, 2015.

[6] K. Uday Kumar, K. Bapayya and M. Sandeep, "FPGA Implementation of Digital Down Converter using Multiplier-Free Filter," *International Journal of Engineering Research & Technology (IJERT)*, vol. 3(10), pp. 648-655, 2014.

[7] S. Majid and A., Faeza, "Design and Implementation of Dual-mode Programmable Decimation Filter for WCDM and GSM Systems," *International Journal of Soft Computing and Engineering (IJSCE)*, vol. 3(6), pp. 168-173, 2014.

[8] S. Majid, H. Abdulsatar, and T. Hasan, "Reconfigurable Down Sampling Channelizer for SDR Receiver Using FPGA," *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, vol. 3(8), pp. 23-27, 2014.

[9] R. Mavrevski, "Selection and comparison of regression models: estimation of torque-angle relationships," *C. R. Acad. Bulg. Sci.*, vol. 67(10), pp. 1345-1354, 2014.

[10] M. Traykov, et. al., "Using partial differential equations for pricing of goods and services," *Scientific Annals of Economics and Business*, vol. 63(2), pp. 291-298, 2016.

[11] Traykov, M., et. al., "Algorithm for protein folding problem in 3D lattice HP model," *International Journal of Biology and Biomedicine*, vol. 3, pp. 16-21, 2018.

[12] R. Mehra and S. Pattnaik, "Reconfigurable Design of GSM Digital down Converter for Enhanced Resource Utilization," *International Journal of Computer Applications*, vol. 57(11), pp. 41-47, 2013.

[13] E. Malki, K. Shehata and A, "Madian, Implementation of optimized Triple-Mode Digital Down Converter for WCDMA, CDMA2000 and GSM of SDR," *22nd International Conference on Microelectronics*, ICM, pp. 395-398, 2010.

[14] Z. Li, Q. Ma and R. Qi, "Design of a programmable digital Down Converter Structure," *Electrical and Computer Engineering, IEEE CCECE 2003, Canadian Conference*, vol. 1, pp. 535-538, 2003.

[15] M. Traykov, et. al., "Risk analysis in the economics through R Language," *WSEAS TRANSACTIONS on BUSINESS and ECONOMICS*, vol. 15, pp. 180-186, 2018.

[16] R. Mavrevski, et. al., "Approaches to modeling of biological experimental data with GraphPad Prism software," *WSEAS TRANSACTIONS on SYSTEMS and CONTROL*, vol. 13, pp. 242-247, 2018.

BIOGRAPHIES OF AUTHORS

Metodi Traykov, Assistant in Department of Informatics, Faculty of Mathematics and Natural Sciences, member of University Center for Advanced, Bioinformatics Research, South-West Uni-versity "Neofit Rilski", 66 Ivan Mihaylov Str., Blagoevgrad, Bulgaria. PhD on Informatics. Scien-tific Interest: programming and bioinformatics. He is one of the organizers of the XXVII REPUBLICAN STUDENT PROGRAMMING OLYMPIAD, 2015, http://bcpc.eu/XXVII/.

Radoslav Mavrevski, Chief Assistant in Department of Informatics, Faculty of Mathematics and Natural Sciences, member of University Center for Advanced, Bioinformatics Research, South-West University "Neofit Rilski", 66 Ivan Mihaylov Str., Blagoevgrad, Bulgaria. PhD on Informatics. Scientific Interest: programming, computer modelling, applied statistics and bioinformatics. He is one of the organizers of the South Eastern European Mathematical Olympiad for University Students (SEEMOUS) with International Participation, 2012, http://seemous2012.swu.bg/ and XXVII REPUBLICAN STUDENT PROGRAMMING OLYMPIAD, 2015, http://bcpc.eu/XXVII/.

Ivan Trenchev, Associate professor in Department of Electrical Engineering, Electronics and Automatics, Faculty of Engineering, member of University Center for Advanced, Bioinformatics Research, South-West University "Neofit Rilski", 66 Ivan Mihay-lov Str., Blagoevgrad, Bulgaria and Associate professor in University of Library Studies and Information Technologies Sofia, Bulgaria. PhD on Informatics. Scientific Interest: virtual reality (VR), computer modelling and bioinformatics. He is one of the organizers of the XXVII REPUBLICAN STUDENT PROGRAMMING OLYMPIAD, 2015, http://bcpc.eu/XXVII/.