A genetic algorithm for the optimal design of a multistage amplifier

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The optimal sizing of analog circuits is one of the most complicated processes, because of the number of variables taken into, to the number of required objectives to be optimized and to the constraint functions restrictions. The aim is to automate this activity in order to accelerate the circuits design and sizing. In this paper, we deal with the optimization of the three stage bipolar transistor amplifier performances namely the voltage gain (AV), the input impedance (ZIN), the output impedance (ZOUT), the power consumption (P) and the low and the high cutoff frequency (FL,FH), through the Genetic Algorithm (GA). The presented optimization problem is of multi-dimensional parameters, and the trade-off of all parameters. In fact, the passive components (Resistors and Capacitors) are selected from manufactured constant values (E12, E24, E48, E96, E192) for the purpose of reduce the cost of design; also, the intrinsic parameters of transistors (hybrid parameters and the junction capacitances) are considered variables in order not to be limited in design. SPICE simulation is used to validate the obtained result/performances.

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1. INTRODUCTION

Despite the strong trend towards integrated circuits, discrete components are still used in analog design especially for circuits that are not produced in large quantities. Discrete components such as Resistors (R) and Capacitors (C) are produced according to the industrial series such as E12, E24, E48, E96 or E192. To reduce costs and make the design faster, discrete components are selected according to values constants of the previous series. An exhaustive search of all possible combinations of values for selection of an optimized design is not always feasible.

On other hand, almost all the design of analog circuits has been oriented towards MOS transistorbased circuits mainly due to their low power consumption. Studies that address the sizing of circuits based on bipolar transistors remain very scarce although they have better speed (switching times) and wider bandwidths [1]. In addition, these studies deal with design considering the intrinsic parameters of bipolar transistors as fixed, such as the works [2, 3] where an usual analog circuits are sized in which the current gain (β) and the base- emitter and base-collector junction capacitances (C π) and (C μ) are considered as fixed which limits the design and subsequently reduces the performance of these circuits.

In order to overcome the aforementioned difficulties and limitations, an intelligent and efficient optimization technique requires short computation time with high accuracy, must be used. Methods based on the use of Meta-heuristics appeared then to resolve complex optimization problems, they always offer

approximate solutions for optimization problems at a very reasonable times [4]. They are used in many engineering problems such as Scheduling Problem [5], Vehicle Routing Problem [6], Language Recognition System [7] etc.

Some Meta-heuristics are used by the analog designers to solve the design problems of integrated circuits and also of discrete component systems, such as Simulated Annealing (SA) [8], Genetic Algorithms (GA) [9], Tabu Search (TS) [10], Particle Swarm Optimization (PSO) [11], Ant Colony Optimization (ACO) [12-14] and Artificial Bee Colony (ABC) [15-17].

In this work, we propose the use of the Genetic Algorithm (GA), known by its effectiveness of optimization, for the optimal sizing of three stages bipolar transistor amplifier. SPICE simulations are given to show the validity of obtained results. The rest of the paper is organized as follows: The second part gives an overview on the principle of the genetic algorithm. The third part deals with the application of the proposed algorithm to the optimal design of a three stages bipolar transistor amplifier. The fourth part shows the results of the optimal sizing. Finally, the fifth section, followed by a conclusion, presents how to set SPICE parameters and shows the simulation results.

2. GENETIC ALGORITHM

The GA find their origins in the biological processes of survival and adaptation. Its principle consists of sampling a population of potential solutions. A population of individuals is, initially, randomly generated. The GA performs then operations of selection, crossover and mutation on the individuals, corresponding respectively to the principal of survival of the fittest, recombination of genetic material and random mutation observed in nature [18]. The optimization process is carried out through the generation of successive populations until a stop criterion is met. The flowchart in Figure 1 provides an overview of a GA procedure [18].



Figure 1. Flowchart of a GA

There are therefore 6 elements necessary for the running of the GA [18]:

- 1. We begin the process of fitting the problem to a GA by defining a chromosome as an array of variable values to be optimized.
- 2. The user must fix a priori the sizing parameters of the algorithm, in particular the size of the population and the number of generations (which is very often used as a condition for stopping the algorithm).

- 3. Then the Generation of the initial population (set of possible solutions) can be random or from known approximate solution(s).
- 4. Each chromosome has a cost found by evaluating the cost function f at the variables. The higher this cost, the greater is the chance of an individual (solution) being selected for reproduction.
- 5. Now is the time to decide which chromosomes in the initial population are fit enough to survive and possibly reproduce offspring in the next generation, the costs and associated chromosomes are ranked from lowest cost to highest cost. The rest die off.
- 6. Then recombination/reproduction is achieved through two genetic operators, namely crossover and mutation.
 - Crossover that combines (mates) two chromosomes (parents) to produce a new chromosome (offspring). The idea behind crossover is that the new chromosome may be better than both of the parents if it takes the best characteristics from each of the parents.
 - Mutation is usually considered as an auxiliary operator to extend the search space and causes release from a local optimum when used cautiously with the selection and crossover systems.

Operations of selection, crossover, and mutation are repeated until a favorable number of individuals for the new generation is created, and the objective function is calculated again for all of the individuals in the new generation. The best individual in the new generation according to its fitness is kept to continue to the next generation. Thus, the fitness of the entire population will be decreased with the reproduction of the generation.

In the literature, the number of application studies of the GA technique is uncountable and the fields of application are very diverse. These include for example: Power Supply System [19], Electric Vehicles [20], Traffic Light Signal Parameters Optimization [21], Dynamic Optimization Problems [22], Resolution university course schedules [23], Power factor improvement in the industry [24], etc. In the following, we present an application of the GA to the optimal design of a three-stage amplifier.

3. APPLICATION: THREE-STAGE BIPOLAR TRANSISTOR AMPLIFIER CIRCUIT

We propose in this section, the optimal sizing of three stage bipolar transistor amplifier. The schematic of this amplifier is given in Figure 2.



Figure 2. The three-stage amplifier

According to the study of the equivalent circuit of this amplifier in small signals in the mid band where all the capacitances are neglected, we have obtained the following equations for A_V , Z_{IN} and Z_{OUT} : The voltage gain:

$$A_{V} = -\frac{R(\beta_{3}+1)R_{th1}R_{th2}\beta_{2}(\beta_{1}+1)}{h_{11}'(h_{11}' + R(\beta_{3}+1) + R_{th2})(h_{11} + R_{th1}(\beta_{1}+1))}$$
(1)

With:

$\mathbf{R}_{\mathbf{B}2} = \mathbf{R}_3 \ \mathbf{R}_4$	(2)
$\mathbf{R}_{\mathbf{B}3} = \mathbf{R}_5 \ \mathbf{R}_6$	(3)
$\mathbf{R}_{\mathbf{I}\mathbf{I}} = \boldsymbol{\rho} \ \mathbf{R}_{\mathbf{E}\mathbf{I}}$	(4)

$$\mathbf{R}_{12} = \rho' \| \mathbf{R}_{C2} \tag{5}$$

$$\mathbf{R} = \boldsymbol{\rho}^{"} \| \mathbf{R}_{\mathrm{E3}} \| \mathbf{R}_{\mathrm{L}} \tag{6}$$

$$z_{e2} = R_{B2} | \dot{h_{11}}$$
 (7)

$$R_{th1} = R_{II} \| z_{e2} \tag{8}$$

$$\mathbf{R}_{\mathrm{th2}} = \mathbf{R}_{\mathrm{I2}} \| \mathbf{R}_{\mathrm{B3}} \tag{9}$$

 h_{11} , ρ , β_1 are the hybrid parameters for the first transistor, h'_{11} , ρ' , β_2 for the second transistor and h''_{11} , ρ'' , β_3 for the third transistor.

The input impedance:

$$Z_{IN} = R_{B1} \left[h_{11} + \left(R_{B2} \| R_{II} \| h_{11} \right) (\beta_1 + 1) \right]$$
(10)

With:

$$R_{B1} = R_1 ||R_2 \tag{11}$$

The output impedance:

$$Z_{OUT} = R_{I3} \frac{\left(R_{II} \| R_{B2}\right) + h_{11}^{''}}{\beta_3 + 1}$$
(12)

With:

$$R_{I3} = R_{E3} \rho''$$
 (13)

An estimate for the lower cutoff frequency for an amplifier with multiple coupling and bypass capacitors is given by the sum of the reciprocals of the "short-circuit" time constants:

$$F_{\rm L} \cong \frac{1}{2\pi} \sum_{i=1}^{5} \frac{1}{R_{iS}C_i}$$
(14)

Where R_{iS} is the resistance at the terminals of the i^{th} capacitor with all the other capacitors are shorted, in our case we have:

$$R_{1S} = RBl((h_{11} + R_{thl}(\beta_1 + 1)))$$
(15)

$$R_{2S} = z_{e2} + \left(R_{II} \left\| \frac{h_{11}}{\beta_1 + 1} \right) \right)$$
(16)

$$R_{3S} = R_{E2} \left\| \left[\left(R_{II} \| R_{B2} \right) + h_{11}^{'} \right] \frac{\left(R_{C2} \| z_{e3} \right) + \rho^{'}}{1 + \frac{\rho^{'} \beta_{2}}{\left(R_{II} \| R_{B2} \right) + h_{11}^{'}}}$$
(17)

$$R_{4S} = R_{12} + \left[R_{B3} \left\| \left(h_{11}^{"} + R(\beta_3 + 1) \right) \right]$$
(18)

$$R_{5S} = R_{L} + \left(R_{13} \left\| \frac{R_{th2} + h_{11}^{"}}{\beta_{3} + 1} \right)$$
(19)

With:

$$z_{e3} = R_{B3} \left\| \left(h_{11}^{"} + R_{L3} (\beta_3 + 1) \right) \right\|$$
(20)

The small signal equivalent circuit at high frequencies is as bellow in Figure 3:



Figure 3. Equivalent circuit of a transistor at high frequencies

At high frequencies, impedances of coupling and bypass capacitors are small enough to be considered short circuits. Open-circuit time constants associated with impedances of device capacitances are considered instead.

The higher cutoff frequency:

$$\omega_{\rm H} \simeq \frac{1}{\sum_{i=1}^{6} R_{i0} C_i}$$
(21)

$$F_{\rm H} = \frac{\omega_{\rm H}}{2\pi} \tag{22}$$

Where R_{io} is resistance at terminals of ith capacitor Ci with all other capacitors open-circuited, for our circuit we have:

$$R_{C_{\pi 1}} = \frac{h_{11}(r_{x1} + R_{th1})}{r_{x1} + h_{11} + R_{th1}(\beta_1 + 1)}$$
(23)

$$R_{C_{\mu l}} = \frac{r_{xl}(h_{1\,l} + R_{thl}(\beta_l + 1))}{r_{xl} + h_{1\,l} + R_{thl}(\beta_l + 1)}$$
(24)

$$R_{C_{\pi 2}} = \left[\left(R_{II} \| R_{B2} \right) + r_{x2} \right] | \mathbf{h}_{11}'$$
(25)

$$R_{C_{\mu2}} = R_{C_{\pi2}} + \left(R_{I2} \| z_{e4} \right) \left(1 + \frac{R_{C_{\pi2}} \beta_2}{h_{11}} \right)$$
(26)

A genetic algorithm for the optimal design of a multistage amplifier (El Beqal Asmae)

$$R_{C_{\pi3}} = \frac{h_{11}^{"}(r_{x3} + R_{th2}) + R}{r_{x3} + h_{11}^{"} + R_{th2} + R(\beta_3 + 1)}$$
(27)

$$R_{C_{\mu3}} = \frac{h_{11}^{"} + R(\beta_{3} + 1)}{1 + \frac{h_{11}^{"} + R(\beta_{3} + 1)}{r_{x3} + R_{tb2}}}$$
(28)

With:

$$z_{e4} = h_{11}^{"} + R(\beta_3 + 1)$$
⁽²⁹⁾

To have a maximum excursion of the output signal, we should check the following constraint for all the transistors and the power consumption equation is expressed in (31).

$$V_{CE} = \frac{V_{CC}}{2}$$
(30)

$$P = 3 \frac{V_{CC}}{2} I_C + I_C^2 (R_{E1} + R_C + R_{E2} + R_{E3})$$
(31)

The decision variables are the resistors, the capacitors, the hybrid parameters of the transistors and the supply voltage V_{CC} , they present the chromosome of our GA, and the discrete components must have a value of the standard series (E12, E24, E48, E96, and E192).

4. RESULT AND DISCUSSION

The collector current at the Q-point I_C is fixed at 0.5mA. The studied algorithm parameters are given in Table 1. The optimization technique works on MATLAB codes and the circuit is simulated in SPICE to obtained frequency response.

	Table 1. GA para	imeters	
Population size	Selection Probability	Mutation Probability	Generation
900	0.5	0.0001	1000

The serial components values are calculated as follows:

 $\mathbf{R}_{i} = \mathbf{p}_{i} \times 100 \times 10^{\mathbf{q}_{i}} \,\Omega \tag{32}$

$$C_i = r_i \times 100 \times 10^{s_i} F$$
 (33)

Where [p, q, r, s] are real numbers that are the design variables for each ith component.

The following two tables present the different optimal values given by the application of the genetic algorithm. The Table 2 presents the optimal values of the hybrid parameters and the supply voltage. The Table 3 presents the optimal values, linear and those following the different series, of resistors and capacitors forming the studied amplifier. The Table 4 gives the corresponding performances to optimal values presented in the Table 2 and Table 3. According to the results in Table 4, we notice that the performances are almost the same for all series with a slight advantage for the series E192 which presents the best gain Av and the best higher cutoff frequency $F_{\rm H}$.

Table 2. Optimal values for hybrid parameters										
	β_1	β_2	β3	ρ(Ω)	ρ' (Ω)	ρ" (Ω)	$h_{11}\left(\Omega\right)$	$h'_{11}\left(\Omega\right)$	$h''_{11}(\Omega)$	V _{CC} (V)
Linear values	300	103	192.41	1038	1085.88	1623.55	1516.66	1856.58	1435.28	5

		Table 3. Opti	mal values of F	R and C		
	Linear values	E12	E24	E48	E96	E192
R1 (KΩ)	44.85	47	43	44.2	45.3	44.8
R2 (KΩ)	68.87	68	68	68.1	68.1	69
R3 (KΩ)	45.50	47	47	46.4	45.3	45.3
R4 (KΩ)	72.10	68	75	71.5	71.5	72.3
R5 (KΩ)	41.30	39	43	42.2	41.2	41.2
R6 (KΩ)	85.73	82	82	86.6	86.6	85.6
RC2 (KΩ)	1.01	1	1	1	1	1
RE1 (K Ω)	5.38	5.6	5.6	5.36	5.36	5.36
RE2 (KΩ)	5.91	5.6	6.2	5.9	5.9	5.9
RE3 (KΩ)	5.52	5.6	5.6	5.62	5.49	5.49
$RL(K\Omega)$	142.07	150	150	140	143	142
C1 (µF)	23.00	22	22	22.6	23.2	22.9
C2 (µF)	64.12	68	62	64.9	63.4	64.2
C3 (µF)	80.24	82	82	78.7	80.6	80.6
C4 (µF)	12.55	12	13	12.7	12.4	12.6
C5 (µF)	69.38	68	68	68.1	69.8	69
$rx1(\Omega)$	15.02	15	15	14.7	15	15
rx2 (Ω)	11.92	12	12	12.1	11.8	12
rx3 (Ω)	11.54	12	12	11.5	11.5	11.5
Cµ1 (pF)	3.08	3.3	3	3.01	3.09	3.09
Cµ2 (pF)	2.85	2.7	2.7	2.87	2.87	2.84
Cµ3 (pF)	5.21	5.6	5.1	5.11	5.23	5.23
Cπ1 (pF)	9.95	8.2	9.1	9.53	9.76	9.88
Cπ2 (pF)	6.40	6.8	6.2	6.49	6.34	6.42
Сπ3 (pF)	16.35	15	16	16.2	16.2	16.4

Table 4. Performances associated to the optimal values

	$A_V(dB)$	$Z_{IN}(K\Omega)$	$Z_{OUT}\left(\Omega ight)$	F _L (Hz)	$F_{\rm H}({\rm MHz})$	P (mW)
Linear values	44.85	47	43	44.2	45.3	44.8
E12	68.87	68	68	68.1	68.1	69.0
E24	45.50	47	47	46.4	45.3	45.3
E48	72.10	68	75	71.5	71.5	72.3
E96	41.30	39	43	42.2	41.2	41.2
E192	85.73	82	82	86.6	86.6	85.6

5. COMPUTING SPICE PARAMETERS AND SIMULATION

5.1. Computing SPICE parameters

The following step-by-step procedure leads to the required spice parameters, indicated by boldface characters in the equations [25].

a. Compute the "transport saturation current" using:

$$\mathbf{IS} = \mathbf{I}_{\mathbf{C}} \exp\left(\frac{-\mathbf{V}_{\mathbf{BE}}}{\mathbf{V}_{\mathbf{T}}}\right)$$
(34)

Where: $V_T = \frac{KT}{q}$.

b. The ideal "maximum forward beta" without correction for Early effect is given by:

 $\mathbf{BF} = \beta \tag{35}$

c. Compute h₁₁ from:

$$h_{11} = \frac{\beta V_T}{I_C}$$
(36)

d. Compute the "forward Early voltage" using:

$$\mathbf{VAF} = \rho \mathbf{I}_{\mathbf{C}} \tag{37}$$

Where I_C , is the bias current at which the h-parameters were measured.

e. Compute the value of the "zero-bias base resistance" using:

$$\mathbf{RB} = \mathbf{r}_{\mathbf{x}} \tag{38}$$

f. Determining CJC:

For $C\mu$, SPICE determines collector-base capacitance from:

$$C\mu = \frac{CJC}{\left(1 + \frac{V_{CB}}{VJC}\right)^{MJC}}$$
(39)

 V_{CB} is the Q-point collector-base voltage that SPICE will determine during the dc analysis. We need to specify MJC, VJC, and CJC so that when SPICE runs a simulation, the resulting Cµ will match the desired value.

Reasonable values for MJC and VJC are MJC = 0.5, VJC = 0.7 V.

To find CJC the "base-collector zero-bias depletion capacitance", the value of $C\mu$, will be given as well as the voltage, V_{CB} , at which the measurement was made.

g. Determining CJE:

For $C_{\pi}\!,$ SPICE determines the base-emitter junction capacitance C_{je} and the diffusion capacitance C_{b} and add these:

$$C_{\pi} = C_{je} + C_b \tag{40}$$

$$C_{\pi} = 2 \times CJE + \frac{\beta}{h_{11}} TF$$
(41)

Here TF is the forward transit time. We need to specify CJE and TF, so that when SPICE runs a simulation, the resulting $C\pi$ will match the desired value. To find CJE, we set TF = 0s, and modeling C_{π} by the junction capacitance alone.

$$C_{\pi} = 2 \times CIE \tag{42}$$

5.2. Simulation

For our simulation we use the 2N2222A NPN BJT, the data sheet of the transistor contain the information needed to find IS, below is a plot of V_{BE} vs. I_C for the used transistor [26]. Figure 4 shows the Base – emitter voltage.



Figure 4. Base – emitter voltage

From the plot above, for I_C = 0.5mA we have V_{BE} = 0.62 V at 25°C, and V_T = 26mV at the same temperature. From (34), IS= 22×10^{-15} A. The following Table 5 presents VAF calculated from (37) corresponds to each transistor.

Table 5. Values of VAF					
	Transistor 1	Transistor 2	Transistor 3		
VAF (V)	0.52	0.54	0.81		

A DC analysis reveals that V_{CB} for the circuit is 1.56 V, from (39) and (42), we find CJC and CJE correspond to the three transistors, as shown in Table 6. After setting SPICE parameters, we simulate the three-stage amplifier and we have the frequency response curve of the voltage gain for E12 as shown in Figure 5, we notice that the mid-band gain is 19.12 dB, the upper cutoff frequency is 14.11 MHz and the lower cutoff frequency is 33.56 Hz, that we give a mid-band equal to 14.10MHz.

Table 6. Values of CJC and CJE for E12				
	Transistor 1	Transistor 2	Transistor 3	
CJC (pF)	6.33	5.18	10.75	
CJE (pF)	4.10	3.40	7.50	



Figure 5. Frequency response curve of the voltage gain for the three-stage amplifier

6. CONCLUSION

In this paper, we have presented an application of the Genetic Algorithm for the optimal design of three-stage bipolar transistor amplifier. We selected the optimal values of discrete components from different manufactured series and we gave the optimal values for the hybrid parameters of the transistors. The design of the amplifier with the targeted performances is successfully realized by using the GA method, validity of the proposed technique was proved via SPICE simulation.

REFERENCES

- [1] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, *Analysis And Design Of Analog Integrated Circuits*, John Wiley & Sons, Inc. Fourth Edition, 2001.
- [2] O. J. Ushie, M. Abbod, and E. C. Ashigwuike, "Naturally Based Optimisation Algorithm for Analogue Electronic Circuits: GA, PSO, ABC, BFO, and Firefly a Case Study," *Journal of Automation & Systems Engineering*, vol. 9, no. 3, pp. 173-184, 2015.
- [3] O. J. Ushie, "Intelligent optimisation of analogue circuits using particle swarm optimisation, genetic programming and genetic folding," Thesis, Brunel University London, 2016.

- [4] I.H. Osman, J.P. Kelly (Eds.), *Meta-heuristics: theory and applications*, Kluwers Academic Publishers, Boston, 1996.
- [5] Laxmi A. Bewoor, V. Chandra Prakash, Sagar U. Sapkal, "Comparative Analysis of Metaheuristic Approaches for Makespan Minimization for No Wait Flow Shop Scheduling Problem," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 7, no. 1, pp. 417-423, Feb 2017.
- [6] M. Dorigo and S. Krzysztof, An Introduction to Ant Colony Optimization, a chapter in Approximation Algorithms and Metaheuristics, a book edited by T. F. Gonzalez. 2006.
- [7] M. Krishnaveni, P. Subashini, T.T. Dhivyaprabha, "Improved Canny Edges Using Cellular Based Particle Swarm Optimization Technique for Tamil Sign Digital Images," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 6, no. 5, pp. 2158-2166, Oct 2016.
- [8] J. Dreo, A. Pe'trowski, P. Siarry, E. Taillard, *Metaheuristics for hard optimization: Methods and case studies*, New York: Springer, 2006.
- [9] B. Benhala and O. Bouattane, "GA and ACO techniques for the analog circuits design optimization," *Journal of Theoretical and Applied Information Technology (JATIT)*, vol. 64, no. 2, pp. 413–419, 2014.
- [10] F. Glover, "Tabu search-part I," ORSA Journal on computing, vol. 1, no. 3, pp. 190-206, 1989.
- [11] F. T. S. Chan, M. K. Tiwari, *Swarm Intelligence: focus on ant and particle swarm optimization*, I-Tech Education and Publishing, 2007.
- [12] B. Benhala, "An improved aco algorithm for the analog circuits design optimization," International Journal of Circuits, Systems and Signal Processing, vol. 10, pp. 128-133, 2016.
- [13] L. Kritele, B. Benhala, and I. Zorkani, "Ant Colony Optimization for Optimal Low-Pass State Variable Filter Sizing," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 8, no. 1, pp. 227-235, Feb 2018.
- [14] L. Kritele, B. Benhala, I. Zorkani, "Optimal Digital IIR Filter Design Using Ant Colony Optimization," *IEEE 4th International Conference on Optimization and Applications (ICOA'18)*, Mohammedia, Morocco, pp. 1-5, Apr 2018.
- [15] H. Bouyghf, B. Benhala and A. Raihani, "Optimization of 60-GHZ down-converting CMOS dual-gate mixer using artificial bee colony algorithm," *Journal of Theoretical and Applied Information Technology (JATIT)*, vol. 95, no 4, pp. 890–902, 2017.
- [16] H. Bouyghf, B. Benhala and A. Raihani, Optimal design of RF CMOS circuits by means of an artificial bee colony technique, Chapter 11, Book: Focus on swarm intelligence research and applications, Eds., B. Benhala, P. Pereira and A. Sallem, NOVA Science Publishers, pp. 221–246, 2017.
- [17] H. Bouyghf, B. Benhala, A. Raihani, "Analysis of the impact of metal thickness and geometric parameters on the quality factor-Q in integrated spiral inductors by means of artificial bee colony technique," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 9, no. 4, pp. 2918-2931, Aug 2019.
- [18] R.L. Haupt and S.E. Haupt, Practical GeneticAlgorithms, (book) John Wiley & Sons, 2004.
- [19] V. Z. Manusov, P. V. Matrenin, E. S. Tretiakova, "Implementation of Population Algorithms to Minimize Power Losses and Cable Cross-Section in Power Supply System," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 6, no. 6, pp. 2955-2961, Dec 2016.
- [20] M. Montazeri-Gh, A. Poursamad and B. Ghalichi, "Application of genetic algorithm for optimization of control strategy in parallel hybrid electric vehicles," *Elsevier, Journal of the Franklin Institute*, vol. 343, no. 4–5, pp. 420-435, Jul–Aug 2006.
- [21] I Gede Pasek Suta Wijaya, Keeichi Uchimura, Gou Koutaki, "Traffic Light Signal Parameters Optimization using Modification of Multielement Genetic Algorithm," *International Journal of Electrical and Computer Engineering* (*IJECE*), vol. 8, no. 1, pp. 246–253, Feb 2018.
- [22] S. Yang, R. Tinós, "A hybrid immigrants scheme for genetic algorithms in dynamic environments," Springer, International Journal of Automation and Computing, vol. 4, no. 3, pp. 243–254, Jul 2007.
- [23] A. A. Gozali, S. Fujimura, "Reinforced Island Model Genetic Algorithm to Solve University Course Timetabling," *TELKOMNIKA (Telecommunication, Computing, Electronics and Control)*, vol. 16, no. 6, pp. 2747–2755, Dec 2018.
- [24] A. Yani, J. Junaidi, M. Irwanto, A. H. Haziah, "Optimum reactive power to improve power factor in industry using genetic algorithm," *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, vol. 14, no. 2, pp. 751–757, May 2019.
- [25] N.R. Malik, "Determining Spice Parameter Values for BJT's," *IEEE Transactions on Education*, vol. 33, no. 4, Nov 1990.
- [26] 2N2222A Small Signal Switching Transistor Datasheet, [Online], Available: http://onsemi.com.