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A novel optimization framework for controlling stabilization issue in design principle of FinFET based SRAM

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ABSTRACT

The conventional design principle of the finFET offers various constraints that act as an impediment towards improving ther performance of finFET SRAM. After reviewing existing approaches, it has been found that there are not enough work found to be emphasizing on cost-effective optimization by addressing the stability problems in finFET design.Therefore, the proposed system introduces a novel optimization mechanism considering some essential design attributes e.g. area, thickness of fin, and number of components. The contribution of the proposed technique is to determine the better form of thickness of fin and its related aspect that can act as a solution to minimize various other asscoiated problems in finFET SRAM. Implemented using soft-computational approach, the proposed system exhibits that it offers better energy retention, lower delay, and potential capability to offer higher throughput irrespective of presence of uncertain amount of noise within the component.

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1. INTRODUCTION

The explosive growth of digitization demands an alternative to CMOS planar technology. The CMOS based devices suffer from many challenges such as higher current leakage, less reliable, huge parameter variation due to gate loosing of control over the channels [1]. However, FinFET has been emerged as technology that has a potential to mitigate the problem of planar FETs. The FinFET is designed with the multiple gates surrounded around the thin channel that offers 10nm of transistor design and provides fully depleated operation that enhances the better electrical characteristics and reduces the problem of short channel effects, gate leakage and decreasing mobility [2]. Among this, FinFITs are drawing a big interest for occupying the major area of designing SRAM memory chips. The conventional SRAM memory chips are based on the CMOS technology also suffers from the issue of bad performance due to higher current leakage and higher power dissipation [3]. The SRAM have to perform three significant tasks in the storage management that is read, write and standby operations. So, it is required to have less energy dissipation, low leakage problem and fast processing and provides high performances [4]. Due to this FinFET based SRAM is more expected to gain high performance and is more recommended over CMOS based SRAM [5].

Therefore, it has been noticed that various research works have carried towards FinFET based SRAM design by considering the circuit, device and technological challenges and issues [6-8]. Also, this paper presents literature work to understand the current trends and the progress of FinFET SRAM technique. Furthermore, along with the flexible benefits of FinFIT based SRAM technology, there exist some major challenges that also need to be overcome when designing the memory circuits. Such challenges can be

represented as design conflict of SRAM read & write stability, width quantization issue, process variation, limited manipulation of spacer, heating problem and etc [9, 10]. Therefore, it is very important to explore some effective design consideration and optimization scheme for designing efficient FinFET based SRAM memory circuits.Therefore, the present paper introduces a simple solutions where stability problems has been addressed using a simple iptimization technique. Discussion of the related work associated with FinFET is carried out in Section 1.1 with respect to different methods and techniques. Briefing of identified research issues is carried out in Section 1.2 while highlights of solutions to address this problem are carried out on Section 1.3. Design of algorithm is carried out on Section 2 while analysis of obtained result is discussed in Section 3 and summary of paper in Section 4.

This section presents existing research works that carried out in the domain of FinFET SRAM Optimization. The work discussed by by Song et al. [11] have implemented 128 mb 6 Transistors SRAM into 10 nm FinFET transistor with different SRAM assists various operation in order to investigate the performance, power and area gain and figure-of-merit which is used to evaluate different types of bitcells. In [12] Kulkarni et al. have introduced a sensing technique for obtaining high density with 256 bit per bitline in 8T SRAM arrays by utilizing low-signal pseudo-differential and single-ended sensing mechanism. Wang et al. [13] have presented an improved Compact model consists of extraction and generation mechanism for achieving higher statistical precision by analysing the relationship between the process and numerical variability. The model is tested on TCDA tool which demonstrate that presented technique provides optimizing tool kit for Circuit designing.

Sakhare et al. [14] have offered targeting mechanism for 10-nm FinFET SRAM by considering capacitance in order to establish technology high density SRAM bit cell. Tang et al. [15] have presented a model based on Taylor expansion and genetic algorithm for examine the FinFET circuit devices under various parameters variations such as power, voltage and temperature. Asenov et al. [16] have applied co-optimization tool to 22 nm FinFET based CMOS technology to demonstrate the FinFET to demonstrate the sensitivity of the FinFET to the fin-shaped changes induced by the process. In [17] the author have presented an optimal scheme for designing 22nm FinFET 6T SRAM cell for achieving increased read and write access time. Lim et al. [18] have utilizes a hybrid model to evaluate stability and power consumption of 14nm FinFET- 6T SRAM for direct current and Transient analysis. Similarly, the study of [19] Bhoj et al. have evaluated several symmetric-gate workfunctions and introduced an approach on the basis of analytical approach for designing Parasitic based asymmetric gate work-functions of FinFET based SRAM.

Sikarwar et al. [20] have described 6T SRAM based on independent FinFET technology in order to reduce total energy consumption. In addition, the authors have applied reduction technique for mitigating current leakage problem. Patil and Bhaaskaran [21] have compared various different adiabatic SRAM cell with DSM and UDSM nodes in terms of their power and energy parameters. The outcomes of presented approach display that energy consumed by FinFET based 8T and 9T SRAM cell is lesser than the existing 6T CMOS based SRAM. In [22] Kang et al. have presented an design approach that includes Fin thickness, height and surface orientation for optimizing the stability, current leakage, read and write delay factor of FinFET SRAM. The outcomes of study reveals that the FinFET based SRAM achieves great margins in noise that occurs in read and write process then traditional planer SRAM.

Pal et al. [23] have presented an optimization approach by using high-k Spacers technique for FinFET based SRAM. The outcome shows that the SRAM achieves good stability and access time. In [24] Bhattachrya and Jha have carried a review on FinFET technology from device level to design level for analyzing the advantages, impact and optimization characteristics. The works of Goel et al. [25] have presented analysis of un-symmetric drain spacer and afterward they have applied an optimization technique for gaining low power and robust FinFET SRAMs. The experimental observation demonstrate that the presented technique achieves about 57% in current leakage, about 11% and 6% enhancement in read and write noise margins respectively and improved access time with 7% increment. In [26] Sachid and Hu have presented another approach for optimizing the reading stability and minimizing cell leakage in FinFET SRAM.

The work of Hu et al. [27] have presented an approach of temporal variability and time intrinsic value for optimizing the design orientation of FinFET in order to improve the stability with Oxide and variability with high-k dielectrics of the 6T-SRAM. Ebrahimi et al. [28] have applied PSO based back- gate voltage concept with statistical optimization mechanism to improve the overall performance of FinFET based SRAM cells. In [29] Kushwah and Akashe have offered a mechanism for improving the quality and stability of noise margin in FinFET 6T SRAM. The work of Gupta and kaushik [30] have focused to co- device-ckt design model in order to achieve an improved stability and mitigating the conflicts of design in FinFET SRAM. Girish and Shashikumar [31] to reduce the computational complexity of an algorithm related to conventional method and performance upgradation of system found in the current times. Girish and Shashikumar [32] focused on FinFET based SRAM cell until today. Mounica and Ganesh [33] have

illustrated about new NVSRAM circuit that generates superior "instant-on operation" related to previous methods used in SRAM's. Riyadi et al. [34] have demonstrated the influence of gate material and process on subthreshold performance of junctionless FET, by comparing four sets of gate properties and process methods. The next section outlines the problems associated with the existing approaches.

The core issues associated with existing system are as follows:

- Existing literature doesn't emphasize on the significance of the thickness factor assocaiated with the fins and its possible connectvity with the optimization performance.
- There are less work towards exploiting distance-based parameters for the components involved in the design principle of FinFET SRAM.
- A soft computational model with simplified approach was less in used towards identifying the problems associated with stability issues in FinFET SRAM.
- Energy problems and its possible relation with dimensional aspect of fins and its number are never studied in existing system.

Therefore, the statement of significant research issue can be stated as "To develop a soft computational model for implementing multi-objective function in order to optimize the stability performance of bit cells of FinFET SRAM is quite challenging".

The proposed work is a continuation our prior optimization work over finFET SRAM [35]. The proposed system implements an analytical research methodology with a prime goal of performing design optimization on FinFET SRAM. In order to accomplish this target, the proposed system implements mechanism of optimizing the stability performance as well as address the delay factor associated with write-read energy dissipation etc. The adopted methodology is highlighted in Figure 1.

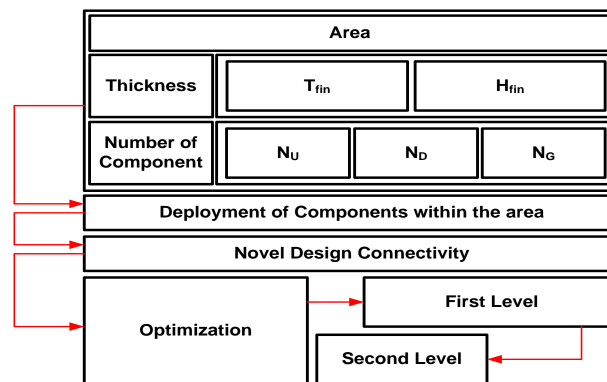

Figure 1. Schema of proposed methodology

The proposed model takes different types of inputs associated with area and components of bit cells of FinFET SRAM. A simulation-based model is used in order to perform stabilization of the performance. The study considers that thicknesses of fin T_{fin} as well as height H_{fin} are some essential parameters that need to be determined precisely in order to ensure better optimization performance. These two parameters have potential effect over the threshold voltage V_{th}. The novelty of the proposed system is that it offers a better investigation platform towards energy consumption as well as delay factor associated with the proposed optimization plan that is carried out in two levels. With diversified components consideration e.g. fins associated with pull up transistor NU, fins of pull down transistor ND, and fins of pass gate transistor PG, the proposed system has been evaluated. The next section illustrates the algorithm implementation of proposed system.

2. ALGORITHM IMPLEMENTATION

The core motive of the proposed algorithm is to implement a sequential set of operation in order to improve performance of bit cell of FinFET-based SRAM using tree-based logic. The prime idea of the proposed algorithm implementation is to encourage the usage of fin thickness as it could offer better resistance against short channel effect. At the same time, the proposed design also emphasize on improving the fin-height parameter in order to improve the width of an effective channel. The algorithm also emphasize on the optimizing the saturation current that is also directly dependent on the fin thickness.

Algorithm for Stability Optimization
Input: *A* (area), *n* (number of component), R_c (total thickness), *e* (number of event)
Output: fluctuation parameter (τ)
Start
1. init A, n, Rc, e
2. **For** i=1:n
3. estm $d \rightarrow f(d_1, d_2)$
4. $ix \rightarrow d<R_c$
5. **End**
6. **For** i=1:length(ix)
7. **If** $\tau_1 > \tau_2$
8. $\tau_2 \rightarrow \tau_1 + E_r/E_{max}$
9. **Elseif** $\tau_1 == \tau_2$
10. $c\tau_2 = c\tau_2$
11. **If** $st_2 \leq st_1$
12. $\tau_2 = \{\tau_1, st_2\}$
13. **End**
14. **End**
15. **End**
16. **If** aa=1
17. $\tau_1 \rightarrow (\tau, H_{fin})$
18. **End**
19. $arg_{min}(\tau 1)$
End

The above algorithm is essentially meant for offering more stabilization over the performance of conventional design of FinFET-based SRAM. The algorihm takes the input of *A* (area), *n* (number of component), R_c (total thickness), and *e* (number of event) that after processing yields to an outcome of fluctuation parameter (τ). The first essential step of the proposed algorithm is to consider all the spatial measurements of the FinFET-based SRAM that consists of fins, gate, contact, etc. Following are the implementation steps carried out for the above mentioned algorithm:

- *Deployment of Components within the area*: This is the first step that ensures a proper optimization of an area; therefore, it chooses the fin thickness T_{fin} as an explicit fraction of area A considering all the components (Line-2). It also ensures that there are only specific set of fin number possible in order not to oversaturate the area A. Proposed study considers fin thickness as $1/4^{th}$ of the area A. A random placement strategy is adopted for positioning the components within the area. The component postion [(x, y) =*random* (A)] are saved in temporary memory (say *xy* matrix). The proposed study also considers a sink fin and positions it within A. Therefore, there are two forms of components i.e. event capturing components with position matrix (xy) and component to dump all the information in the form of sink with position matrix ($x_s y_s$).
- *Novel Design Connectivity*: The proposed system implements a hierarchical organizing map where all the components are considered (Line-2) and assessessment of distance among the components are evaluated (Line-3). The variable d_1 and d_2 corresponds to the position of all normal components i.e. (x, y) with the sink components (x_s, y_s). An explicit function f(x) is implemented in order to obtain the effective spatial factor d between d_1 and d_2 (Line-3). In order to resist in anyfor of interference or noise related effect, it is needed that the component fins are well connected to the gates. For this purpose, a logical condition is stated where it finds that the effective distance should be kept less than or equal to total thickness of the component (Line-4). During establishing the component connectivity, various parameters thatcontributes to energy consumptions are also initialized (e.g. Energy consumed in electrical circuits (E_e), Energy required for amplification (E_a), Size of data (d_{size}), Maximum energy (E_{max}) etc). Therefore, the variable *ix* represents only the effective components that are performing event-based communication. The proposed system also constructs two fluctuation parameter τ_1 and τ_2. The first parameter τ_1 is thickness of fin (i.e. T_{fin}) while second parameter is related to various factor that gets affected if T_{fin} is reduced i.e. saturation current, reduce short channel effect, read static noise margin, and threshold voltage. According to observation from various existing system, it was found that if the thickness of the fin is reduced than it also reduces short channel effect, reduces saturation current, increases noise and also increases threshold voltage. Therefore, the condition stated in Line-7 of algorithm directs to the condition of enhanced

outcome in order to investigate an effective value of T_{fin}. As the proposed system also targets about reviewing the energy consumption so it includes energy parameters associated with second parameter τ_2 (Line-8). However, there is also good probability of these fluctuation parameters to be same (Line-9). In such case, the proposed system computes the state-based parameter st obtained by dividing remaining energy divided by maximum energy (Line-10-11). In case of achieving a lower value of new state of event compared from its previous state by the FinFET SRAM (Line-11), the proposed system performs the updating operation of the state. More the updating operation is performed, the proposed system can obtain more information associated with its current state thereby contributing to the lowering the instability of the states by the FinFET SRAM. The above operations are applicable for multiple events and how to schedule them. In case there is single event occurred (Line-16) than the effective T_{fin} is obtained from the aggregated value of τ and height of fin H_{fin}. Therefore, the proposed algorithm successfully finds an effective T_{fin} and H_{fin} that directly assist in optimizing (Line-19) the bitcells of FinFET SRAM.

- *First level Optimization*: This level of operation takes the input of number and range of events along with size of data to the processed through FinFET SRAM. Assuming that the nodes are supplied with internal battery system, the proposed system searches for the component where E_o is less than or equal to zero. More number of events is randomly generated in order to assess the further instability in new random position of components (ex, ey).
- *Second level Optimization*: This is the final process of performing optimization. In this process, the proposed algorithm is simulated for all the number of events. Following steps are further performed:
  - Updated effective distance between the random instable components and components that has recently received an event. It assists in identifying the components that has higher possibility of malfunctioning without using any new components or devices or adding extra fin thickness.
  - The best component is found for all the values of *ix* obtained from Line-4. In this process, the matrix constructed from τ_1 is accessed in order to obtain all the possible values matching with *ix*. This process results in updating τ_2 matrix thereby resulting in minimizing random dopant fluctuation. The obtained value is further minimized (Line-20).
  - Assessment with data dumping on sink is followed as a next step. In this process, the proposed system considers that data could be dumped directly to the sink or using multiple number of gates to further process and forward it as an aggregated value to the sink. For better form of an optimization, the proposed system considers that the maximum fin number will not be more than 2 in order to ensure that proposed system doesn't overpopulate the area.
  - A closer look into the proposed system shows that there will be always certain level of T_{fin} and random dopant fluctuation that will evolve during any events that is unpredictable and uninevitable. However, the proposed system performs identification of the fin numbers present within the component with respect to transistors. The study considers that there are three types of fins that are used for pull-up transistor, pull-down transistor, and pass gate. In order to control large scale of noise, the proposed system ensures that the number of fins in pass gate transistor should be kept less than number of fins associated with the pull-down transistor. This logic offers significant stability that directly reduces in delay problems associated with write-read operation in bit cell of FinFET SRAM.

Hence, the discussion highlights a significant algorithm implementation, which is not only new but also very simplified mechanism to implement it using a soft-computational model. The target of the proposed algorithm is essentially meant for reducing the factors as well as events that result in unstability in the operation of FinFET SRAM. Another uniqueness of the proposed algorithm is that it doesn't perform any form of iterative operation and always adopts a highly streamlined and progressive flow. This operational design has positive effect on reducing the computational complexity associated with proposed system. The consecutive section of this paper discusses about the results obtained.

3. ANALYSIS OF OBTAINED RESULT

The implementation of the proposed system is carriedout over MATLAB considering T_{fin}=0-10 nm and H_{fin}=10-40nm. The energy of the component is initialized to 10 joules. The obtained outcome of the simulation was also compared with similar cadre of optimization work being carried out by Kang et al. [22] and Ebrahimi et al. [36]. As the proposed system mainly targets for stability control using optimization principle over new design principle of FinFET SRAM; therefore, it is assessed with respect to different forms of performance parameters that are discussed as below.

Figure 2 highlights that proposed system offer better retention of the energy in a test 1400 simulation rounds and this is much better than exising approach of Kang et al. [22] and Ebrahimi et al. [32]. The prime reason behind this is approach of Kang et al. [22] includes too many parameters for minimizing

Vth; however; it couldn't balance with energy saving. Similarly, the approach of Embrahimi et al. [32] includes too much iterative-based approach where complete focus was towards constructing and obtaining data for failure metric. This process consumes maximum energy as well as it also result to higher degree of instability (Figure 3). The discontinuation as well as steep fall of curve for Ebrahimi et al. [36] is the evidence about it. Hence, proposed system offers both energy efficiency as well as better stability performance.

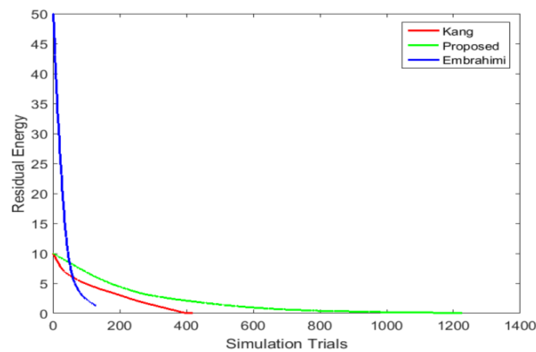

Figure 2. Comparative analysis of residual energy

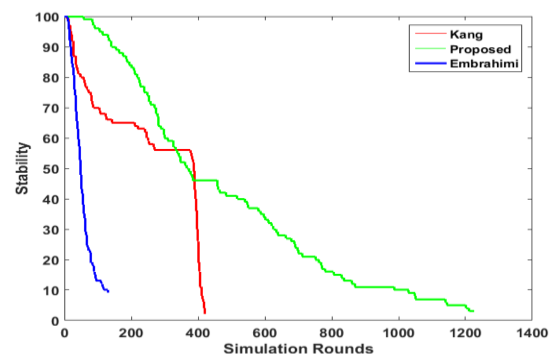

Figure 3. Comparative analysis of stability

The better form of optimization performance could be also seen by higher throughput and lower delay as seen from Figure 4 and Figure 5 respectively. Owing to progressive operation imposed by the proposed system that target to find the best combination of the T_{fin} with respect to side channel effect, satirated current, and thresholded voltage, the proposed system invokes usage of multi-objective optimization principle resulting in a better balance between the operation of random event processing by the best components in FinFET SRAM as well as proposed system performs complete operation over runtime with no dependency of any form of internal memory management system. Therefore, such simplistic matrix-based approach has significantly assisted to imrove the optimization performanve of proposed system.

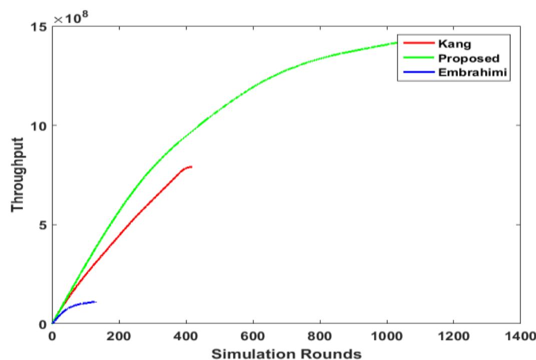

Figure 4. Comparative analysis of throughput

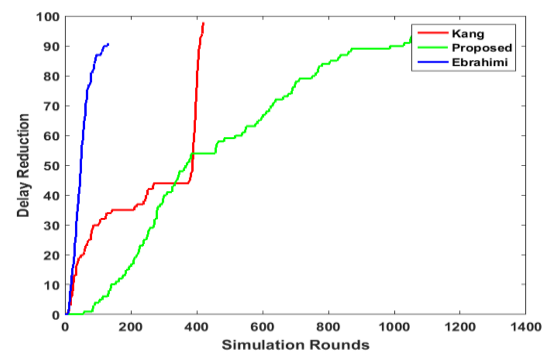

Figure 5. Comparative analysis of delay reduction

4. CONCLUSION

Compared to conventional approach, FinFET based SRAM offers highly faster switching time as well as the density of its current is also very high. However, with the involvement of various parameters in its design, iit has been seen that it offers instability problems. For an example lowering the Tfin also lowers the side channel effect, which is good; however, such lowering of Tfin to higher extent is never practically possible. Hence, it leads to stability problems in FinFET device that calls for optimization. The proposed system implements a multi-objective function in order to stabilize the performance considering multiple attributes associated with FinFET. The study outcome is also found to be highly improved in contrast to existing system.

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